Materials to System Co-optimization (MSCO^{TM}) for SRAM and its application towards Gate-All-Around Technology

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***Abstract*—In this paper, we deploy our SRAM MSCO framework to evaluate the GAA SRAM performance and explore different performance optimization strategies. Our modeling indicates that GAA SRAM can have better stability, writability and read-current compared to FinFET SRAM, primarily due to better electrostatics and drive-strength ratio between nMOS and pMOS. Furthermore, we show that design optimizations through varying nanosheet count, nanosheet width and RMG workfunction allows GAA SRAM to be tailored for different applications.**

***Index Terms*—SRAM, GAA, FinFET, DTCO, SNM, Write Margin, circuit design, device modeling.**

I. Introduction

With scaling of device dimensions and supply voltages, the energy efficiency of the SoC can see tremendous improvement [1]. SRAM is a critical component of the SoC in regard to energy consumption since it can impose a limitation on the minimum operating voltage and standby leakage for the entire SoC. In this paper, we explore the design space of GAA SRAM and compare its performance to FinFET SRAM, with focus on the stability, readability and writability operations. In particular, we explore different GAA design elements and investigate their impact on the SRAM performance.

GAA and FinFET-based SRAM: Structure and Characterization Flow

(a) Key Transistor Dimensions (b) SRAM Characterization Flow

FinFET	Value
Fin Height	60 nm
Fin Width	5 nm
W-eff	125 nm

GAA	Value
NS width	10 nm
NS thickness	5 nm
W-eff	90 nm

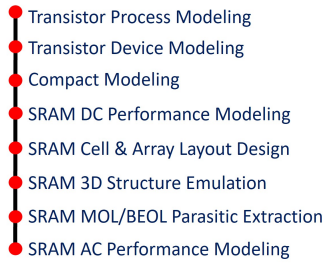

Fig. 1. (a) Typical device dimensions at the 3 nm technology node show FinFET has higher W-eff compared to GAA. (b) Description of the SRAM characterization flow.

SRAM Bitcell Layout

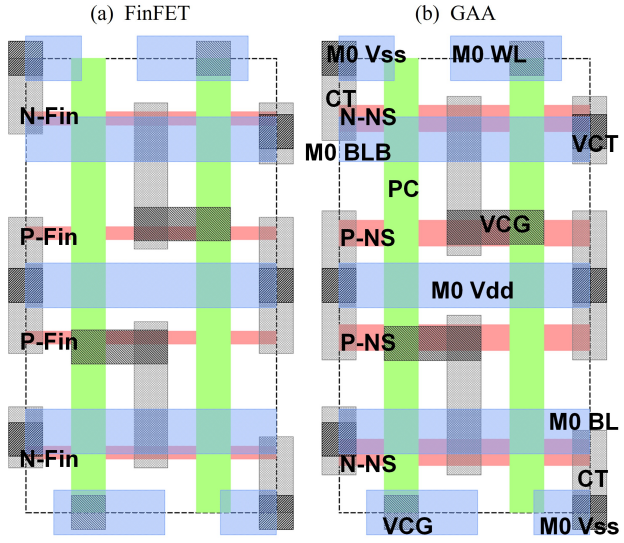

Fig. 2. SRAM schematics of (a) FinFET and (b) GAA transistors at the 3 nm technology node.

II. SRAM Modeling Framework

FinFET and GAA (3-nanosheet stack) transistors used in this study are designed with the typical dimensions (Fig. 1(a)) projected for the 3nm technology node [2]–[4]. We deploy our comprehensive Materials to Systems Co-Optimization (MSCO^{TM}) [5] framework to analyze and compare high-density 1-1-1 SRAM performances. Fig. 1(b) describes the process flow used to characterize the SRAM performance, while Fig. 2 shows the 6-transistor (6-T) FinFET and GAA SRAM bitcell layouts used in this study. The FEOL transistor-level performances are characterized using advanced drift-diffusion transport models calibrated to the self-consistent solution of the Schrodinger, Poisson and subband Boltzmann transport equations [6], [7]. For the SRAM cell and array performance analyses, compact models [8] calibrated to the aforementioned FEOL characteristics are used, together with MOL/BEOL modeling and its parasitic extraction (PEX).

GAA vs FinFET: Transistor-level Performance Comparison

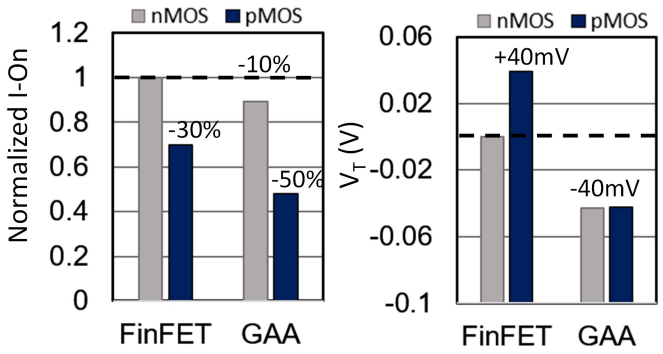

Fig. 3. Transistor-level comparison: FinFET pMOS V_T tuned to achieve greater than 1 nMOS-to-pMOS drive-current ratio for optimum SRAM performance. Higher FinFET W-eff leads to better FinFET nMOS drive current compared to GAA. FinFET pMOS performs significantly better compared to GAA pMOS due to better hole mobility along with higher W-eff. GAA nMOS-to-pMOS drive-strength ratio is ideal for SRAM operation, allowing to match their V_T matching for same target I-off

III. Results and Discussion

Figure 3 shows that the drive-strength of GAA pMOS (with Si channel and no stress) is significantly lower as compared to GAA nMOS which favors SRAM operation (particularly the writability). On the other hand, the nMOS-to-pMOS drive-strength ratio is low for FinFET due to strong pMOS performance for same threshold voltage V_T (with compressive channel stress and favorable fin side-wall orientation). Consequently, the FinFET pMOS V_T is skewed to improve the nMOS-to-pMOS drive-strength ratio, while the GAA pMOS V_T can be chosen to match nMOS V_T. As a result, compared to FinFET, the GAA SRAM has 13% higher SNM due to better V_T-matching, 5% higher I-read due to better electrostatics and 15% better write-margin due to better transistor strength-ratio, as seen in Fig. 3. Due to this, as well as lower gate capacitance (lower W-eff in Figure 1(a)), the GAA SRAM also exhibits better AC performance with 10% and 20% lower read and write delays, respectively. In the following sections, we explore different GAA performance knobs and investigate their impact on GAA SRAM performance.

GAA vs FinFET: SRAM Cell-level Performance Comparison

Metric	FinFET	GAA
SNM	0.132V	0.15V (+13%)
Write-margin	0.2V	0.23V (+15%)
I-read	16μA	17μA (+5%)
Read delay	70ps	63ps (-10%)
Write delay	50ps	40ps (-20%)

Fig. 4. GAA SRAM has better SNM due to better nMOS-pMOS V_T matching, higher I-read due to better electrostatics, and higher write-margin due to better nMOS-to-pMOS drive-strength ratio. Due to this, the GAA SRAM has better AC performance (read and write delay) compared to FinFET.

Impact of GAA pMOS Nanosheet Width

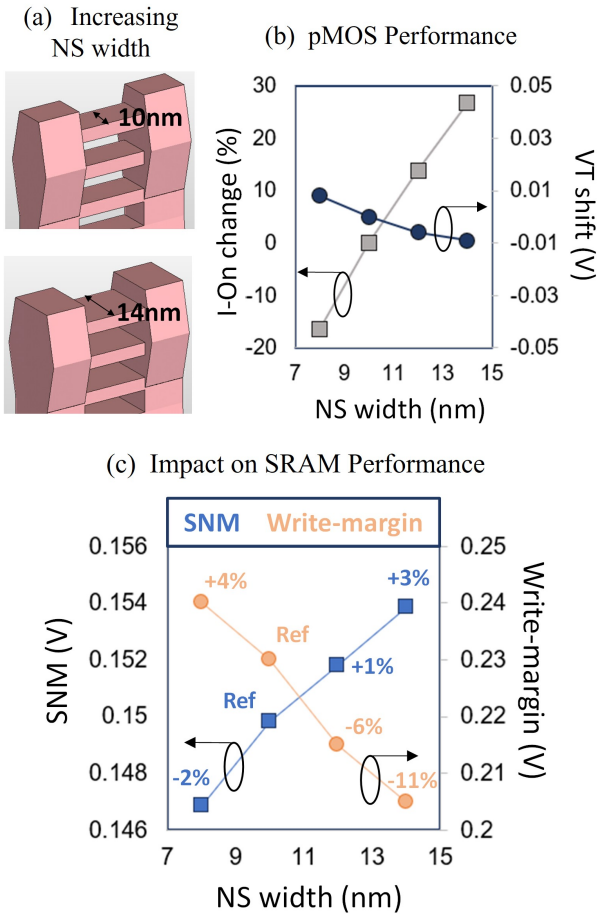

Fig. 5. (a) Increase in W-eff with higher pMOS nanosheet (NS) width leads to (b) pMOS drive-current improvement, while V_T is negligibly impacted. (c) This leads to 3% GAA SRAM SNM improvement. However, write-margin is degraded by 11% due to lowering of nMOS-to-pMOS drive-strength ratio. Reducing NS width more beneficial due to write-margin improvement.

A. Impact of GAA pMOS Nanosheet Width

The capability to tune nMOS/pMOS nanosheet (NS) widths independently is a key advantage of GAA compared to FinFET. Fig. 5(b) shows that increasing pMOS NS width by 4 nm can improve the pMOS drive current (at constant I-off) by 26% due to higher W-eff. However, the pMOS V_T is negligibly impacted by the increase in NS width. This results in only 3% improvement in the GAA SNM (Fig. 5(c)) with increase in NS width from 10nm (baseline) to 14nm. However, the GAA write-margin is degraded by 11% owing to the lower nMOS-to-pMOS drive-strength ratio. This indicates that reducing NS width can be more beneficial, leading to

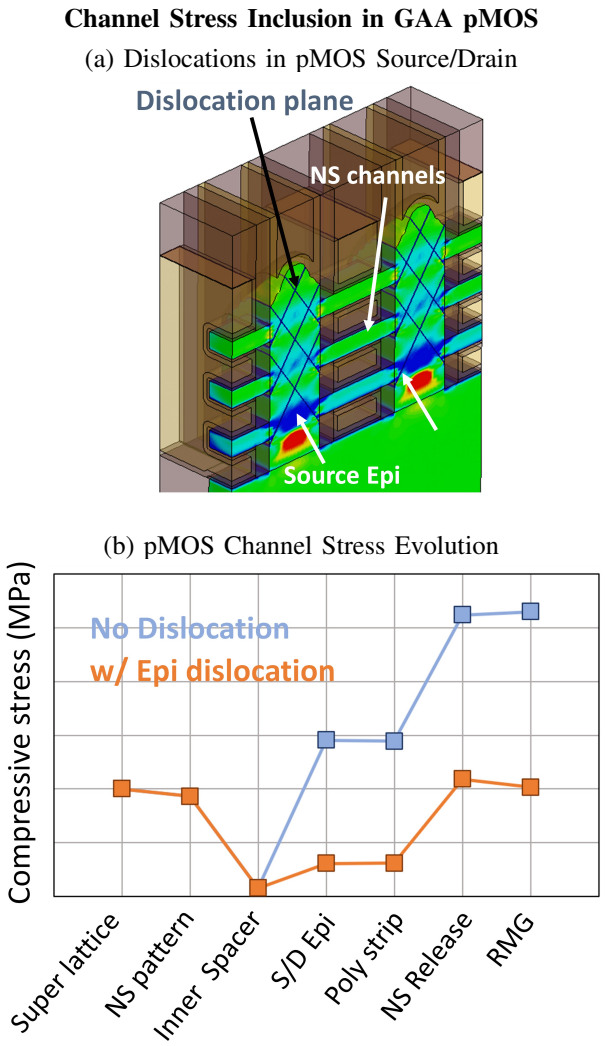

Fig. 6. (a) Channel stress relaxation due to dislocation planes in GAA S/D Epi. (b) Evolution of channel stress w/ and w/o dislocation along GAA process modules.

improvement in SRAM write-margin. SRAM I-read is not affected in this process since nMOS is unchanged.

B. Incorporating Channel Stress in GAA pMOS

Fig. 6 highlights that the compressive stress in GAA NS channel undergoes relaxation in the presence of dislocations [9] in the source/drain (S/D) Epi. Fig. 6(b) shows the evolution of channel stress in GAA pMOS at the different simulated process steps, whereby at the end, there is negligible compressive stress in the channel in presence of S/D Epi dislocations. On the other hand, when no dislocations are present, compressive stress in the GAA pMOS channel has negligible impact on the SNM (Fig. 7(a)) and I-read (Fig. 7(c)), while write-margin is degraded by 13% (Fig. 7(c)), owing to the improved pMOS drive-strength.

C. RMG Work-function Optimization for GAA pMOS

GAA pMOS V_T can be tuned using the RMG work-function (WF) to improve the stability of the SRAM cell.

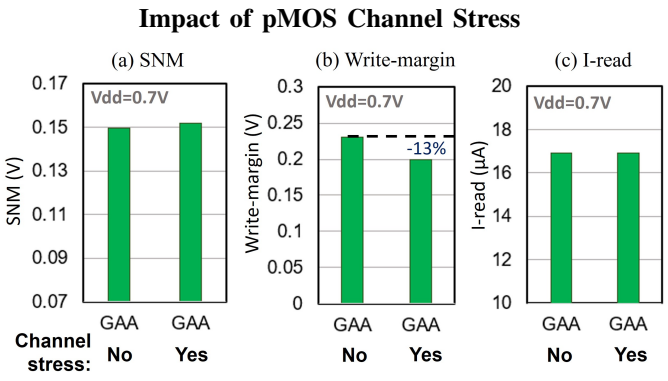

Fig. 7. Channel stress in pMOS, leads to (a) marginal improvement in GAA SNM while (b) Write margin degrades by 13% due to lower nMOS-pMOS drive strength ratio. (c) No impact on I-read as nMOS is unaffected.

Through this approach, the GAA SRAM SNM (Fig. 8(a)) can be significantly improved (over 15%) but with a penalty (over 30%) on the write-margin (Fig. 8(b)). Nevertheless, the relatively high sensitivity of this approach to SNM can be of value in applications where cell tolerance to static noise sources is prioritized over writability. An example is SRAM for advanced space applications requiring high stability to withstand flux of highly energetic particles/radiation [10]. It is important to note that the pMOS WF optimization approach comes with the caveat of increase in pMOS leakage current with lower V_T.

D. Increasing GAA Nanosheet Count

Increasing the number of NS has been an active area of study for improving GAA drive-strength [11]. Comparing 4-NS GAA with the 3-NS case in our modeling (Figs. 9(a)

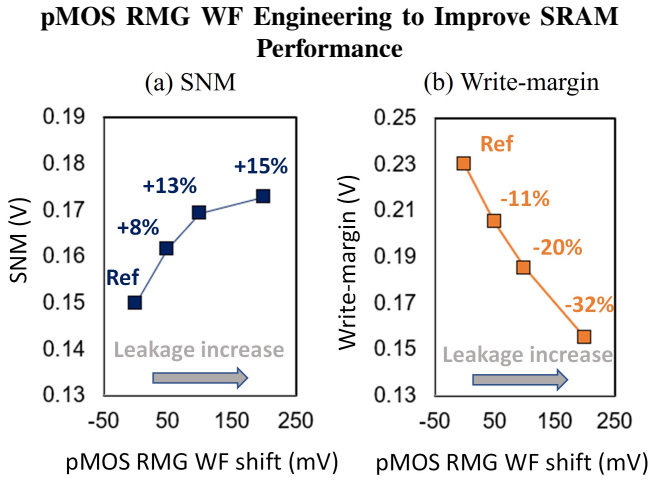

Fig. 8. : (a) pMOS GAA RMG work function (WF) optimization significantly improves SNM. (b) However, write-margin is degraded due to increase in pMOS strength. This can be a useful method to improve SRAM stability (as required for space applications). Decrease in pMOS WF is beneficial for write-critical applications, the amount of WF shift allowed is limited by the write/read delay increase at high WF shifts.

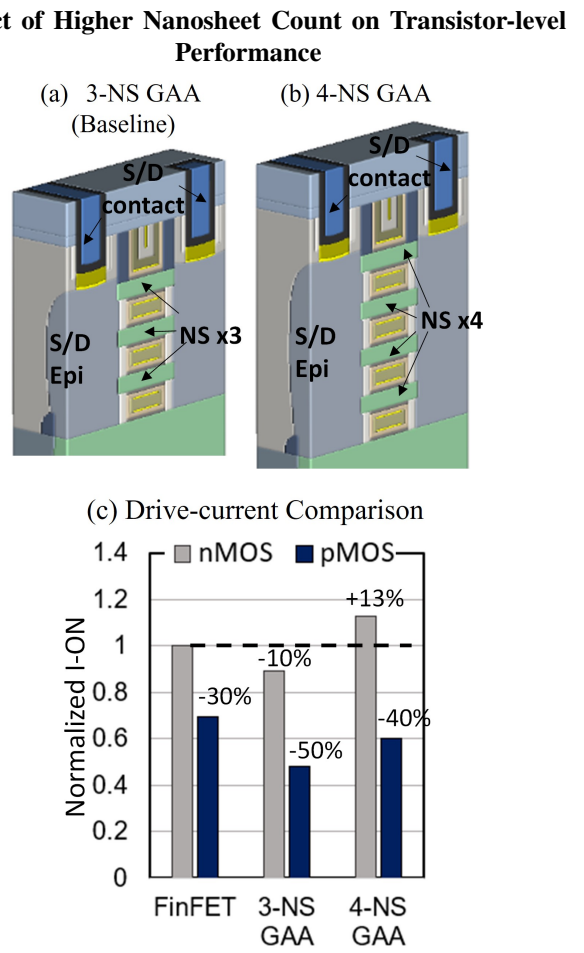

Fig. 9. (a) GAA device structures with 3- and 4-NS. (b) Drive current improvement due to increase in W-eff in 4-NS GAA.

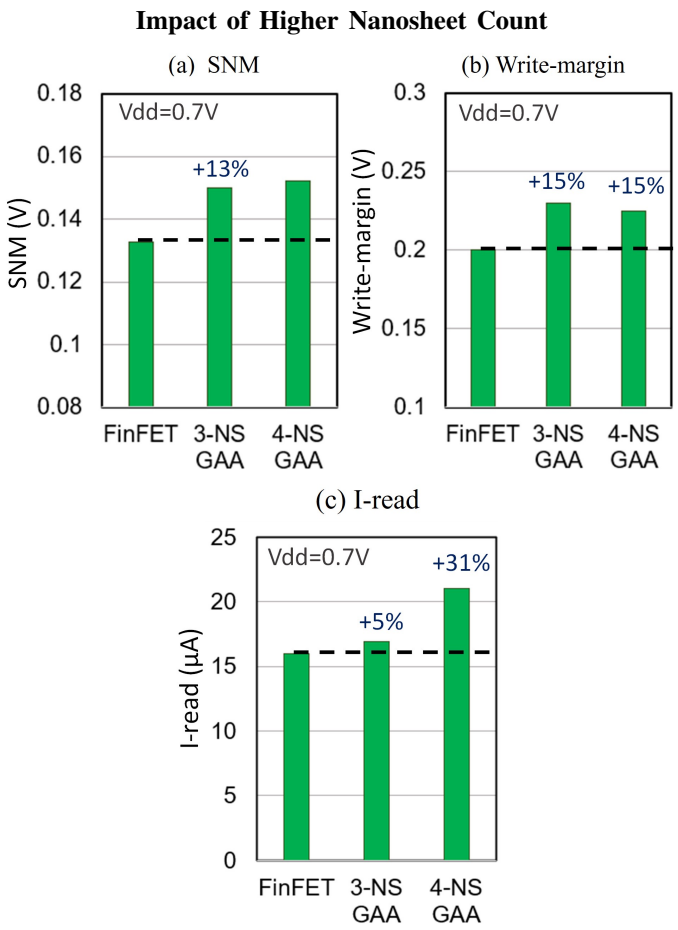

Fig. 10. (a) SNM and (b) Write-margin in 4-NS GAA SRAM are similar to the 3-NS case. On the other hand, (c) I-read in 4-NS GAA SRAM increases significantly (25% compared to 3-NS GAA) due to improvement in nMOS strength. Overall improvement in SRAM performance, useful configuration for high performance applications.

and 9(b)), we see that both nMOS and pMOS drive-strength improves by 26% (Fig. 9(c)) due to higher W-eff. However, the V_T is not affected by this process, resulting in only a small improvement (2%) in the SRAM SNM (Fig. 10(a)) for the 4-NS GAA compared to the 3-NS case. Negligible impact of increasing NS count is seen on the GAA SRAM write-margin (Fig. 10(b)) since change in the relative nMOS-to-pMOS drive strength is small. I-read, on the other hand, improves by 25% (Fig. 10(c)) due to the better drive-strength of 4-NS GAA nMOS compared to its 3-NS counterpart. Thus, our analysis shows that increasing the GAA NS count leads to an overall improvement in GAA SRAM performance, with 25% higher I-read and no penalty on the SNM and write-margin, indicating that this configuration may be better suited for high performance applications.

IV. Conclusion

We present our SRAM MSCO framework to analyze the GAA SRAM performance and show that GAA SRAM has 13% higher SNM, 5% higher I-read and 15% better write-margin than FinFET SRAM. In terms of AC performance, the GAA SRAM also exhibits 10% and 20% lower read and write delays, respectively, compared to FinFET SRAM. We also show that GAA SRAM write-margin can be improved (4%) by reducing pMOS NS width. pMOS RMG WF optimization can lead to significant improvements (15%) in GAA SNM and can be a useful approach for stability-critical applications. GAA SRAM I-read can be significantly improved (25%) by increasing the nanosheet stack count from 3 to 4 (without penalty on SNM or write-margin), beneficial for high performance applications.

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