Multi-Scale Modeling of Transistors Based on the 2D Semiconductor Bi_2O_2Se

Mohammad Rasool Davoudi*, Pedram Khakbaz*, Theresia Knobloch*, Dominic Waldhoer*,
Changze Liu†, Aftab Nazir,† Yichi Zhang‡, Hailin Peng‡, and Tibor Grasser*
* Institute for Microelectronics, Technische Universitat Wien, Vienna, Austria
† Huawei Technologies R&D Belgium NV, Leuven, Belgium
‡ Peking University, Beijing, China
Email: davoudi | grasser@iue.tuwien.ac.at

***Abstract*—The growing interest in 2D materials for novel electronic devices has sparked extensive research into their properties. These atomically thin materials, such as graphene and transition metal dichalcogenides, possess unique properties that make them highly appealing for various applications. In this context, our study focuses on investigating the material and non-ideal properties of the 2D layered semiconductor bismuth oxyselenide (Bi_2O_2Se) and its native oxide Bi_2SeO_5. Through a multi-scale simulation approach combining density functional theory (DFT) with technology computer-aided design (TCAD), we extract critical parameters and simulate transfer characteristics, demonstrating the potential of these materials in nanoelectronics.**

***Index Terms*—Bi_2O_2Se, Bi_2SeO_5, defects, 2D materials, reliability, TCAD, DFT, FET, MOSFET**

I. Introduction

As it offers higher integration density and lower energy consumption, scaling down electronic devices has always been desirable. Field-effect transistors (FETs), which are at the heart of modern electronics, likewise benefit from lower switching times [1]. In recent years, there has been a growing interest in finding new materials that can serve as alternatives to silicon technology [2] due to the challenges faced in scaling down silicon-based transistors into the nanometer regime, such as severe loss of mobility or short channel effects [3]. Utilizing materials with high dielectric constants as gate insulators helps to scale the insulator down to a smaller equivalent oxide thickness, resulting in reduced leakage current [4,5] and suppressed short-channel effects due to the reduced transistor characteristic length [6]."

Among the aforementioned materials, a promising group of candidates are 2D materials, which exhibit atomically thin layers and promising behavior [6]. However, exploiting the full potential of 2D materials is challenging due to obstacles such as the lack of high dielectric constant oxides with perfectly flat and dangling-bond-free interfaces [7]. Contrary to other 2D semiconductors with a native oxide (such as $HfSe_2$ with HfO_2), the atomically thin layered gate dielectric of Bi_2SeO_5 can be fabricated through layer-by-layer oxidization of a high-mobility two-dimensional semiconductor, Bi_2O_2Se [8,9]. Moreover, while $HfSe_2$ is not stable in air [10], Bi_2O_2Se is a chemically stable compound. Recently it has been demonstrated that slabs of Bi_2O_2Se can be grown vertically and oxidized from the side for the fabrication of high-quality finFETs based on layered materials [11]. Given their promising intrinsic properties, a thorough understanding of the non-idealities of the Bi_2O_2Se/Bi_2SeO_5 material system becomes essential. Since these materials are new and have not yet been studied in detail, many of their parameters are currently unknown.

Here, we investigate non-idealities in planar layered Bi_2O_2Se FETs such as interface traps and Schottky contact barriers by employing a multi-scale modeling approach. We conducted a combination of DFT and TCAD simulations, where some experimentally not easily accessible quantities like the effective masses and band gaps are calculated within DFT and then used in our TCAD model to create a physically meaningful device description which can be later employed to study the additional impacts of defects (causing a hysteresis, BTI, and RTN) to extract defect parameters based on experimental data [12].

II. Methodology

In this investigation focused on Bi_2O_2Se and its native oxide, we performed DFT simulations with the Quantum ESPRESSO suite to analyze their structural, optical, and electronic properties. The crystal structures of Bi_2O_2Se and Bi_2SeO_5 were optimized using plane-wave basis sets within the Mega Generalized Gradient Approximation (MGGA) framework, employing the PBE functional for Bi, Se, and O atoms. To overcome the tendency of conventional GGA functionals to underestimate the band

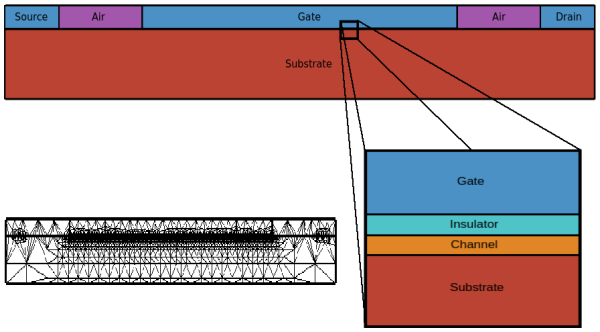


Figure 1: The geometry of the device designed in TCAD and the triangular grids utilized for the simulations are shown, with a focus on the channel and the insulator.

gap, we employed Hybrid GGA functionals to achieve a more accurate assessment of the electronic structure of the investigated materials.

Device simulations were performed by employing the drift-diffusion transport model [13] that is proven to be computationally efficient [14]. That approach is justified since the charge carriers transport in the available micrometer-scaled prototype devices with a large number of potential scattering centers in the channel is dominated by scattering at ambient temperatures, which leads to diffusive transport. We conducted our simulations using Minimos-NT [15,16].

The device geometry and mesh used in our simulations is shown in Fig. 1. The device under investigation in this study was a top-gated field effect transistor that has the following dimensions: width $(W) = 7.9\,\mu\text{m}$, length $(L) = 6\,\mu\text{m}$, source-drain spacing $(L_{\text{S-D}}) = 4.9\,\mu\text{m}$, gate length $(L_{\text{G}}) = 3.2\,\mu\text{m}$. The channel of the device consists of Bi_2O_2Se and has a thickness of $5.6\,\text{nm}$, while β-Bi_2SeO_5 with the same thickness was grown as the gate insulator. In this context, β-Bi_2SeO_5 refers to the low-temperature oxide phase of Bi_2SeO_5 which was grown in a UV-assisted intercalative oxidation step, described in [8]. Furthermore, the device was fabricated on a $SrTiO_3$ (STO) substrate with a thickness of $500\,\mu\text{m}$.

Simulations were performed at room temperature ($25\,^\circ\text{C}$) and two higher temperatures ($90\,^\circ\text{C}$ and $120\,^\circ\text{C}$) to ensure obtaining the best agreement with the experimental measurements. We used the L-BFGS algorithm [17] to extract the unknown parameters such as the electron mobility in the channel, the Schottky barrier height at source and drain contacts, and the interface trap energy levels. The Shockley-Read-Hall model [18] was used for modeling the interface traps.

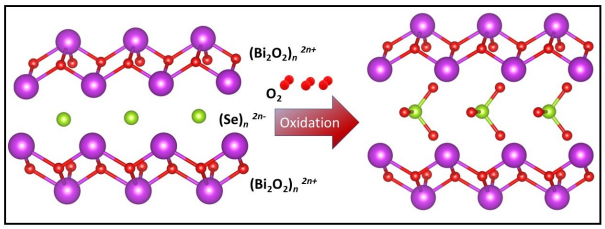


Figure 2: Transition between the crystal structure of Bi_2O_2Se and β-Bi_2SeO_5. Bi_2O_2Se can be oxidized layer-by-layer to form a crystalline Bi_2SeO_5 oxide.

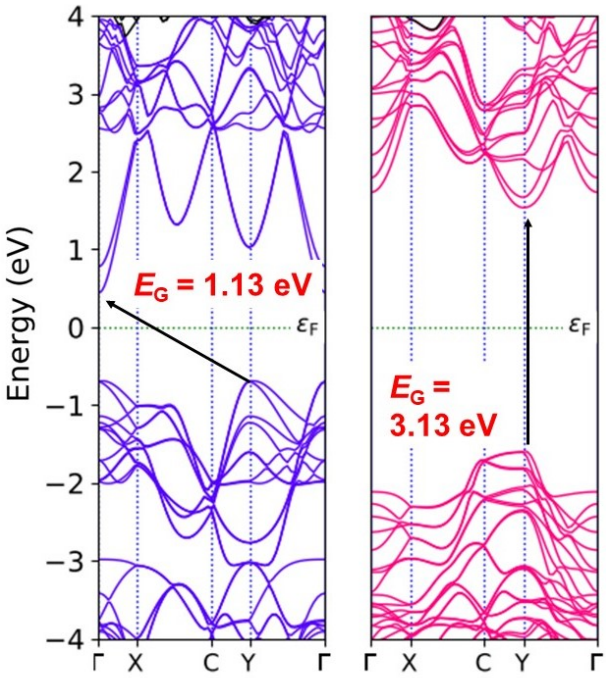
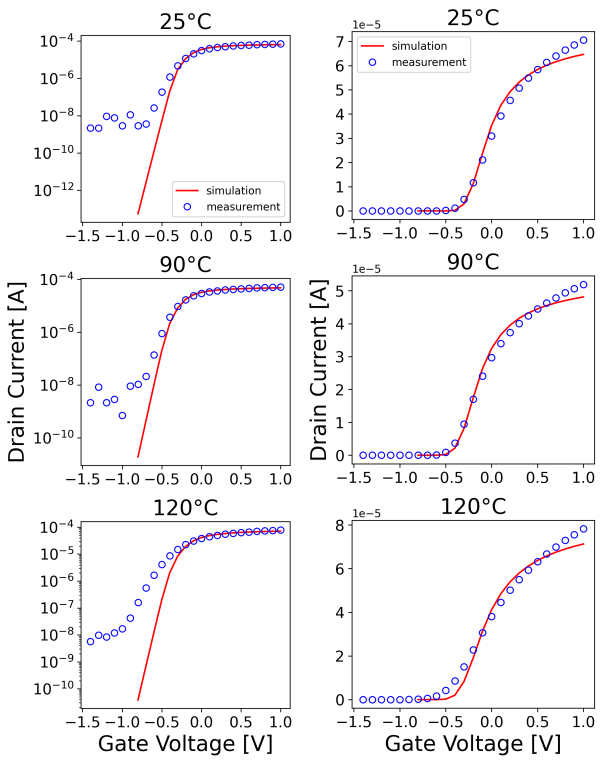


Figure 3: Electronic band structure of Bi_2O_2Se and Bi_2SeO_5. Bi_2O_2Se has an indirect band gap, while it is direct for β-Bi_2SeO_5.

III. Result and Conclusion

Table I compares the calculated structural parameters of Bi_2O_2Se and β-Bi_2SeO_5 using DFT with the experimental values [8,9,11]. As shown, the calculated lattice parameters and the distance between two nearby Se atoms are consistent with the experimental data. Fig. 2 displays the resulting crystal structures of Bi_2O_2Se and Bi_2SeO_5. Note that each layer (Se-Se) of Bi_2O_2Se occupies $6.2\,\text{Å}$ of space, but the thickness of a single layer after oxidation is about $7.4\,\text{Å}$. Fig. 3 shows the electronic band structure of the materials, as obtained from DFT calculations. It can be observed that the semiconductor has an indirect band gap, while the ox-



(a) (b)

Figure 4: Transfer characteristics at three different temperatures (25°C, 90°C, 120°C) on logarithmic (a) and linear (b) scales. The red lines represent simulated values and the blue circles represent the experimental data. The difference in SS at 120°C seems to exist because of additional interface trap formation as the device apparently degraded during heating.

ide has a direct band gap. We calculated permittivity, band gap, and effective mass of electrons for Bi_2O_2Se and β-Bi_2SeO_5, these extracted material parameters are summarized in Table II. We obtained $35.3\epsilon_0$ for the permittivity of β-Bi_2SeO_5 which confirms Bi_2SeO_5 as a high-κ material. Note that even though the band gap of Bi_2SeO_5 is relatively small, extremely low gate leakage currents have been demonstrated experimentally [8,11] as the high permittivity (>30) allows for physically thick insulator layers.

The transfer characteristics for the device obtained from TCAD simulations at different temperatures (25 °C, 90 °C and 120 °C) are shown in Fig. 4. We can see that the on-state currents exhibit good agreement with the experimental data at all three temperatures. The sub-threshold slope also agrees well with the experiments, more specifically, the room temperature (the difference in slopes ΔSS = 39 mV/dec) and 90 °C (ΔSS = 32 mV/dec) curves agree with the experiments well, and

	Experiment	DFT
Bi_2O_2Se ΔZ(Se-Se) [Å]	6.1	6.2
Bi_2SeO_5 ΔZ(Se-Se) [Å]	7.8	7.4
Bi_2SeO_5 Lattice parameters [Å]	$a = 3.90$,	$a = 3.81$,
		$b = 4.06$,
	$c = 15.50$	$c = 14.77$

Table I: Comparing essential structural parameters from experimental measurements and DFT for two materials used in our device: Bi_2O_2Se and its native oxide β-Bi_2SeO_5.

	Bi_2O_2Se	β-Bi_2SeO_5
Permittivity [ϵ_0]	99.48	35.3
Band gap [eV]	1.13	3.13
Effective mass [m_0]	0.08	0.2

Table II: Calculated material parameters using DFT that has been used to perform TCAD simulations for Bi_2O_2Se and its two native oxides α-Bi_2SeO_5 and β-Bi_2SeO_5. The values for permittivity are calculated along the out of plane direction while the effective masses are calculated along the in plane direction

in the 120 °C curve the sub-threshold slope is sloppier than expected (ΔSS = 92 mV/dec.), it seems that the creation of additional interface traps is responsible for the difference. The threshold voltages at all three temperatures also show good agreement. Having achieved a high degree of accuracy in our model and confirmed its validity, we were able to extract the mobility and non-ideality parameters, which are summarized in Table III. As illustrated, the mobility of the material is consistent with experimentally reported values and the agreement in the sub-threshold slope confirms the extracted value for Schottky Barrier Height. Fig. 5 demonstrates how the transfer characteristics of the devices at 25 °C vary with mobility among the calculated range. The experimental curve is sandwiched between the curves corresponding to the assumed maximum and minimum values of the mobility.

	TCAD	Experimental
Electron mobility μ [cm^2/Vs]	112	270 [11]
Schottky barrier height for electrons [eV]	0.09	–
Interface charge traps level E_t [eV]	1.25	–

Table III: Optimized TCAD parameters obtained after parameter fitting. The interface trap levels are referenced to the semiconductor valence band edge. Except for the mobility, other parameters are investigated for the first time and no experimental values are available.

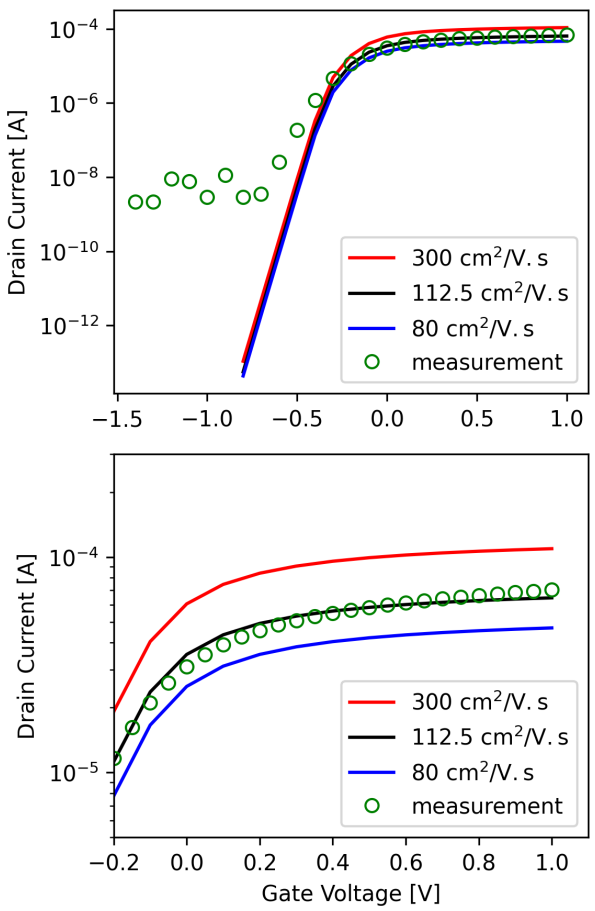


Figure 5: Impact of mobility on the full transfer curve (top) and on the threshold and on-state area (bottom). The experimental curve is sandwiched between the curves corresponding to the maximum and minimum of the extracted mobility.

In conclusion, our model has demonstrated its capability to accurately capture the ID-VG characteristics, as evidenced by the good agreement observed between the TCAD simulation results and the experimental data. This agreement holds true for both logarithmic and linear scales, highlighting the accuracy of our model in reproducing the electrostatics and behavior of the devices under investigation. The extracted material parameters obtained from our model provide valuable insights for further analysis and design of devices using these promising new materials.

References

[1] M. Neisser, "International roadmap for devices and systems lithography roadmap," *Journal of Micro/Nanopatterning, Materials, and Metrology*, vol. 20, no. 4, p. 044601, 2021.

[2] S. B. Desai, S. R. Madhvapathy, A. B. Sachid, J. P. Llinas, Q. Wang, G. H. Ahn, G. Pitner, M. J. Kim, J. Bokor, C. Hu, *et al.*, "MoS_2 transistors with 1-nanometer gate lengths," *Science*, vol. 354, no. 6308, pp. 99–102, 2016.

[3] C. Colinge and J. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors," *Nature*, vol. 479, pp. 310–6, 11 2011.

[4] R. Chau, J. Brask, S. Datta, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, B. Jin, M. Metz, A. Majumdar, and M. Radosavljevic, "Application of high-$\varkappa$ gate dielectrics and metal gate electrodes to enable silicon and non-silicon logic nanotechnology," *Microelectronic Engineering*, vol. 80, pp. 1–6, 2005. 14th biennial Conference on Insulating Films on Semiconductors.

[5] T. Knobloch, Y. Y. Illarionov, F. Ducry, C. Schleich, S. Wachter, K. Watanabe, T. Taniguchi, T. Mueller, M. Waltl, M. Lanza, M. I. Vexler, M. Luisier, and T. Grasser, "The performance limits of hexagonal boron nitride as an insulator for scaled CMOS devices based on two-dimensional materials," *Nature Electronics*, vol. 4, no. 2, pp. 98–108, 2021.

[6] Y. Liu, X. Duan, H.-J. Shin, S. Park, Y. Huang, and X. Duan, "Promises and prospects of two-dimensional transistors," *Nature*, vol. 591, no. 7848, pp. 43–53, 2021.

[7] H. Zhu, X. Qin, L. Cheng, A. Azcatl, J. Kim, and R. M. Wallace, "Remote plasma oxidation and atomic layer etching of MoS_2," *ACS Applied Materials & Interfaces*, vol. 8, no. 29, pp. 19119–19126, 2016.

[8] Y. Zhang, J. Yu, R. Zhu, M. Wang, C. Tan, T. Tu, X. Zhou, C. Zhang, M. Yu, X. Gao, Y. Wang, H. Liu, P. Gao, K. Lai, and H. Peng, "A single-crystalline native dielectric for two-dimensional semiconductors with an equivalent oxide thickness below 0.5 nm," *Nature Electronics*, vol. 5, pp. 1–7, 09 2022.

[9] T. Li, T. Tu, Y. Sun, H. Fu, J. Yu, L. Xing, Z. Wang, H. Wang, R. Jia, J. Wu, *et al.*, "A native oxide high-κ gate dielectric for two-dimensional electronics," *Nature Electronics*, vol. 3, no. 8, pp. 473–478, 2020.

[10] M. J. Mleczko, C. Zhang, H. R. Lee, H. H. Kuo, B. Magyari-Köpe, R. G. Moore, Z. X. Shen, I. R. Fisher, Y. Nishi, and E. Pop, "HfSe2 and ZrSe2: Two-Dimensional Semiconductors with Native High-κ Oxides," *Science Advances*, vol. 3, no. 8, 2017.

[11] C. Tan, M. Yu, J. Tang, X. Gao, Y. Yin, Z. Yichi, J. Wang, X. Gao, C. Zhang, X. Zhou, L. Zheng, H. Liu, K. Jiang, F. Ding, and H. Peng, "2D Fin field-effect transistors integrated with epitaxial high-k gate oxide," *Nature*, vol. 616, pp. 1–7, 03 2023.

[12] D. Waldhoer, C. Schleich, J. Michl, A. Grill, D. Claes, A. Karl, T. Knobloch, G. Rzepa, J. Franco, B. Kaczer, M. Waltl, and T. Grasser, "Comphy v3.0—a compact-physics framework for modeling charge trapping related reliability phenomena in MOS devices," *Microelectronics Reliability*, vol. 146, p. 115004, jul 2023.

[13] W. Van Roosbroeck, "Theory of the flow of electrons and holes in germanium and other semiconductors," *The Bell System Technical Journal*, vol. 29, no. 4, pp. 560–607, 1950.

[14] M. Lundstrom, "Drift-diffusion and computational electronics-still going strong after 40 years!," in *2015 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, pp. 1–3, IEEE, 2015.

[15] IμE, *MINIMOS-NT user's Guide*. Institute für Microelektronik, Technische Universität Wien, Austria, 1998-2008. http://www.iue.tuwien.ac.at/software/minimos-nt.

[16] Global TCAD Solutions, Vienna, Austria, *Minimos-NT Manual*, 2018.

[17] D. C. Liu and J. Nocedal, "On the limited memory BFGS method for large scale optimization.," *Math. Program.*, vol. 45, no. 1-3, pp. 503–528, 1989.

[18] W. Shockley and W. T. Read, "Statistics of the recombinations of holes and electrons," *Phys. Rev.*, vol. 87, pp. 835–842, Sep 1952.