Self-Consistent Monte Carlo Device Simulation of Capture-Excitation Processes of Carriers

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***Abstract*—The capture-excitation processes of carriers are implemented in self-consistent Monte Carlo device simulations. The carrier transfer characteristics in n-type resistors and CMOS image sensors (CISs) are simulated. The long tail observed in experiments in time evolutions of the number of residual carriers has been successfully reproduced.**

***Index Terms*—transport, random discrete dopant, Monte-Carlo device simulation, carrier capture excitation**

I. Introduction

The time scale of carrier transfer in nanoscale semiconductor devices predicted by conventional TCAD device simulators differs significantly from actual measurements. This is due to the fact that the discreteness of impurity and the carrier capture via trap states are not accurately introduced, even though they are prominent in nanoscale devices. We would like to stress that taking into account the localized (discretized) nature of trapped charges is mandatory when the carrier capture processes are introduced into the MC simulations. In the present study, we introduced those effects into the MC simulation for the first time and succeeded to predict a long tail of time evolution of the residual carriers which is experimentally observed.

II. Simulation model and methodology

Figure 1 shows the device structure employed in MC simulations; an n-type resistor with $100\,\mathrm{nm}$ along the x-direction and the cross-section of $50\,\mathrm{nm} \times 50\,\mathrm{nm}$. The donor impurity density with a trap level of $0.05\,\mathrm{eV}$ is uniform at $10^{18}\,\mathrm{cm}^{-3}$ and discretized impurities are configured consistently with the Poisson distribution in the substrate. Two deep neutral trap levels, $0.25\,\mathrm{eV}$ and $0.5\,\mathrm{eV}$, are also assumed in the whole region with the concentration of $0.5 \times 10^{17}\,\mathrm{cm}^{-3}$. Donor impurities and deep neutral traps are treated as carrier capture sites during the simulations, and the capture-excitation probabilities are calculated by imposing the detailed balance. When a carrier enters within $5\,\mathrm{nm}$ of the capture center, a decision is made as to whether or not the carrier is captured according to its probability. The Coulomb potential of trapped charges and ionized impurities is separated into the long- and short-range part to avoid double-counting the short-range scattering potential [1], [2]. The charge of the long-range part of impurities, $N_{long}(r)$, was introduced by the following expression

$$N_{long}(r) = \sum_{i=1}^{N_I} \frac{q_c^2}{4\pi} \frac{e^{-q_c|r-R_i|}}{|r-R_i|}. \tag{1}$$

Here, N_I is the number of discrete donor impurities, q_c is the inverse of the screening length, r is the position of mesh grid, R_i the position of discrete donor impurity. The charges with this expression are introduced into Poisson's equation and solved self-consistently with the Boltzmann transport equation. The donor impurity neutralized by carrier-trap is excluded from Eq.1, and Poisson's equation is re-solved to update the potential. On the other hand, the donor impurity that released the carrier is again introduced in Eq.1. Namely, Poisson's equation is solved each time a capture or excitation occurs. An external electric field of $1\,\mathrm{kV/cm}$ is applied in the x-direction to simulate the transfer behavior of 250 carriers initially distributed around the left electrode.

Figure 6 shows the computational model of the CMOS image sensor (CIS) employed in this study, assuming a $2\,\mathrm{um}$ long device with a cross section of $1\,\mathrm{um} \times 1\,\mathrm{um}$. A cross-sectional view of the impurity distribution at $y = 0.5\,\mathrm{um}$ is shown below in Fig. 6. The n-type region is surrounded by a p-type region. The n-type region is graded in the x direction so that the electric field gradient is in the direction of the drain electrode. The discretization of impurities is performed only in n-type region. As with n-type resistor, two deep neutral trap levels, $0.25\,\mathrm{eV}$ and $0.5\,\mathrm{eV}$, are also assumed in the whole region with the concentration of $0.5 \times 10^{17}\,\mathrm{cm}^{-3}$. Then, a voltage was applied to the gate electrodes to simulate the transfer behavior of 200 carriers initially distributed in the middle of the device until they reach the drain electrode.

III. Results and discussion

A. N-type resistor

Figure 2 shows electron mobility as a function of impurity density. Considering the long-range part of discrete impurities, mobility decreases with increasing impurity density due to potential fluctuations induced by localized impurities as shown by blue line. Figure 3 shows the potential fluctuation with the donor impurity density of $1 \times 10^{17}\,\mathrm{cm}^{-3}$ (a)(b) and of $1 \times 10^{18}\,\mathrm{cm}^{-3}$ (c)(d). It can be seen that the potential fluctuation increases as the density increases, as $20\,\mathrm{mV}$ at $1 \times 10^{17}\,\mathrm{cm}^{-3}$ becomes $30\,\mathrm{mV}$ at $1 \times 10^{18}\,\mathrm{cm}^{-3}$. When we additionally introduce scattering of the short-range part, the mobility decreases further as shown by red line in Fig. 2, approaching the measurements indicated by the black dots. Taking into account the potential fluctuations associated with the long-range part of the Coulomb potential that is usually ignored in the traditional treatments, we could correctly reproduce the measured electron mobility indicated by the black dots. Taking into account the long- and short-range part of the Coulomb potential separately, we could correctly reproduce the measured electron mobility.

Figure 4 shows a time evolution of the number of carriers that remained in the substrate. The black line results from the jellium impurities, where discreteness and carrier capture are ignored. The blue and red lines show the results when only traps by the discrete donor impurities and those by all traps, respectively, are taken into account. The number in parentheses indicates the time required until the number of carriers reduces to one-tenth ($250 \rightarrow 25$). We found three orders of magnitude increase in time compared to the jellium impurity case by including the capture-excitation processes through all traps and the long-time carrier capture phenomenon observed in experiments was reproduced.

Figure 5 shows the potential and carrier positions (white dots) at $y = 0.25\,\mathrm{um}$ for (a) $0\,\mathrm{s}$, (b) $4\,\mathrm{ps}$, (c) $10\,\mathrm{ps}$, (d) $200\,\mathrm{ps}$, when all traps are considerd (red line in Fig. 4). The potential is greatly lowered due to captured carriers at $10\,\mathrm{ps}$, and most of the captured carriers are then released from the shallow traps, yet some are still captured by the deep traps even at $200\,\mathrm{ps}$. These results indicate that the potential variation via capture-excitation processes of carriers is crucial in the analyses of the transfer characteristics in nanoscale devices.

B. CMOS image sensor

The time evolution of the number of remaining carriers in the CIS is shown in Fig. 7. The gray line shows the results of the deep trap distribution with 5000 different conditions, and the black line shows the average of them. As the $500\,\mathrm{ns}$ long tail is observed, the transfer delay due to the carrier capture effect can be also reproduced in CISs. The curve seems to be stair-stepped because of the discrete trap levels at 0.05, 0.25 and $0.5\,\mathrm{eV}$. It also can be seen that the variation of the deep trap distribution (width of gray lines) is increasing in the $1 - 100\,\mathrm{ns}$ time range. This time range corresponds to an excitation probability of $1/78\,\mathrm{ns}$ with deep traps of $0.25\,\mathrm{eV}$, indicating that deep traps have a significant impact on the carrier transfer of the nanosecond time scale.

Figure 8 shows a histgram for the number of carriers reaching drain at $500\,\mathrm{ns}$ with 5000 different conditions of the deep trap distribution. The distribution of the number of carriers transferred during the gate-ON time becomes Gaussian-like, but it has a tail on the low side (arrow in Fig. 8). This tail, which can be seen in the actual measurements, appeared due to the correct introduction of carrier capture process, and is exactly a indication of the transfer delay phenomenon.

Figure 9 shows the time evolution of the number of residual carriers for two different deep trap distributions (condition-A and -B in blue and red color, respectively) with 50 different donor distributions (bright lines of each color). The dark lines represent the average of the results of 50 donor distribution for each deep trap distribution. The deep trap distribution was found to have the effect of significantly shifting the average of transfer characteristics that vary with the donor impurity distribution.

Figure 10 shows the potential at $y = 0.5\,\mathrm{um}$ and carrier positions at each time for (a) fast transfer condition (condition-A) and (b) slow transfer condition (condition-B) Black, blue and red dots represent carriers caputured in $0.05\,\mathrm{eV}$ donor traps, $0.25\,\mathrm{eV}$, and $0.5\,\mathrm{eV}$ deep traps, respectively. White dots represent free carriers not captured in the traps. Under both conditions, most carriers are transferred to the top surface of the substrate near the gate by $100\,\mathrm{ps}$ and are captured in traps near the surface. At $500\,\mathrm{ns}$, all carriers captured in the $0.05\,\mathrm{eV}$ and $0.25\,\mathrm{eV}$ traps are excited and transferred to Drain electrode, leaving only the carriers captured in the $0.5\,\mathrm{eV}$ deep traps in the substrate. More carriers are captured in the $0.5\,\mathrm{eV}$ deep trap in condition-B (slow transfer) than in condition-A (fast transfer), indicating that the number of traps near the gate have a significant impact on transfer characteristics. From this MC simulation analysis, it was found that deep level trapping grately affects the nanosecond-scale transfer in CISs, indicating that the carrier capture model is effective for analyzing transfer delays.

IV. Conclusion

We have implemented the capture-excitation processes of carriers in self-consistent MC device simulations and simulated carrier transfer characteristics in n-type resistors and CISs. The constructed model was validated by reproducing the impurity density dependence of electron mobility and the transfer delay due to the carrier capture in n-type resistors. We have applied the model to CIS and analyzed the effect of deep trap distribution variation, and found that the number of traps near the gate has a significant impact on the transfer characteristics of CIS.

References

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[2] N. Sano and T. Fukui, "Fundamental Aspects of Semiconductor Device Modeling Associated with Discrete Impurities: Monte Carlo Simulation Scheme" IEEE Trans. Electron Devices, vol. 68, p. 5394, 2021.

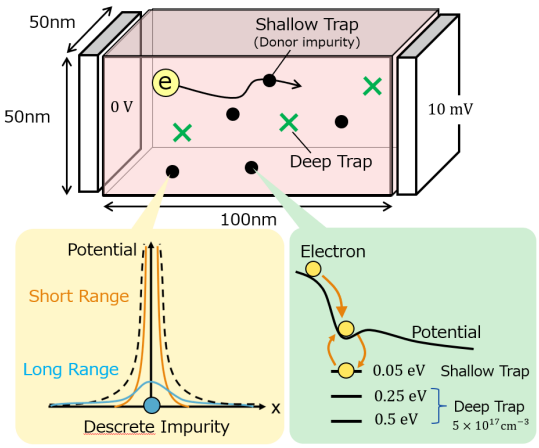

Fig. 1. Schematics of n-type resistor (top) and considierd models (bottom).

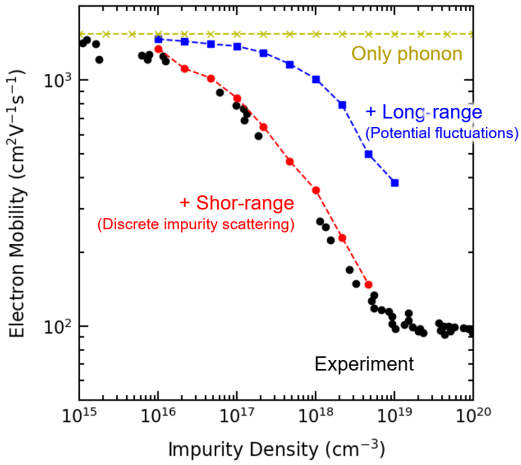

Fig. 2. Electron mobility vs. impurity density, considering only phonon scattering (yellow), long-range part of discrete impurity added (blue), and short-range part added (red). Black dots indicate experimental values.

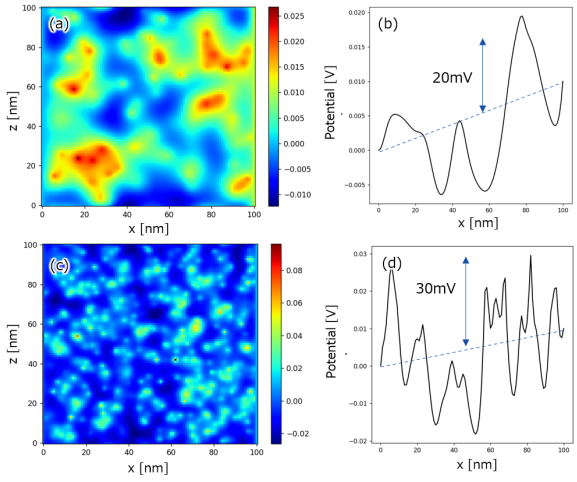

Fig. 3. Potential fluctuation with the donor impurity density of (a)(b) $1 \times 10^{17}\,\mathrm{cm}^{-3}$ and of (c)(d) $1 \times 10^{18}\,\mathrm{cm}^{-3}$.

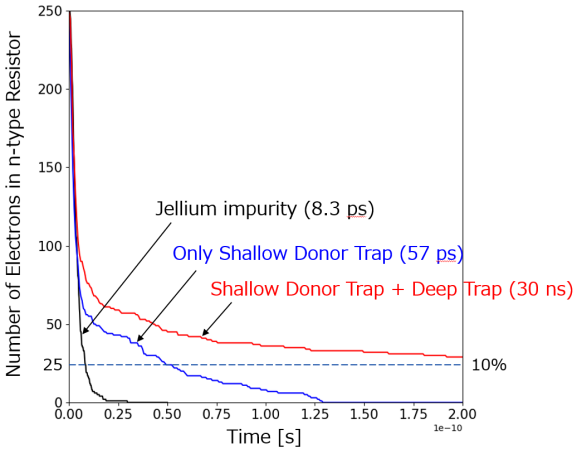

Fig. 4. Time evolution of the number of remaining electrons in n-type resistor for jellium impurities without charge capture (black line), for only discrete donor traps (blue line), and for all traps including deep neutral traps (red line).

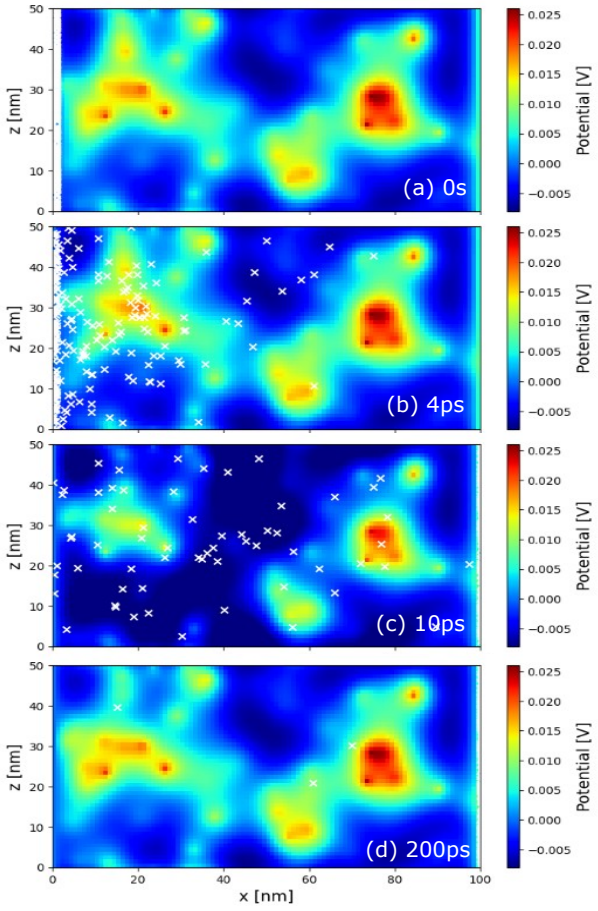

Fig. 5. Color map of potential in $y = 0.25\,\mathrm{um}$ plane and carrier positions (white dots) at (a) 0 s, (b) 4 ps, (c) 10 ps, (d) 200 ps

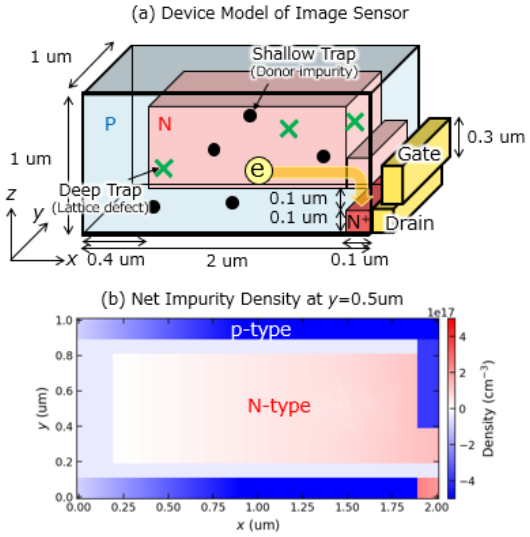

Fig. 6. Schematics of CMOS image sensor model (upper) and impurity density distribution at $y = 0.5\,\mathrm{um}$ (lower)

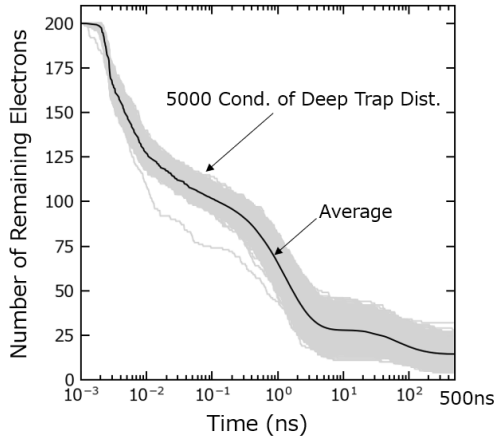

Fig. 7. Time evolution of the number of remaining electrons in CMOS image sensor. The gray line is the result of 5000 different conditions of deep trap distribution, and the black line shows their average.

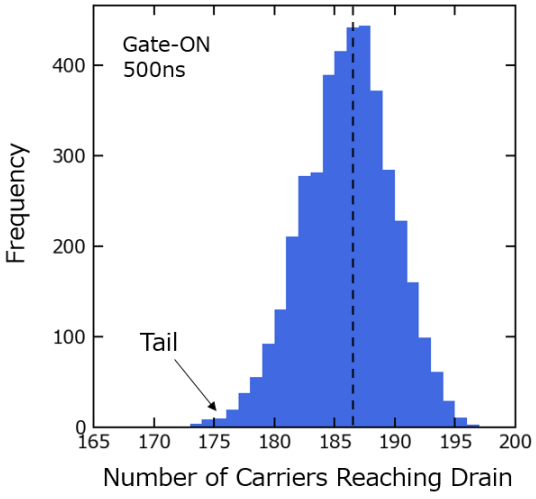

Fig. 8. Histgram for the number of carriers reaching drain at $500\,\mathrm{ns}$

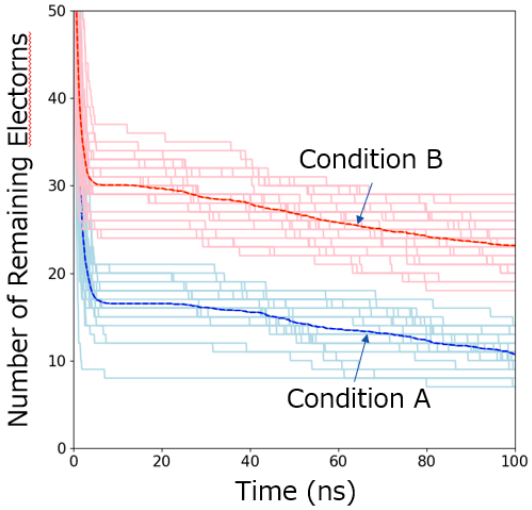

Fig. 9. Time evolution of the number of remaining electrons in CIS for two different deep trap distribution condition (blue and red lines) with 50 different donor distributions (bright lines of each color).

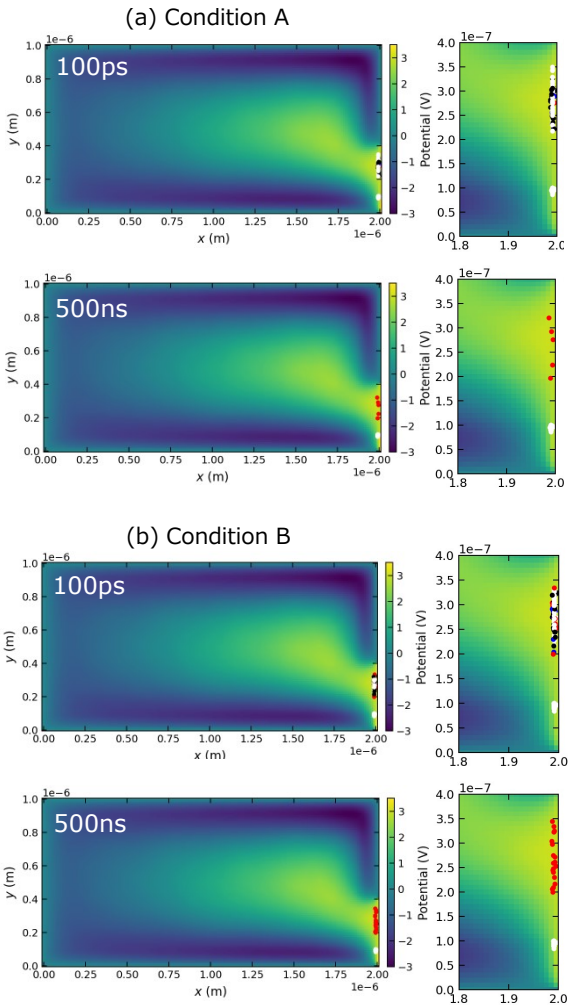

Fig. 10. Potential at $y = 0.5\,\mathrm{um}$ and carrier positions at each time for (a) fast transfer condition (condition-A) and (b) slow transfer condition (condition-B)