TCAD Modeling of Germanium Behavior During Forming Operation in Ge-Rich ePCM

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***Abstract*—Ge-rich GST alloys have been demonstrated to be an excellent material for embedded Phase Change Memories (ePCM) applications. The stoichiometric unbalance from $Ge_2Sb_2Te_5$ in favor of a higher Ge concentration led this technology to meet the high data retention standards required by the automotive industry. Ge clusters tend to segregate during the high temperature steps of fabrication creating the characteristic heterogeneous element distribution of the virgin, or out of fab, state. This characteristics introduced the need of an activation pulse, called forming, at the end of fabrication to properly set the cell properties. In this work the pristine state and the forming pulse are modeled by leveraging three dimensional TCAD simulations. A segregation function is introduced to properly distinguish the Ge agglomerates characteristics from the rest of the material. Electrical and thermal evolution of the device is reproduced with good agreement with experimental data, giving a further insight in the chalcogenide dynamics during these first crucial steps.**

***Index Terms*—ePCM, Forming, Germanium, Ge-GST, TCAD**

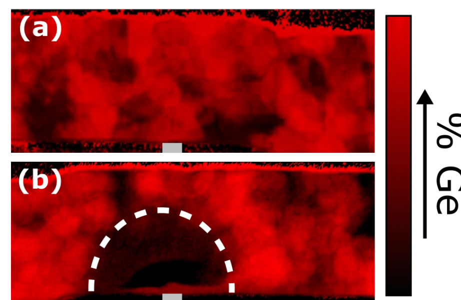

Fig. 1. Electron Energy Loss Spectroscopy (EELS) images representing the Ge concentration inside a Ge-GST cell in the virgin state (a) and after the forming pulse (b). The heater contact is highlighted in gray at the bottom of each image. In (b) the formed area is outlined in white.

I. Introduction

Phase Change Memory devices have attracted interest of the scientific community for the past years thanks to their many advantageous proprieties such as scalability, integration in the Back End of the Line (BEOL), speed and low programming voltage [1]. These devices rely on the different electrical proprieties of chalcogenide materials between their amorphous and crystalline phase (with high and low resistivity respectively). The transition between these two states is achieved with the application of electrical pulses that, through joule heating, induce a change in the alloy structure [2]. Material engineering was necessary for large scale industrialization due to the lack of high temperature data retention of the well established $Ge_2Sb_2Te_5$ chalcogenide. Ge rich GST alloy (Ge-GST) was demonstrated to have a higher crystallization temperature [3] enabling data retention after multiple soldering re-flows [4] and satisfying the automotive market requirements [1]. This new composition have some unique physical and electrical characteristics due to its off-stoichiometric balance. After the fabrication process, the alloy material is poly-crystalline with segregated composition, due to its propensity to decompose [5]. In first approximation this phenomenon separates the material into Ge agglomerates and grains with a fcc-GST structure [6], [7]. The distribution of electrical resistances in this state, called virgin, has a very large spread that can range over multiple decades [8]. To initialize the cell correctly a first activation pulse, called forming, is needed before programming operations [9]. This electrical pulse, first rises the chalcogenide temperature over melting, then slowly decrease it to re-crystallize the perturbed region of the material. This step was shown to homogenize the active region composition removing Ge agglomerates present in the virgin state. In Fig. 1 Electron Energy Loss Spectroscopy (EELS) maps of the Ge content in the virgin state (a) and after the forming pulse (b) are shown. After this activation step the resistance distribution is narrowly distributed with a low median value.

This works focuses on the Ge clusters role in the electrical and physical characteristics of the device expanding what done in [8]. A 3D TCAD model based on a randomly generated segregation function accounts for the composition heterogeneity, enabling the distinction of different electrical, thermal and material proprieties for the two states. Compositional changes and physical discontinuities over the melting temperature were taken into account to fully describe the material evolution during the forming pulse. TCAD simulations, reproducing a 90nm BCD technology cell structure, are in agreement with physical and electrical data confirming the robustness of model framework purposed.

The following pages are divided as follows: Section II describes the segregation function and how the different material proprieties were included in the same framework for temperatures below melting. Section III shows how the solid to melt

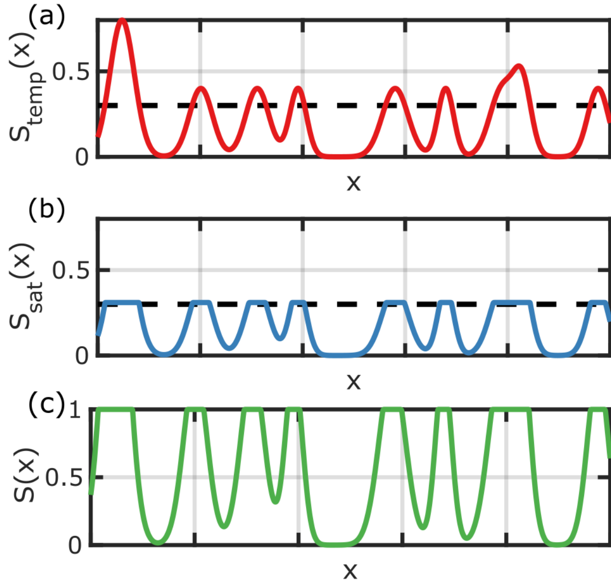

Fig. 2. Difference steps to define the segregation variable S(x) in a 1D space. In (a) a sum of random gaussian funcions is computed along the domain as in Eq. 1. The black dashed line represent the maximum permitted level. In (b) the funcion is saturated to the maximum value maintaining the continuity and derivability proprieties of the function as in Eq.2. In (c) normalization of the function range is performed to obtain a S(x) domain bounded between 0 and 1 as in Eq.3.

transition was modeled and the effects on the re-crystallized material. Finally Section IV compares the simulation results with the available data and Section V draws the conclusions.

II. Segregation Function

To account for Ge segregation in the chalcogenide, a function $S(\vec{x})$ is defined to distinguish Ge and GST volumes. This segregation function is defined in three steps. First a landscape profile is created following

$$S_{tmp}(\vec{x}) = \Sigma_i^N S_{peak} \exp(-(\vec{x} - \vec{x_i})^2/(2\vec{r_i^2})) \quad (1)$$

that is a sum of three dimensional Gaussian contributions each with random position ($\vec{x_i}$) and dimension ($\vec{r_i}$) similarly to what done in [8]. The resulting function is then distorted

$$S_{sat}(\vec{x}) = \tanh((S_{tmp}(\vec{x}) - S_{crit})/S_{trn}) \cdot S_{trn} + S_{crit} \quad (2)$$

to have a deterministic maximum value. In Eq.(2) S_{trn} and S_{crit} are the values that define respectively the transition region and the critical level chosen. Finally the range of Eq.(2) is modified as

$$S(\vec{x}) = S_{sat}(\vec{x})/(S_{crit} + S_{trn}) \quad (3)$$

to have values bounded between 0 and 1. This procedure ensure a continuous and derivable function of the three space variables x,y,z. A graphical mono-dimensional representation of these three steps is reported in Fig.2. In this scenario 0 will correspond to GST while 1 to a Ge cluster.

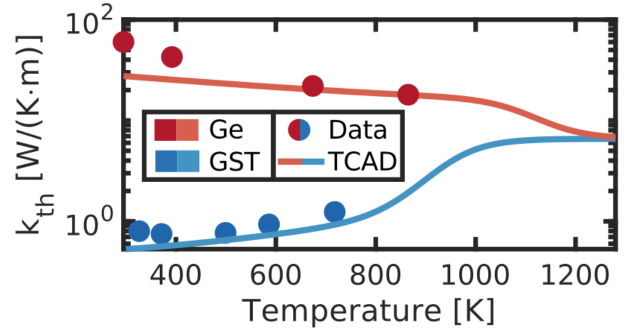

Fig. 3. Thermal conductivity dependence on temperature for GST and Ge. The two curves have a polynomial trend set to fit the experimental data [11], [12]. When the melting temperature for each material is reached both curves collapse on the same value to emulate the liquid material behavior [13] according to Eq.(11).

The function $S(\vec{x})$ is then used to calculate all the characteristic proprieties for each point in the chalcogenide material. The low temperature electrical resistivity is modeled as

$$\rho^{T_{low}}(\vec{x}, T) = \rho_0 \exp((S(\vec{x})(E_{Ge} - E_{GST}) + E_{GST})/(k_B T)) \quad (4)$$

as an Arrhenius behavior and the segregation function is used to modulate the activation energy between crystalline GST and Ge. In Eq.(4) ρ_0 is set constant through the whole material, k_B is the Boltzmann constant, E_{GST} was set to be 22meV and E_{Ge} 0.4eV (half band-gap of intrinsic Germanium). This dependence is in line with the physical interpretation of GST behaving as a p-doped semiconductor [10], [11].
The low temperature behavior of the thermal conductivity of both Ge (k_{th}^{Ge}) and GST (k_{th}^{GST}) were modeled using polynomial interpolation of literature data as shown in Fig. 3 [11], [12]. Contribution to the local conductivity of these two behaviors was then weighted through $S(\vec{x})$ according to the following formula

$$k_{th}^{T_{low}}(\vec{x}, T) = k_{th}^{Ge}(T) \cdot S(\vec{x}) + k_{th}^{GST}(T)(1 - S(\vec{x})) \quad (5)$$

Finally, also the melting temperature T_{melt} is modulated by $S(x)$, similarly to what done in Eq.(5), to account the difference between the different compositions according to

$$T_{melt}(\vec{x}) = T_{melt}^{Ge} \cdot S(\vec{x}) + T_{melt}^{GST}(1 - S(\vec{x})) \quad (6)$$

Where T_{melt}^{Ge} was set to be 1100K and T_{melt}^{GST} 950K. These values are close to the one reported in litterature in [11], [12] and were tuned to remove the Ge clusters from the active region.

III. Forming Pulse

As shown in Fig.1 the forming process induces a compositional redistribution inside the chalcogenide. This is caused by high temperatures reached during the activation pulse that melt the material defining the active region of the cell [9]. To simulate the solid to liquid transition a quasi-stationary study was computed ramping up the electrical stimulus until the desired current level was reached. As the current in the cell rises so does the local temperature of the chalcogenide due to

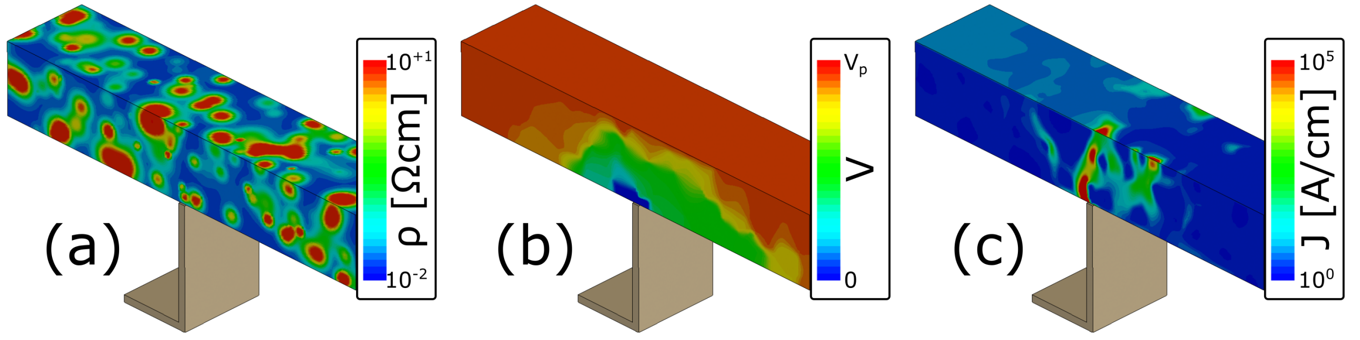

Fig. 4. 3D profiles extracted during the read phase of a cell in the virgin state. (a) shows the resistivity in the chalcogenide material, (b) the voltage distribution, (c) the absolute current density profile. In a) the color follow a logarithmic scale. The heater contact of the active cell is shown in light brown.

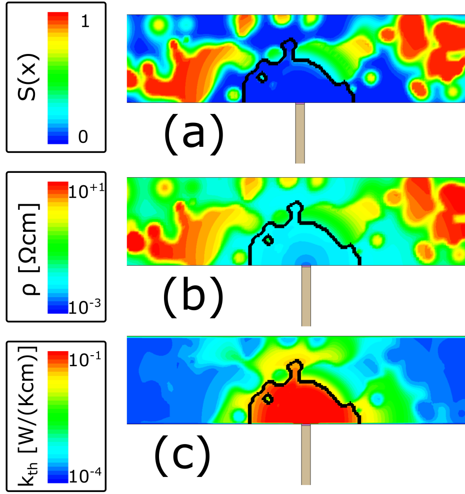

Fig. 5. 2D section of a simulated cell while a high current impulse is applied. (a) shows the segregation variable, (b) the resistivity and (c) the thermal conductance of the material. The black line delimits the interface between solid and liquid phase. Modulation with temperature of the electrical and thermal proprieties of the material can be noticed in graphs (b) and (c) as described in Eq(10-11).

Joule heating generated either in the phase change material, or in the heater structure [1]. At every simulation step, in each point of the alloy domain, the following inverse sigmoid function is calculated

$$\Omega(\vec{x}, T) = 1 - 1/(1 + \exp(-(T - T_{melt}(\vec{x}))/T_0)) \quad (7)$$

where T is the temperature in the point considered, $T_{melt}(\vec{x})$ is the melting point as calculated in Eq.6, and T_0 defines a transition region. This function is then used to update the value of the segregation function $S(\vec{x})$ as

$$S(\vec{x}, T) = S(\vec{x}) \cdot \Omega(\vec{x}, T) \quad (8)$$

For every simulation step the melting temperature landscape is updated, according to the newly calculated segregation function, following Eq.(6). In this way, while increasing the current during the quasi-stationary study, if the alloy temperature rise high enough the local peaks of $S(x)$ are lowered. This recursive framework reproduces the progressive evolution of the material allowing dissolution of the Ge grains inside the active volume.

To properly account for the discontinuity between solid and liquid phase occurring around melting, the following function, derived from Eq.(7), is introduced

$$\xi(\vec{x}, T) = 1 - \Omega(\vec{x}, T) \quad (9)$$

Eq.(9) is used to modulate the low temperature thermal and electrical behaviors of Eq.(4-5) around and over T_{melt} as in

$$\rho(\vec{x}, T) = \rho^{T_{low}}(\vec{x}, T) \cdot (1 - \xi(T)) + \rho^{melt}(T)\xi(\vec{x}, T) \quad (10)$$

$$k_{th}(\vec{x}, T) = k_{th}^{T_{low}}(\vec{x}, T) \cdot (1 - \xi(T)) + k_{th}^{melt}(T)\xi(\vec{x}, T) \quad (11)$$

The use of $\xi(\vec{x}, T)$, in Eq.(10-11), enable an increase of both conductivities around the melting point [13] allowing to describe correctly the material characteristics. Fig.3 shows this transition at high temperatures around the melting point of each material.

IV. Implementation and Results

To fully track the cell evolution, the simulation was divided in three successive steps.

First, after the definition of a unique random $S(x)$ profile, the application of a low voltage pulse (0.4V) is simulated. By doing so the resistance of the virgin state can be extracted. Fig. 4 shows different 3D cell profiles calculated during this initial step. In particular Fig. 4(a) shows the local resistivity as described by Eq.(4), Fig. 4(b) is the voltage distribution and Fig. 4(c) the current density. This last two profiles have the same characteristics, of heterogeneity and percolation respectively, as described in [8]. Due to the low voltage stimulus applied during this step the temperature was considered constant though the whole cell and the thermal effects were neglected.

The second step is the application of the forming pulse. During this step a high current pulse is applied to the previously simulated landscape. To properly reproduce the thermal profile a large portion of the overall device structure was considered covering in total three different bit-lines with three cells each. The reference device used to simulate the virgin state was

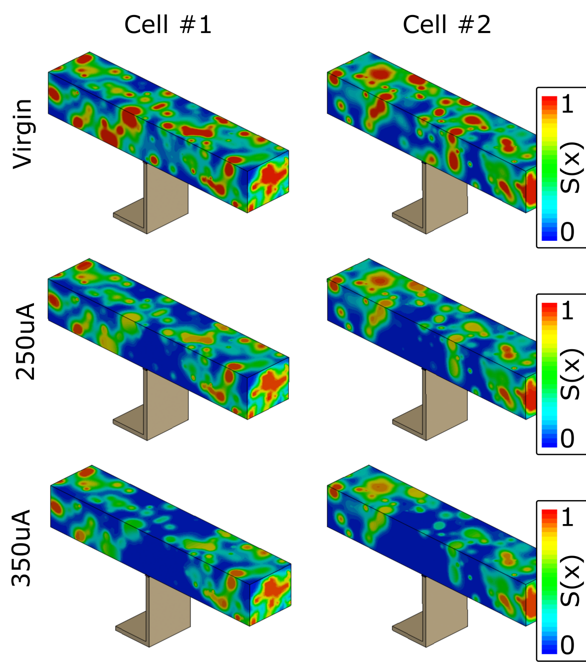

Fig. 6. Segregation variable profile of two cells in different forming conditions during reading operation. The first row shows the virgin profile. Second and third rows are the same cell formed with two increasing forming current peaks. Ge agglomerates dissolve in a larger volume for higher current pulses.

chosen in the center of the domain to avoid the influence of boundary conditions. During the application of the forming pulse the temperature rises and changes the segregation profile according to what described in Section III. Fig. 5 shows 2D cuts of a cell during this step. The black line in the images defines the liquid to solid interface. In Fig. 5(a) the $S(x)$ profile is shown. A depletion of peaks in the area around the heater can be noticed as well a gradual decrease of the segregation function in some grains. Fig. 5(b) and (c) show the electrical and thermal characteristics of the section. The influence of $S(x)$ peaks can be noticed in both cases as a lower electrical or higher thermal conductivity. In these two images the temperature's influence and the discontinuity at melting can be noticed in the area toward the heater contact where the melting values introduced in Eq.(10-11) can be noticed.
Finally the modified segregation profile is then used to read the formed resistance similarly to what done in the first step. Multiple increasing current levels are simulated for the same landscape profile to collect the evolution with higher currents. Fig. 6 shows the the 3D segregation profile for the same cell after different current peaks were applied. The Ge grains gradually dissolve from the melted region and around the heater area as shown in Fig. 1 and in [9].
A set of 25 different landscape profiles were simulated, each one for increasing current levels, following the procedure reported. The resulting resistance distributions are compared with data in Fig. 7. Both median and spread of the curves decrease with increasing forming current level coherently with the experimental data and past literature [8], [9].

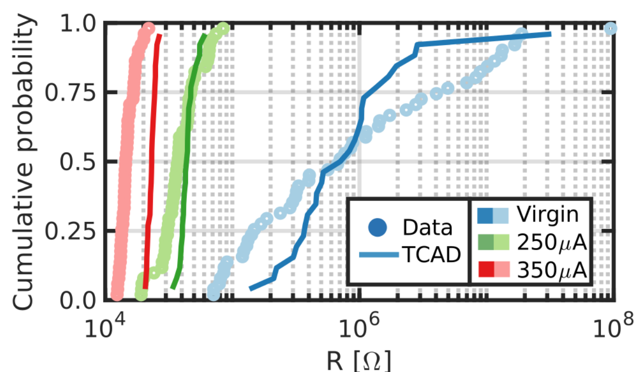

Fig. 7. Resistance distribution for different levels of forming. Spread and median of the distributions lowers with increasing forming current. Data are collected in 90nm BCD technology [4] over a sample of 400 cells for each distribution. TCAD simulations are performed over 25 different simulated landscapes.

V. Conclusions

Ge segregation and material heterogeneity are key characteristics playing an important role in the operation of Ge-rich GST PCM cells. The presented model enables to properly reproduce and predict the electrical and physical behavior of both virgin and formed cells. This framework can provide insight on cell operations and be the starting point for further studies regarding material redistribution in PCM cells.

References

[1] F. Arnaud, P. Ferreira *et al.*, in *2020 IEEE International Electron Devices Meeting (IEDM)*. San Francisco, CA, USA: IEEE, Dec. 2020, pp. 24.2.1–24.2.4. doi: 10.1109/IEDM13553.2020.9371934
[2] A. Antolini, E. Franchi Scarselli *et al.*, *Materials*, vol. 14, no. 7, 2021. doi: 10.3390/ma14071624
[3] P. Zuliani, E. Varesi *et al.*, *IEEE Transactions on Electron Devices*, vol. 60, no. 12, pp. 4020–4026, Dec. 2013. doi: 10.1109/TED.2013.2285403
[4] G. Croce, in *2022 IEEE International Memory Workshop (IMW)*, 2022, pp. 1–4. doi: 10.1109/IMW52921.2022.9779244
[5] D. T. Yimam, A. J. T. Van Der Ree *et al.*, *Nanomaterials*, vol. 12, no. 10, 2022. doi: 10.3390/nano12101717
[6] E. Petroni, A. Serafini *et al.*, *Frontiers in Physics*, vol. 10, p. 862954, 04 2022. doi: 10.3389/fphy.2022.862954
[7] E. Rahier, S. Ran *et al.*, *ACS Applied Electronic Materials*, vol. 4, no. 6, pp. 2682–2688, 2022. doi: 10.1021/acsaelm.2c00038
[8] M. Baldo, O. Melnic *et al.*, in *2020 IEEE International Electron Devices Meeting (IEDM)*. San Francisco, CA, USA: IEEE, Dec. 2020, pp. 13.3.1–13.3.4. doi: 10.1109/IEDM13553.2020.9372089
[9] E. Palumbo, P. Zuliani, M. Borghi, and R. Annunziata, *Solid-State Electronics*, vol. 133, pp. 38–44, Jul. 2017. doi: 10.1016/j.sse.2017.03.016
[10] D. Ielmini, D. Sharma, S. Lavizzari, and A. L. Lacaita, in *2008 IEEE International Reliability Physics Symposium*. Phoenix, AZ, USA: IEEE, Apr. 2008, pp. 597–603. doi: 10.1109/RELPHY.2008.4558952
[11] M. Baldo, L. Laurin *et al.*, in *2022 IEEE International Memory Workshop (IMW)*, 2022, pp. 1–4. doi: 10.1109/IMW52921.2022.9779290
[12] R. Bayle, O. Cueto *et al.*, *Journal of Applied Physics*, vol. 128, no. 18, p. 185101, 2020. doi: 10.1063/5.0023692
[13] L. Crespi, A. Ghetti, M. Boniardi, and A. L. Lacaita, *IEEE Electron Device Letters*, vol. 35, no. 7, pp. 747–749, 2014. doi: 10.1109/LED.2014.2320967