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Trap and self-heating effect based reliability analysis to reveal early aging effect in nanosheet FET

Sunil Rathore [a], Rajeewa Kumar Jaisawal [a], P.N. Kondekar [a], Navjeet Bagga [b,*]

[a] VLSI Design and Nano-scale Computational Lab, Electronics and Communication Engineering Department, PDPM-IIITDM, 482005, India
[b] Indian Institute of Technology Bhubaneswar, Odisha, India

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ABSTRACT

The reliability of the CMOS devices is severely affected due to the presence of interface (Si/SiO_2) trap charges and self-heating effect (SHE). In this paper, we investigated the trap and temperature-dependent performance barrier and aging issues in Nanosheet FET (NSFET). Through well-calibrated TCAD models, we investigated: a) the threshold voltage (V_{th}) modulation due to type (donor/acceptor) and concentration of the trap charges; b) the role of the location of the trap charges around the conduction band (CB) and valence band (VB); c) the impact of the ambient temperature (T_A) and SHE on the performance of NSFET; d) the performance metrics viz I_{ON}, I_{OFF}, subthreshold slope (SS) influenced by the trap assisted SHE; e) the device aging, i.e., end of a lifetime (EOL) defined as V_{th} shift by ± 50 mV. Hence, trap-assisted SHE analysis by varying the ambient temperature is worth exploring for reliable NSFET operation.

1. Introduction

To achieve higher device density, the downscaling of the device dimensions leads to the evolution of the semiconductor industry from planar devices to non-planar devices like gate-all-around FET, FinFETs, Tunnel FET, etc. [1–5]. Among all the promising candidates, the Nanosheet FET has gained significant popularity as a potential high-performance sub-5 nm node device due to the higher drive current, improved electrostatic integrity, immune to short channel effects, and FinFET compatible layout [6–9]. However, the confined geometry of the NSFET is severely influenced by the performance barrier parameters like trap charges, self-heating effect, temperature, etc., which draw attention to research. In general, NSFETs have a higher surface-to-volume ratio, more dangling bonds at the nanosheet sidewalls, and surface damage from etching which exhibits a higher interface trap density than conventional FETs [10–11]. On similar grounds, the stacked channels constrain the heat flow path; thus, NSFETs are severely affected by the SHE, as the stacked channels are surrounded by the low thermal conductivity material [12,13]. The interface trap charges and induced SHE primarily affects the V_{th} of the device, which is an essential device design parameter. The shift in V_{th} can be used to decide the aging of the device, i.e., end of life (EOL) when V_{th} is shifted by ~ 50 mV.

1.1. The key contribution of this work

(i) the impact of interface trap charge in the Si-SiO_2 interface is investigated by considering both donor and acceptor traps separately; (ii) the significance of the location where the trap charges lie in the energy bandgap (E_g) or around CB/VB is studied; (iii) the investigation of the influence of ambient temperature and SHE induced performance degradation with the presence of traps; (iv) evaluation of the aging effect (ΔV_{th} = 50 mV) for deciding the optimal reliability of the device.

2. Device structure and TCAD setup

The schematic view of the vertically-three-stacked NSFET considered as a baseline reference for the trap and SHE analysis is shown in Fig. 1 (a-b). The source/drain (S/D) pads and channel regions are uniformly doped. Gaussian doping is used in the extension region for considering the realistic scenario. *Sentaurus* TCAD [14] is employed for the device

* Corresponding author.
E-mail address: navjeet@iiitdmj.ac.in (N. Bagga).

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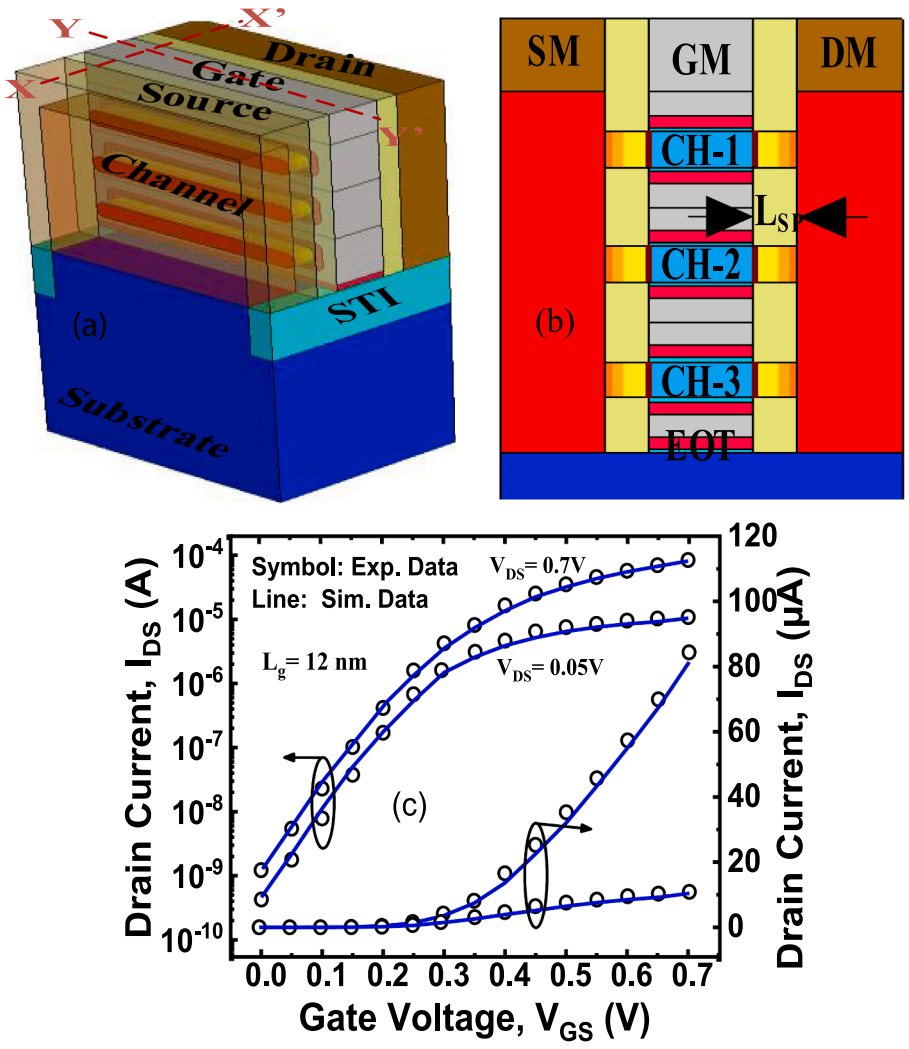

Fig. 1. Shows (a) a three-dimensional (*3D*) schematic of NSFET; (b) a cross-sectional view (along cutline XX') showing all the relevant portions and dimensions of the device; (c) calibration of TCAD models, showing simulated I_{DS}-V_{GS} against the experimental data [6]. The parameters used in the simulation are mentioned in Table 1.

Table 1
Parameter Table.

Parameter	Value
Gate Length (L_G)	12 nm
Eff. Oxide Thick.	0.9 nm
Spacer Length (L_{SP})	5 nm
Sheet Thickness	5 nm
Sheet Width (W)	25 nm
Sheet Spacing	11 nm

simulation, and the device parameters are mentioned in Table 1 unless stated otherwise. The conventional drift/diffusion (DD) model is coupled with the density gradient model to capture the carrier transport and govern the spatial and electrostatic quantum confinement in the 5 nm thick channel. The modified local density approximation model (MLDA) is incorporated to consider the carrier distribution near the oxide/silicon interface, vertical field mobility, and ballistic mobility, and a high field saturation model is included to consider the short channel effects (SCEs) [15,16]. The IAL mobility model governs the surface roughness scattering effect on mobility. The Slotboom and SRH models are used to capture the doping/temperature-dependent bandgap and recombination, respectively. High-*k* mobility degradation models

such as remote phonon scattering and remote Columb scattering capture the excepted leakage current degradation. Finally, the work function of TiN is tuned to match the transfer characteristics (I_{DS}-V_{GS}), showing a good match in TCAD and experimental data [6], as shown in Fig. 1(c). The *Sentaurus* TCAD uses the statistical impedance field method (along with the Poisson distribution function) to investigate the interface trap variability [17]. The domination of the resistive phonon process compared to the normal phonon process leads to the ballistic phonon at low and normal temperatures [18–19]. The doping and temperature-dependent thermal conductivity (k_{th}) reduces at the nanoscale regime due to phonon mean free path and phonon boundary scattering.

The phonon Boltzmann equation (BTE) with relaxation time approximation (RTA) model is used to compute the device lattice temperature [20].

$$k_{th} = \frac{1}{3} \times \frac{1}{2\pi^2} \times n_i \sum_i \int_0^{2\pi f_{0,i}} \frac{\tau_{2\pi f,i}}{v_{2\pi f,i}} B(2\pi f)(2\pi f)^2 d(2\pi f) \quad (1)$$

$$B(x) = kx^2 e^x (e^x - 1)^{-2} \quad (2)$$

where, $x = 2\pi\hbar f/kT, 2\pi f_{o,i}, \tau_{o,i}, v_{o,i}$ are the peak frequency, total RTA, and sound velocity, respectively. For longitudinal ($i = L$) and transverse ($i = T$) modes, $n_L = n_T = 1$. Further, the quantum-corrected DD model coupled with hydrodynamic and thermodynamic models is employed to capture the SHE-induced thermal degradation for the sub-5-nm technology node to precisely predict the nanometer geometry effects.

3. Results and discussion

This work investigates the influence of the interface trap charges and SHE-induced thermal effect on NSFET aging. In NSFET, the channel regions are surrounded by the low thermal conductivity material, i.e., SiO_2, which confines the heat flux in the channel direction [Fig. 2 (a-b)]. This causes an increase in the lattice temperature, resulting in SHE-induced performance degradation (Fig. 2c). To investigate the impact of interface trap charges, we considered randomly located both donor and acceptor traps at the *Si-SiO₂* of each channel in NSFET (Fig. 3). In the following sub-sections, we analyzed the impact of trap location and trap charge concentration on the device performance, revealing the device's aging considering the SHE.

3.1. Impact of trap energy location

The location where the trap charges lie, i.e., either in between the E_g, above CB, or below VB, plays a vital role (Fig. 4). The shift in location is fixed by the Fermi potential, i.e.,$\varphi_F = kT/qln(N_{ch}/n_i)$, where N_{ch} and n_i are channels and intrinsic doping, respectively. We have considered the peak trap density $N_0 = 1 \times 10^{12}$ cm^{-2} and standard deviation $\sigma = 0.2$ eV. The acceptor traps become negatively charged below the Fermi Level (FL) and neutral above the FL. The shift in energy location of acceptor (donor) traps induces the deviation in the I_{DS}-V_{GS} [Fig. 4a (d)]. Thus, the acceptor traps near the CB edge reduce the V_{th} (Fig. 4b), thereby reducing SS and I_{OFF} (Fig. 4c). In contrast, the donor traps become positively charged above the FL and neutral below the FL. Therefore, an opposite trend in V_{th} is observed (Fig. 4e) and alters other parameters

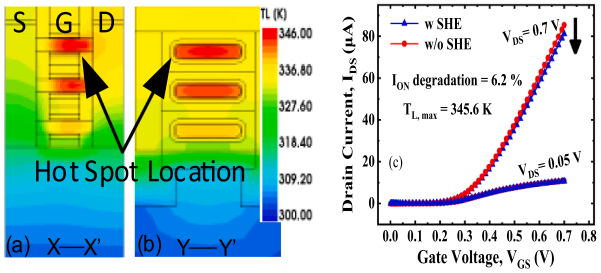

Fig. 2. Shows the hotspot location found at the channel (sheets) near the drain (a) along the channel direction (x-x'); (b) along the transversal direction (y-y'). the maximum temperature is accumulated towards the channel/drain interface due to the low thermal conductivity material wrapped around the channel. (c) exhibition of the on current (i_{ON}) degradation in the transfer characteristics due to SHE.

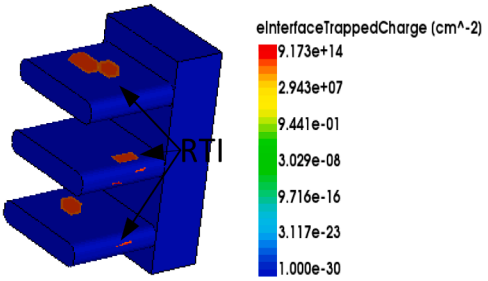

Fig. 3. Shows the random traps located at the*Si-SiO₂* interface in a three-stacked Nanosheet FET.

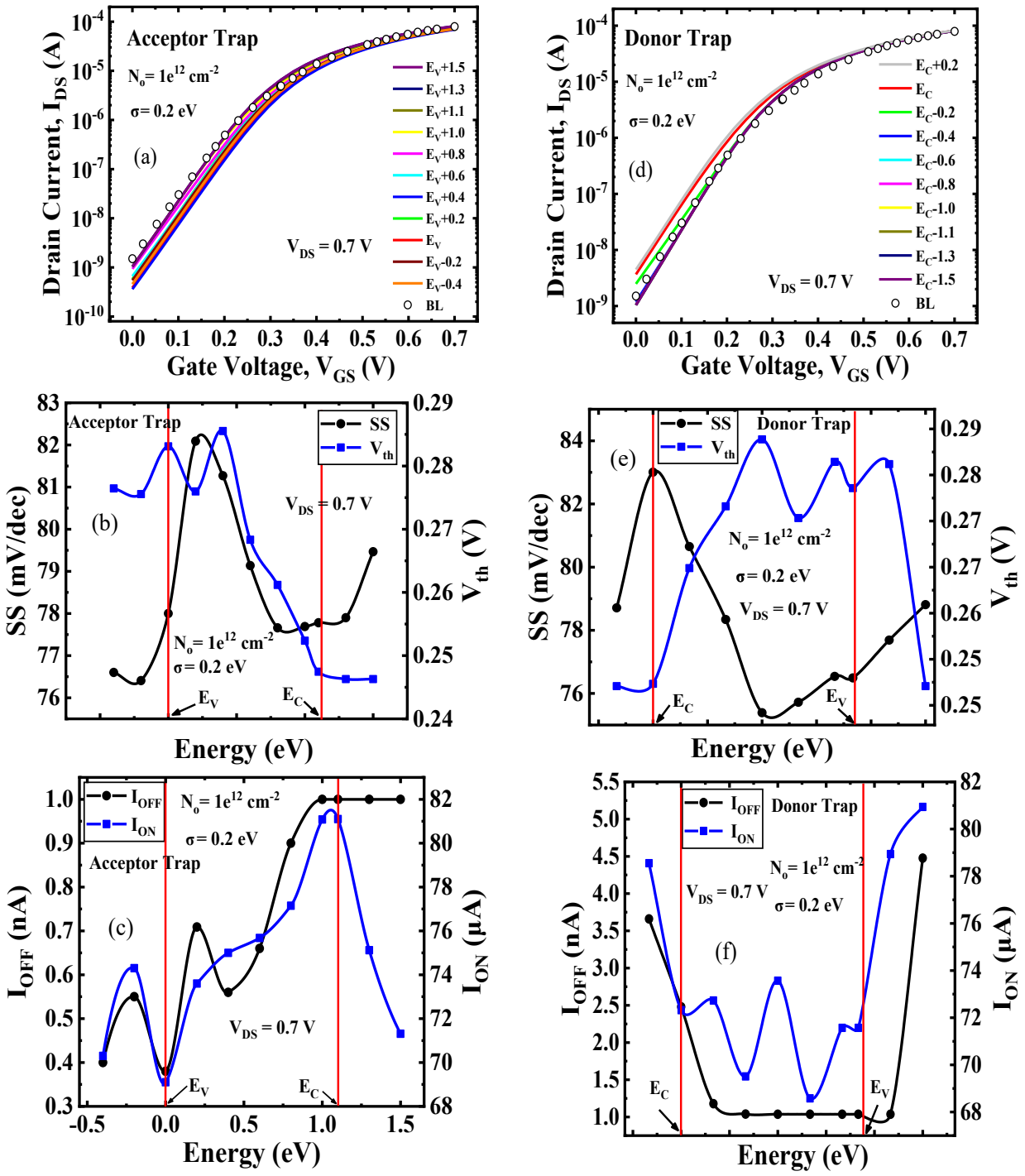

Fig.4. Shows (a) the impact of the acceptor trap location on i_{DS}-V_{GS} characteristics. The shift in I_{DS}-V_{GS} shows the significance of trap location in the bandgap. For acceptor [donor] traps, the location is measured with respect to the VB [CB] edge with the interval of φ_F; (b) threshold voltage (V_{th}) decreases when the location of acceptor traps moves towards the conduction band (CB), then the charges do not get any vacant energy state near the valence band (VB); (c) I_{ON} and I_{OFF} variation for acceptor traps with varying location; (d) the impact of the donor trap location on I_{DS}-V_{GS} characteristics; (e) variation of V_{th} and SS with trap location; (f) I_{ON} and I_{OFF} variation for donor traps with the varying location.

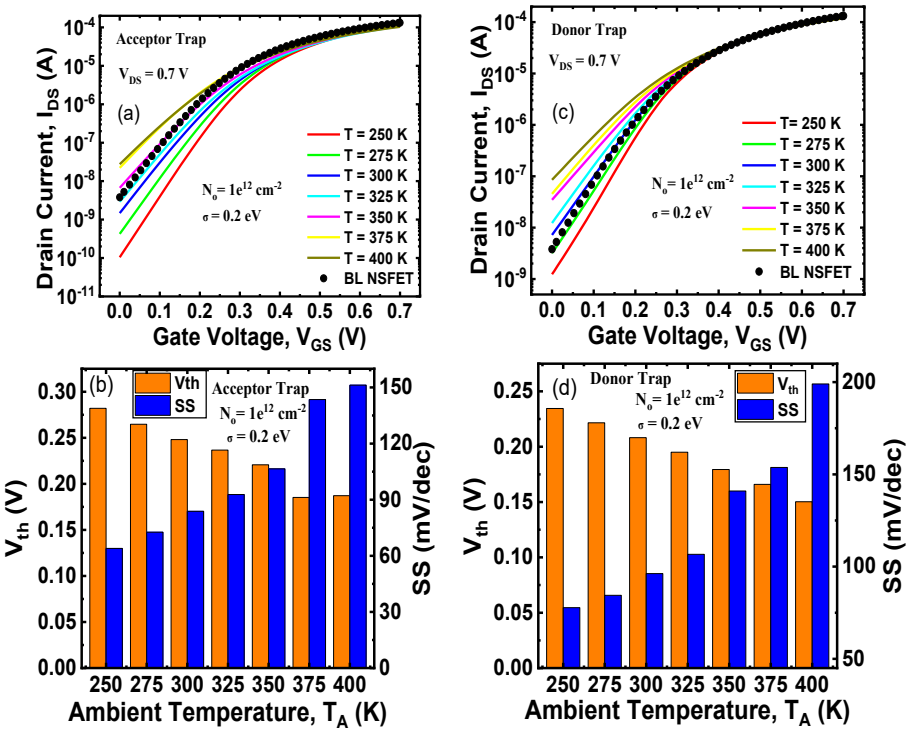

Fig. 5. Shows the consideration of she with varying ambient temperature for fixed trap concentration and location [acceptor (donor) traps taken at vb (cb) edges]. (a) the i_{DS}-V_{GS} characteristics for acceptor traps; (b) variation in V_{th} and SS with varying ambient temperature considering acceptor traps; (c) I_{DS}-V_{GS} characteristics show that the donor traps are prone to the temperature effect as they provide extra charges in CB and thus increase the $I_{OFF;}$ (d) variation in V_{th} and SS with varying ambient temperature considering donor traps.

like $I_{ON,}$ I_{OFF} (Fig. 4f), and SS (Fig. 4e).

3.2. Effect of ambient temperature

The peak energy density of the traps follows the Gaussian distribution with a standard deviation (σ) for the donor and acceptor traps. By keeping the fixed trap concentration and fixed σ, the impact of SHE by varying the ambient temperature has been analyzed (Fig. 5). With the temperature rise, the acceptor (donor) trap concentration decreases (increases) the channel charges resulting in less (more) leakage current, as shown in Fig. 5 a(c). This increase in temperature shows a significant shift in V_{th} compared to the baseline (BL) case, i.e., at room temperature 300 K. As the ambient temperature increases from 250 K to 400 K, the V_{th} shift is more pronounced in the acceptor trap case [Fig. 5 (b)], whereas the donor trap causes higher SS [Fig. 5(d)]. In addition, the concentration of the trap charges has a significant role as it alters the overall channel charge.

3.3. Impact of trap concentration

In this subsection, we have investigated the impact of varying the peak concentration of the trap charges from 10^{11} to 10^{13} cm^{-2} (Fig. 6), keeping the location fixed, i.e., donor trap at CB edge and acceptor trap at VB edges, respectively. With an increase in acceptor trap concentration, the charge concentration at Si/SiO_2 interface decreases, which reduces the effective charge in the channel region; hence the leakage current reduces [Fig. 6(a)] and I_{ON}/I_{OFF} current ratio [Fig. 6(b)] and threshold voltage reduces [Fig. 6(c)]. Thus, by increasing the acceptor trap concentration at the VB edge, the overall electrical characteristics of the NSFET improve significantly. However, with an increase in donor trap concentration, the OFF current significantly increases[Fig. 6(d)], resulting in a deteriorating I_{ON}/I_{OFF} current ratio [Fig. 6(e)], owing to threshold voltage reduction [Fig. 6(f)].

3.4. Aging analysis (EOL)

Improving the reliability of the Nanosheet FET is a key challenge owing to its confined intrinsic geometry, which is severely affected by the interface trap charges and self-heating effect. Fig. 7 (a, b) shows the threshold voltage variation (ΔV_{th}) with acceptor and donor trap concentration, respectively. The acceptor trap concentration is more resilient to NSFET EOL (i.e., threshold voltage variation by 50 mV). The donor traps present at Si/SiO_2 the surface interface is more prone to ambient temperature (T_A) induced EOL degradation in NSFET because it provides extra charges in the channel region [Fig. 7 (c, d)]. The ambient temperature-induced ΔV_{th} variation of both donor and acceptor concentration shows that acceptor trap charges are more susceptible to the EOL variation than the donor trap charge [Fig. 7(e)]. Hence, the combined impact on the NSFET performance will provide an optimal design guideline to detain the early aging of the device.

4. Conclusion

In this work, using well-calibrated TCAD models, we comprehensively analyzed the impact of interface trap charges at Si/SiO_2 and SHE-induced thermal degradation to predict the reliability and EOL in a

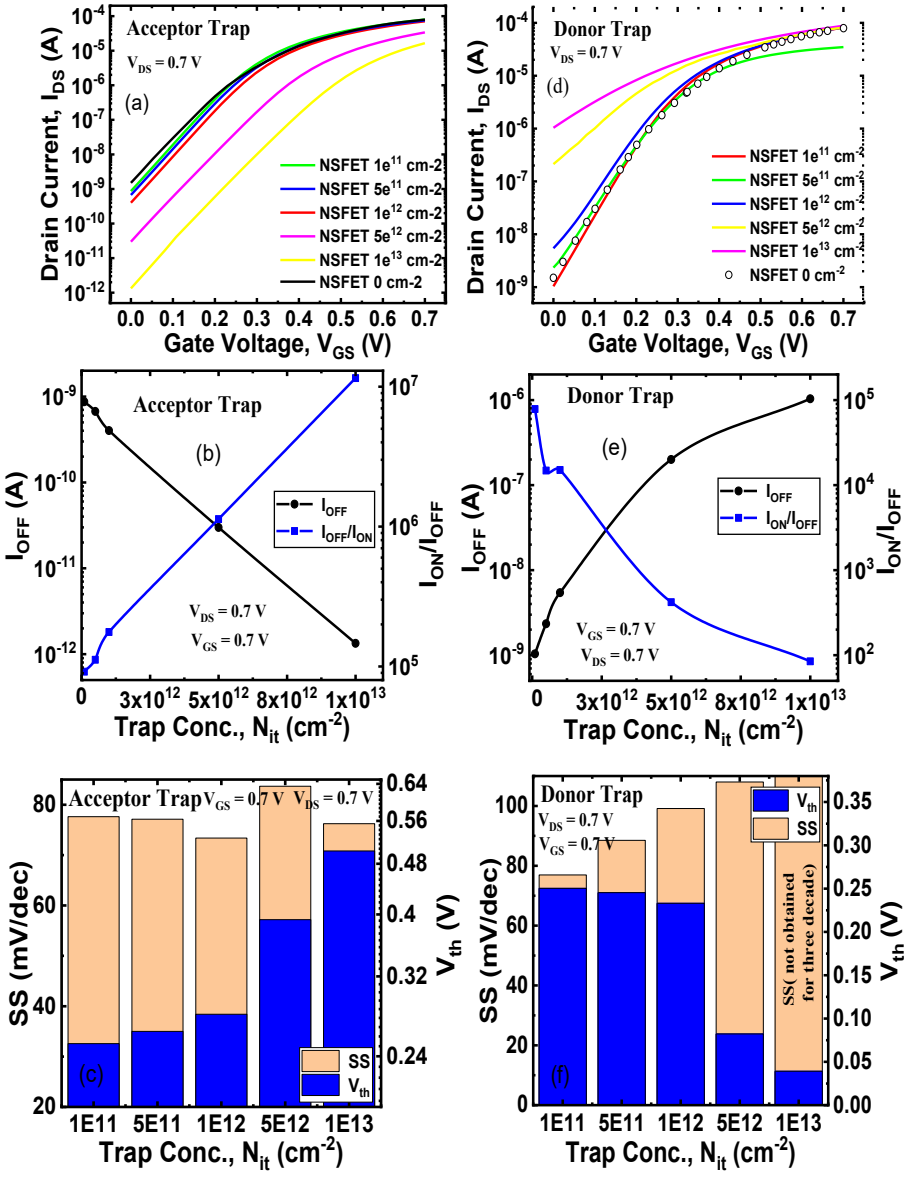

Fig. 6. Shows the impact of varying the trap charge concentration (n_{it}) from 10^{11} cm^{-2} to 10^{13} cm^{-2} for acceptor (donor) traps with a standard deviation of σ = 0.2 eV at room temperature. (a) I_{DS}-V_{GS} curves for varying acceptor trap concentration; (b) I_{OFF} and I_{ON}/I_{OFF} variation with varying acceptor N_{it}; (c) SS and V_{th} variation with varying acceptor N_{it}; (d) I_{DS}-V_{GS} curves showing that increasing the donor trap concentration increases the effective charge concentration in the channel region, thus, I_{ON}; (e) at higher gate voltage (V_{GS}), with donor N_{it}, the inversion charges increase which reduce the mobility hence reduce (increases) the I_{ON}/I_{OFF} (I_{OFF}); (f) SS and V_{th} variation with varying donor N_{it}.

promising emerging sub 5 nm technology node nanosheet FET. Both traps, i.e., donor and acceptor, have been considered separately, and investigated the effect of their location and concentration. The effect of interface trap charges becomes more severe with ambient temperature. Thusly, the trap and temperature-induced V_{th} shifts occur in the device, which results in end-of-life (EOL). Hence, properly investigating these performance barrier parameters is worthy of achieving optimal NSFET performances.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The authors do not have permission to share data.

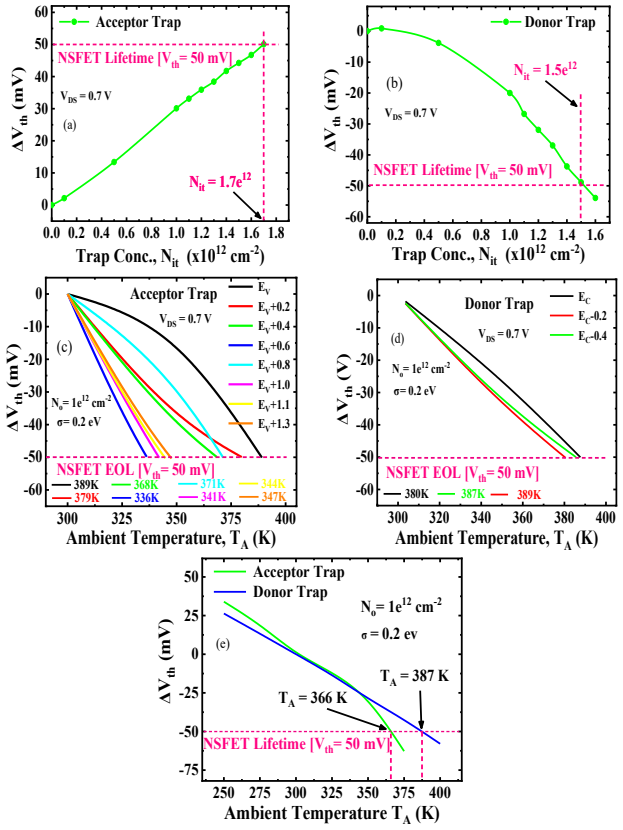

Fig. 7. Shows [a(b)] the acceptor (donor) trap concentration induced threshold voltage variation; [c (d)] the impact of the acceptor (donor) trap energy location and ambient temperature-induced v_{th} modulation effectively determining the EOL; (e) ambient temperature-induced V_{th} variation, showing that acceptor traps are more susceptible to the ambient temperature-induced EOL.

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