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TCAD-based design and verification of the components of a 200 V GaN-IC platform☆

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ABSTRACT

This paper describes the TCAD-based design and verification of the different components of a 200 V GaN-on-SOI integrated circuits (ICs) platform developed on 200 mm substrates. This platform comprises of depletion-mode (d-mode) MIS-HEMTs, and Gated-Edge-Termination Schottky barrier diodes (GET-SBDs) monolithically integrated in an enhancement-mode (e-mode) HEMT technology baseline. A variety of low-voltage analog/logic devices and passive components further supports the GaN ICs platform. Device simulations have been verified using measured low voltage test structures. Verification of simulations with the measurements results in calibration of sheet resistance (R_{sh}) in the gate and access region, threshold voltage (V_{th}), drain current (I_{ds}), ON-resistance (R_{ON}), gate current (I_g) for HEMT structures, and turn-on voltage (V_T) and forward voltage drop (V_F) for GET-SBD structure.

1. Introduction

GaN power devices are promising for high voltage and high-power applications to operate at increased switching speeds due to its superior fundamental material properties [1]. To exploit the full potential of GaN, parasitic inductance or capacitance arise due to the interconnections and layout of PCB should be minimized to overcome the various reliability issues, such as undesired turn-on due to voltage spikes at the gate terminal and the ringing effect [2]. Discrete GaN power devices are generally driven by an external driver IC with narrower margins compared to counter Si power devices, thus more prone to spurious voltage spikes at the gate terminal [3]. Devices can be integrated at great densities, thanks to the GaN heterojunction structure's lateral layout. The reduction of parasitic interconnect inductance between drivers and power devices and the tight control of the dead-time between switching the low-side and high-side power devices are just two benefits of the monolithic integration of the GaN power devices and drivers in a half-bridge configuration [4]. It makes it possible to co-integrate extra features like protective circuitry, separate level shifters, temperature management, and control circuits. By utilizing GaN-on-SOI or GaN-on-QST substrates in combination with deep trench isolation, the demonstrated GaN-IC platform efficiently suppresses back-gating effects in the high-side power device and crosstalk between the switching power devices and the sensitive analog circuits [5,6]. Thibault et al. provides additional information on this platform about the epitaxial structure and the device processing. The components offered are summarized in the schematic overview in Fig. 1 [6]. Low voltage D-mode MIS HEMT replaces Resistor–Transistor Logic (RTL) by Direct-Coupled FET Logic (DCFL) in GaN-IC platform, whereas GET-SBD acts as a freewheeling (flyback) diode or anti parallel diode in rectifier and converter applications.

A pre-existing TCAD process deck for p-GaN HEMTs [7] as well as experimental data are used to calibrate the other components of the GaN-IC platform. This TCAD platform was extended to simulate the additional components, i.e., the co-integrated d-mode HEMTs and Schottky diodes based on the pGaN HEMT technology baseline. This work describes the calibration flow for the Schottky diodes and d-mode HEMTs along with pGaN HEMTs. For verification, overlays between the simulated and measured properties will be displayed. The components used in a 200 V GaN-on-SOI integrated circuit (IC) created on 200 mm substrates were calibrated using Sentaurus TCAD in this paper, and the calibration was verified using measured power devices. The schematic overview depicted in Fig. 1 showcase the accessible components of a 200 V GaN-IC platform. The major objective of this work is to optimize GaN-IC technologies by calibrating the lateral co-integrated GaN power devices with overlay of measured findings.

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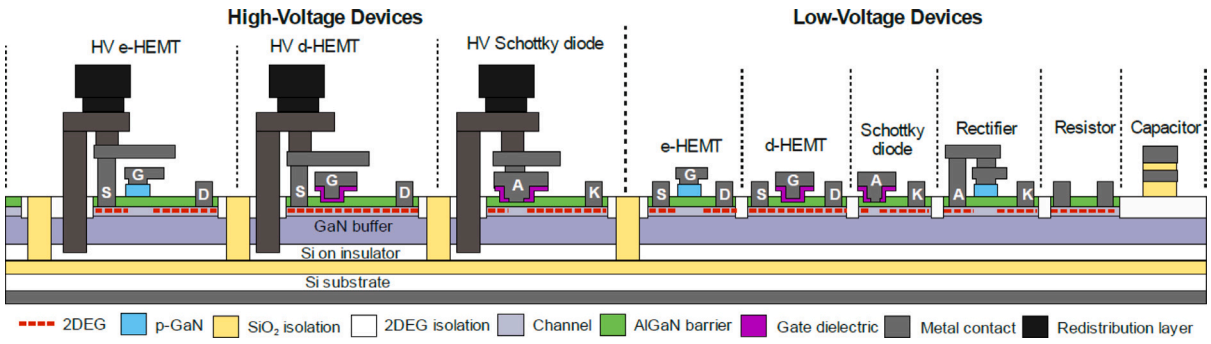
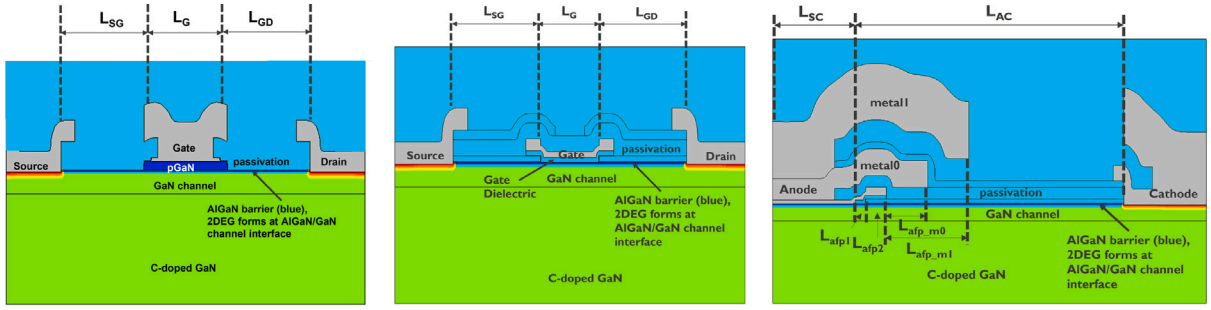


Fig. 1. Schematic cross section of IMEC 200 V GaN-on-SOI Power IC technology with low and high voltage components [6].



(a) (b) (c)

Fig. 2. TCAD calibration structures of (a) low voltage E-mode HEMT, (b) low voltage D-mode HEMT, and (c) 200 V GET-SBD with field plate configurations.

2. Device structure and simulation methodology

On a 200-mm SOI substrate, imec grew the GaN power device components using metalorganic chemical vapor deposition (MOCVD). Starting from the top active region, 80 nm Mg-doped p-GaN, 12.2 nm (Al)GaN barrier and its variability of thickness in gate region depends on the process split, 200 nm undoped GaN channel, back barrier with carbon (C) -doped GaN thickness of 1 μm, (Al)GaN super lattice buffer thickness of 1.65 μm and 200 nm aluminium nitride (AlN) nucleation layer constitutes the epi stack of the lateral power devices in the GaN-IC platform, [8] contains more process details. Fig. 2 shows the schematic view of the simulated symmetrical low voltage (a) E-mode pGaN HEMT, (b) D-mode MIS HEMT, and (c) 200 V GET SBD test structures for calibration. Three process splits with 6 nm, 8 nm (process of reference), 10 nm AlGaN thickness and gate dielectric thickness of 45 nm, 55 nm in the gate region of D-mode MIS HEMT is designed to evaluate the impact of partial recess AlGaN and gate dielectric thickness on V_{TH}. Partial recess of the AlGaN barrier in the gate region (process splits on remaining AlGaN barrier thickness: 6, 8, 10 nm) impacts the D-mode HEMT threshold voltage and GET-SBD turn-on voltage, while the thickness of AlGaN barrier in the access region is 12.2 nm. Simulated low voltage test structures do not have any field plate configurations, whereas GET-SBD has field plate configurations int the following order: L_{afp1} = 0.25 μm, L_{afp2} = 0.5 μm, $L_{afp\text{-}m0}$ = 1 μm, $L_{afp\text{-}m1}$ = 2 μm.

Sentaurus TCAD has been adopted to simulate the GaN-IC components with the standard physical models [9]. The calibration involves process simulations based on the SIMS profile and then fine meshing the critical areas such as GaN channel, passivation and interfaces. Strain activation in piezo electric polarization is adjusted to 80% to account for the calibration of 2DEG density and sheet resistance in the access region. Self-compensating model is considered to model the traps in the buffer with 70% acceptor and 30% donors' type, which are uniformly distributed with trap concentrations and its associated energy levels unique for each region in the epistack. Source for 2DEG density is modeled by the donor interface traps with an activation of 10 % at the passivation/AlGaN interface and at an energy level close to the conduction band (assumed remaining 90% are compensated by the border traps). Gate leakage current is modeled by back-to-back connection of metal/p-GaN Schottky diode and p-GaN/(Al)GaN/GaN (PIN) diodes and leakage path is defined by non-local traps in the AlGaN barrier [10].

3. Results and discussion

Fig. 3 shows the TCAD calibration methodology for extracting the sheet resistance in the gate region ($R_{sh\text{-}gate}$) by varying the gate length of symmetrical low voltage E-mode HEMT and D-mode HEMT test structures with AlGaN recess splits, while the sheet resistance in the access region ($R_{sh\text{-}access}$) already measured to be 765 Ω/□. The extrapolation from the slope of R_{ON} for various gate lengths from 0.8 μm to 20 μm gives the sheet resistance in the gate region for pGaN and D-mode MIS HEMT devices. Extrapolated $R_{sh\text{-}gate}$ values: 550 Ω/□, 1540 Ω/□, 1090 Ω/□, 910 Ω/□ for measured pGaN and D-mode MIS HEMT with AlGaN recess splits of 6, 8, 10 nm are in close match with the simulated $R_{sh\text{-}gate}$ values: 545 Ω/□, 1480 Ω/□, 1026 Ω/□, 822 Ω/□. Thus, access region and gate region resistance components are calibrated for modeling on-state resistance from source to drain by including the gate region. Fig. 4 shows the capacitance–voltage (C–V)/conductance–voltage (G–V) measurement results for the calibration of interface traps (D_{it}) at the passivation/AlGaN interface [5]. Conductance values are calculated from C–V measurements of MIS capacitor for multiple frequencies in between 1 kHz to 1 MHz as shown in Fig. 4a. The following Eqs. (1) & (2) are used for calculation of interface trap density at the passivation/AlGaN interface and the associated energy levels [11]:

$$D_{it} = \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max} \tag{1}$$

$$\tau_e = \frac{exp\left(\frac{E_C - E_T}{KT}\right)}{\gamma_n \sigma_n T^2} \tag{2}$$

D_{it} calculated to be 2.5 times the peak value of conductance from Fig. 4b i.e., 6.625 × 10^{12} eV^{-1} cm^{-2} with a trap energy level of

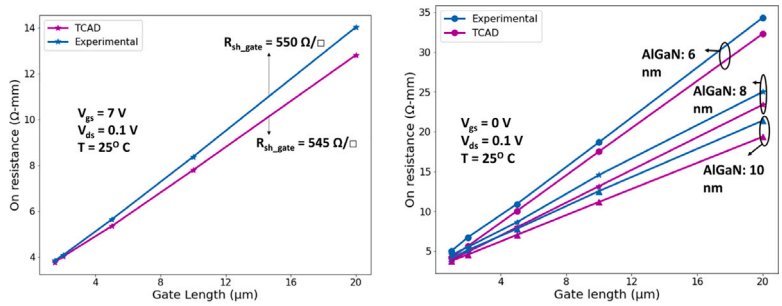


Fig. 3. Extrapolation of sheet resistance in the channel region from ON-resistance (R_{ON}) by varying the gate length of low voltage test structures (a) E-mode HEMT and (b) D-mode HEMT from 0.8 μm to 20 μm, while the sheet resistance in the access region is 765 Ω/□.

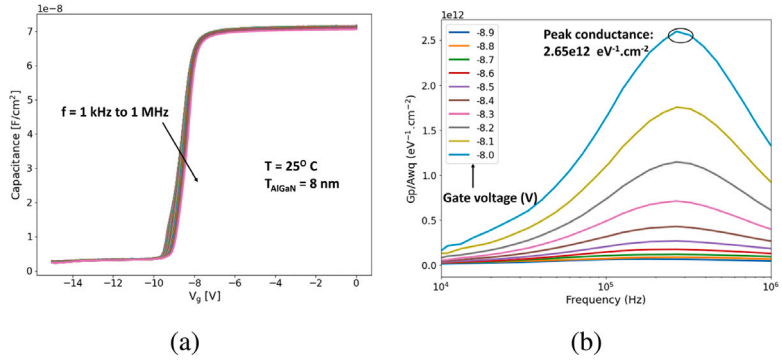


Fig. 4. Extraction of interface traps at passivation/AlGaN interface from measured (a) C–V and (b) G–V curves.

0.32 eV from conduction band (E_C-E_T). The same interface trap concentration and trap energy levels are considered for all the three components (pGaN HEMT, D-mode MIS HEMT, and GET-SBD) with passivation/AlGaN interfaces near to the AlGaN barrier.

Figs. 5, 6, and 7 show the simulated I–V curves overlay with the measured data of E-mode, D-mode HEMTs at room temperature, and GET-SBDs at 25 °C, 150 °C. Fig. 5a shows the simulated band diagram of p-GaN HEMT structure in the gate region, where the conduction band is uplifted to unpin the Fermi level with the formation of Schottky barrier contact on p-GaN gate terminal. Threshold voltage is extracted using maximum transconductance method and simulated V_{th} and on-resistance (R_{ON}) of E-mode HEMT is 2.9 V and 5 Ω-mm, which matches experimental results as shown in linear (Fig. 5b) and logarithmic scale (Fig. 5c). Fig. 5d shows the measured gate current in the E-mode HEMT overlay with simulated gate current. Gate current in p-GaN HEMT is modeled by the back-to-back connection of Schottky and PIN diode in the gate region and observed to be around 1×10^{-4} A/mm for a maximum gate bias of 7 V. Fig. 6a shows the simulated band diagram of D-mode MIS HEMT structure in the gate region for recess splits of 6, 8, and 10 nm, where the Fermi level pinning in the gate region allows the formation of 2DEG at equilibrium condition ($V_S = V_D = V_g = 0$ V). I_d-V_g simulations of D-mode HEMT are performed to analyze the impact of remaining AlGaN thickness in the gate region and also the impact of dielectric thickness on V_{th}, as shown in Fig. 6b and c. Measured V_{th} for recess splits of 6, 8, 10 nm with a dielectric thickness of 45 nm is observed to be −6 V, −9 V, and −12 V, which are in match with the simulated V_{th}. In line with process plits, measured V_{th} values are matching with simulated values for a gate dielectric thickness of 45 nm and 55 nm with recess split of 8 nm in the gate region. Forward measured I–V characteristics of GET-SBDs for an AlGaN split of 8 nm are compared with simulations to analyze the V_T and V_F, as shown in Fig. 7a and b. Simulated Schottky barrier structure is modeled with a work function of 5.1 eV along with barrier lowering mechanism to model forward currents. V_T and V_F for GET-SBD is measured at 25 °C and 150 °C for corresponding forward currents: 1 mA/mm and 0.1 A/mm. Ideality factor is calculated for GET-SBD to determine the rectification property of the diode and higher the value means schottky contact is not good enough for rectification. Ideality factor of simulated results are slightly higher compared to measured forward currents. Table 1 lists the simulated parameters compared to the measured results of 200 V GET SBDs at 25 °C and 150 °C.

Table 1
Comparison of simulated and experimental results of 200 V GET-SBD.

Parameter	TCAD	Experimental
V_T: 25 °C	0.89 V	0.90 V
V_T: 150 °C	0.68 V	0.68 V
V_F: 25 °C	1.42 V	1.42 V
V_F: 150 °C	1.67 V	1.67 V
Ideality factor (η)		
η: 25 °C	1.82	2.06
η: 150 °C	1.21	1.47

4. Conclusion

TCAD simulations were overlayed with measured findings to provide a verification of several components of the 200 V GaN-on-SOI platform. Starting with the calibration of sheet resistance in the gate/access region and interface traps at the passivation/AlGaN interface, physics-based simulations were performed adequately to be capable of reproducing in comparison to the low voltage test structure measured data. The back-to-back connection of Schottky and PiN diodes was used to represent the gate leakage current mechanism in the p-GaN gate topology. Electrical parameters: V_{th}, I_{ds}, R_{ON}, I_g, V_T, and V_F was compared to measured findings to help device designers not only improve performance but also optimize GaN-IC process parameters.

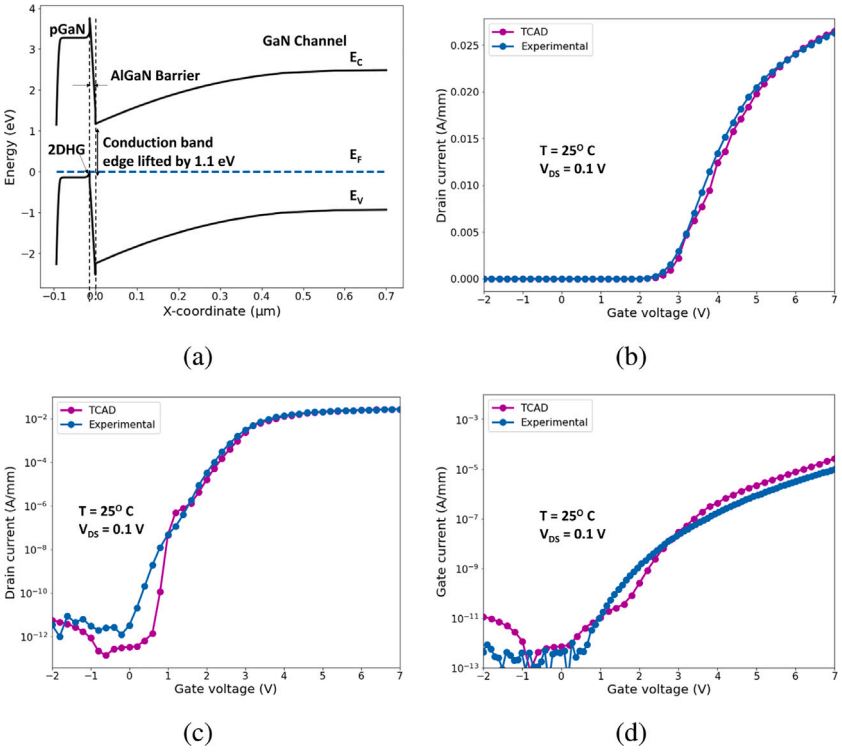


Fig. 5. (a) Band diagram of E-mode pGaN HEMT TCAD calibration structure shows unpinned Fermi level (depletion of 2DEG under pGaN at AlGaN/GaN interface) at equilibrium condition ($V_g = V_d = V_s = 0$ V). Transfer characteristics of low voltage test structure ($L_G = L_{GD} = L_{SG} = 1.5$ μm) in (b) linear, (c) semi-logarithm scale, (d) gate current with the comparison of experimental results.

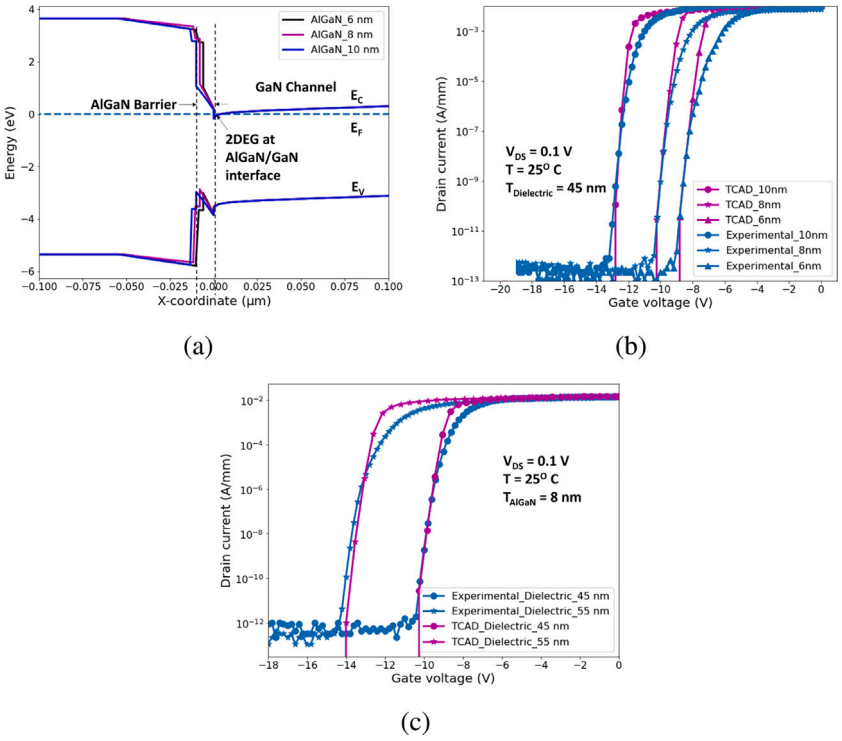


Fig. 6. (a) Band diagram of D-mode HEMT TCAD calibration structure shows the pinned Fermi level (2DEG formation) for AlGaN process splits of 6, 8, 10 nm. Transfer characteristics of low voltage test structure ($L_G = 1.3$ μm, $L_{GD} = L_{SG} = 3.0$ μm) in comparison with experimental results for (b) AlGaN splits in the gate region, (c) gate dielectric thickness of 45 nm, and 55 nm.

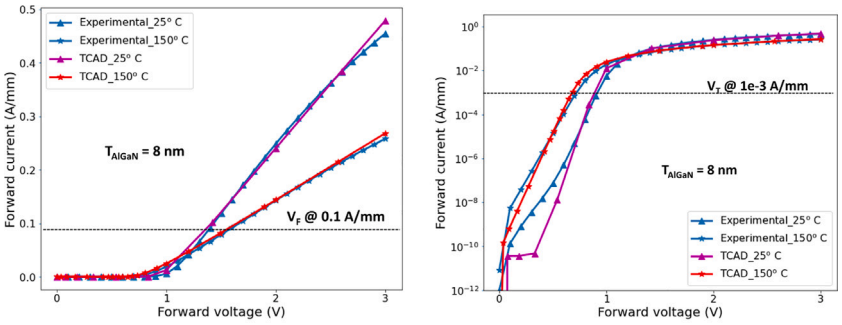


Fig. 7. Forward I–V characteristics of 200 V GET SBD (L_{SC} = 2.0 μm, L_{AC} = 6.5 μm) in (a) linear and (b) semi-logarithm scale with the comparison of experimental results.

CRediT authorship contribution statement

Pavan Vudumula: Conception and design, or analysis and interpretation of the data, Drafting the article or revising it critically for important intellectual content. **Thibault Cosnier:** Analysis and interpretation of the data. **Olga Syshchyk:** analysis and interpretation of the data. **Benoit Bakeroot:** Conception and design, or analysis and interpretation of the data. **Stefaan Decoutere:** Drafting the article or revising it critically for important intellectual content.

Data availability

Data will be made available on request.

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