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TCAD-Based RF performance prediction and process optimization of 3D monolithically stacked complementary FET

Shu-Wei Chang [a], Jia-Hon Chou [b], Wen-Hsi Lee [a], Yao-Jen Lee [c], Darsen D. Lu [d,*]

[a] Department of Electrical Engineering, National Cheng Kung University, Tainan City 701401, Taiwan
[b] M.S. Degree Program on Nano-IC Engineering, Department of Electrical Engineering, National Cheng Kung University, Tainan City 701401, Taiwan
[c] International College of Semiconductor Technology, National Yang Ming Chiao Tung University, Hsinchu City 300093, Taiwan
[d] Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, Tainan City 701401, Taiwan

A B S T R A C T

Radio frequency devices based on the state-of-the-art gate-all-around (GAA) nanosheet CFET process suffer from extra parasitic capacitance due to the stacked architecture compared to planar or FinFET devices. In this study, we first calibrate the TCAD process simulation model to experimental data. Subsequently, the model is applied to the simulation of RF characteristics of CFET devices with similar design as our real devices. Subsequently, the influence of various design parameters of the CFET structure are investigated, with emphasis on high frequency characteristics. The optimal design for CFET-based RF device is determined, which resulted in and f_T and f_{Max} improvements by 3.74 times and 8.44 times, respectively.

1. Introduction

Polycrystalline silicon thin-film transistors (poly-TFTs) with low fabrication temperature, moderate carrier mobility and CMOS compatibility may be optimized for radio frequency (RF) operation to enable system on panel (SoP), or stacked above CMOS devices during back-end-of-line (BEoL) processing for monolithic 3D-IC (M3D) applications [1,2]. In recent years, three-dimensional structures such as FinFET, nanowire and nanosheet are adopted for optimal electrostatic control and device performance. In particular, the on-state current of nanowire and nanosheet devices is enhanced multifold with stacked channels, while maintaining excellent gate controllability through their gate-all-around structure. To continue footprint scaling, we have demonstrated a CFET technology which consists of pFETs stacked on top of nFETs, with gate-all-around junctionless nanosheet design, for M3D logic applications [3]. In this study, we further fabricate poly-Si RF devices along with CFET-based logic circuit, realizing heterogeneous integration. Like CFETs, the RF devices also have upper p-type and lower *n*-type channels. This not only boosts device density but also extends CFET towards diverse applications. However, direct application of CFET towards RF without optimization is inappropriate due to parasitic capacitances between the stacked channels and the extra gate-to-drain capacitance, which lead to poor cutoff frequency (f_T) and maximum oscillation frequency (f_{Max}). In this study, we simulate a CFET device which mimics the process and device structure in our previous experimental work [1] with TCAD [4] and analyze its electrical properties, focusing on high frequency performance [5].

2. Simulation setup and device structure

We adopted process simulation (Sentaurus Process) to construct the device structure, since the series resistance of the thin source/drain, contact resistance, residual high-k/metal gate after gate definition, and other process-induced non-ideal structures should be considered when we calibrate the TCAD model to experimental data. Fig. 1**(a)** shows the 3-D schematic of the CFET with a p-type nanosheet device stacked on an *n*-type nanosheet device with raised source and drain. Raised S/D is formed by protecting the source/drain area with photoresist during the channel thin-down process. Fig. 1**(b)** is the cross-section of the channels, which is similar to experimental CFET devices (Fig. 1**(d)**). HfO_2 and TiN were considered as gate dielectric and metal gate materials, respectively. Fig. 1**(c)** shows the cross-section of the source/drain regions of top and bottom devices. The source and drain doping concentrations of p- and *n*-channels are $8 \times 10^{19}/cm^3$ (boron) and $3 \times 10^{19}/cm^3$ (phosphorus), respectively, according to our previous analysis [6]. The device parameters applied for 3-D TCAD simulation is given in Table 1. We investigate the impacts of tuning individual process parameters, including nanosheet channel width ($W_{CH} = 40 \sim 200$ nm), release width ($W_R = 5 \sim 30$ nm), lateral-etched width of the sacrificial layer, sacrificial oxide thickness ($T_S = 20 \sim 70$ nm), or the spacing between two

* Corresponding author.
E-mail address: darsenlu@mail.ncku.edu.tw (D.D. Lu).

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silicon channels, and the source/drain thickness (T_{SD} = 8 ~ 50 nm), analyzing the impact of each parameter. The definitions of each parameter are illustrated in Fig. 1**(a)**. The TCAD CFET model is calibrated to measurements by adjusting the surface scattering model to account for lower mobility in the polysilicon channel. The model of quantum confinement we adopted is the default one in TCAD, which is the density-gradient model. The BTBT model is Hurkx and the mobility model is the inversion and accumulation layer mobility model (IALMob) [7]. The device structure with parameters listed in Table 1 was utilized for calibration by matching simulated transfer characteristics (I_D-V_G) to measured data (Fig. 2), with good agreement. The effects of the device parameters on the high-frequency characteristics are investigated in more detail by the analysis of the small-signal equivalent circuit. The relationship between f_T and g_m can be described as equation (1) and the approximate expression for f_{Max} is given by equation (2):

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{1}$$

$$f_{Max} \approx \frac{f_T}{\sqrt{4g_{ds}R_g + 8\pi f_T C_{gd}(R_g + \alpha R_d)}} \tag{2}$$

where g_m is the transconductance; C_{gs} is the gate-to-source capacitance, and C_{gd} is the gate-to-drain capacitance; g_{ds} is the output conductance; R_g is the gate series resistance, which is extracted by the small signal model (equation (3)), and R_d is the drain series resistance.

$$R_g = \left| \frac{Real(Y_{12})}{Imag(Y_{12}) \bullet Imag(Y_{12})} \right| \tag{3}$$

3. Result and discussion

Channel Width (W_{CH}) - In the setting of design rules, channel width enhancement is one way to increase drive current without significant process modifications. The transconductance of RF devices can usually be enlarged through wider channel width design to push operating frequency higher. In Fig. 3, the maximum transconductance is indeed

Table 1
Device parameters of CFET-based RF device for bottom NMOS.

Parameters	Value	Parameters	Value
Channel Width (W_{CH})	60 nm	Gate Length (L_G)	100 nm
Released width (W_R)	30 nm	High-k Thickness	10 nm
Sacrificial oxide thickness (T_S)	30 nm	Channel Thickness	8 nm
S/D thickness (T_{SD})	8 nm	Doping Conc.	3×10^{19} cm^{-3}

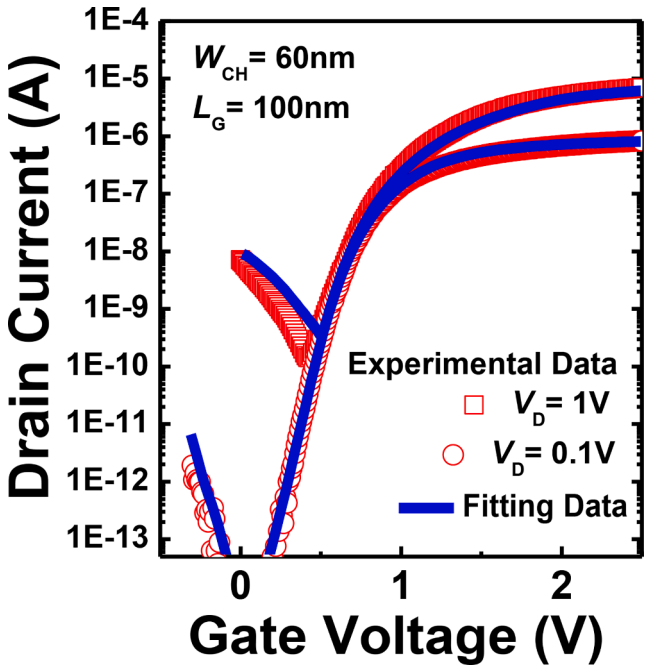

Fig. 2. The I_D-V_G curve simulated using TCAD (Fitting Data) agree well with experimental data.

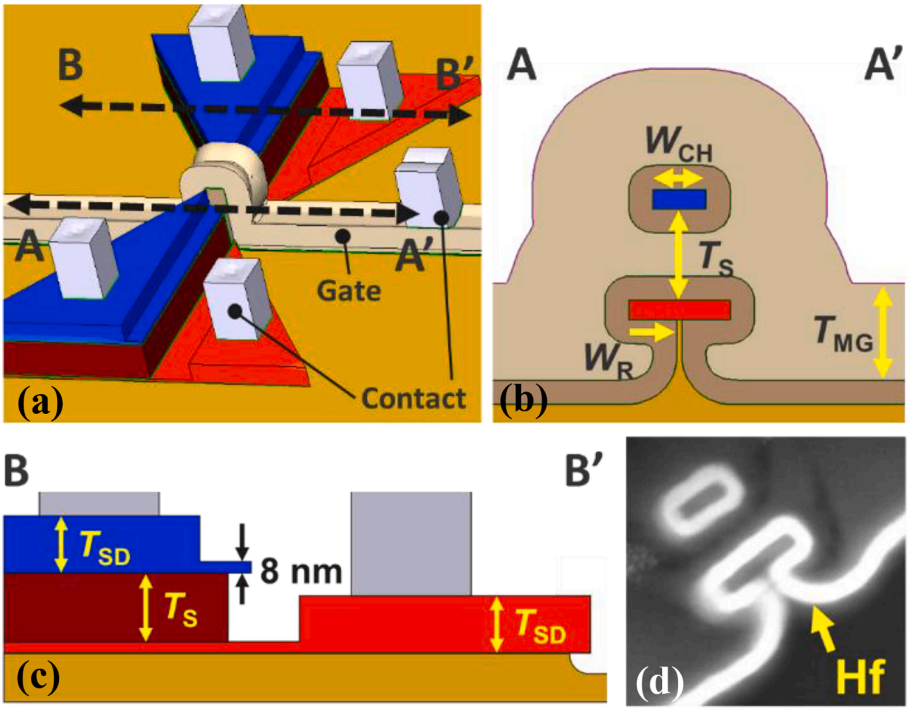

Fig. 1. (a) Cross sectional and (b) top view of CFET generated with Sentaurus Process TCAD simulation. (c) Cross sectional image of CFET-based high frequency device.

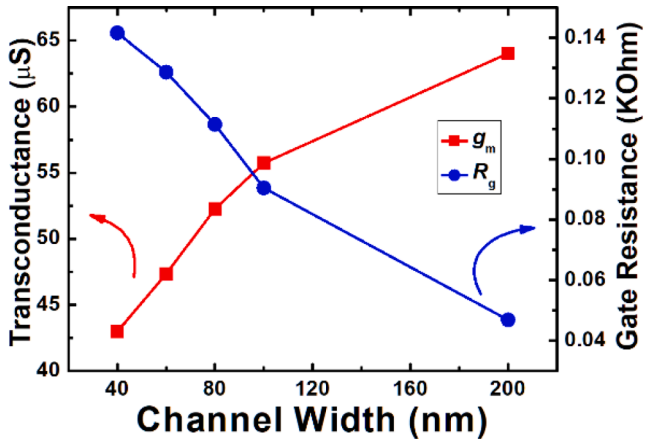

Fig. 3. Maximum transconductance and gate resistance versus channel width of bottom *n*-type nanosheet.

boosted from 43μS to 64μS when bottom nanosheet width is increased from 40 nm to 200 nm. Yet transconductance per effective channel width significantly decreases, likely due to the fixed series resistance of the source and drain (R_{ds}). Therefore, both f_T and f_{Max} decrease at the same time, as shown in Fig. 4. We have also noticed that gate capacitance (C_{gg}) scales roughly linearly with channel width (Fig. 4). Consequently, narrower channel width is a better design for RF CFETs in terms of operating frequency for such R_{ds}-limited scenario, and is also beneficial from a device footprint point of view. Furthermore, shorter etch time poses a lower risk during channel release.

Released Channel Width (W_R) - As the stacked-channel FET is a serious candidate structure for next generation CMOS, the channel release process becomes a crucial step among the entire fabrication process. During channel release, the sacrificial oxide between the top and bottom channels is etched away to make space for the gate stack to ensure the device becomes gate-all-around after high-k/metal gate deposition. Fig. 5 shows that both f_T and f_{Max} are enhanced as W_R increases. When W_R is 30 nm in the 60 nm-width channel (full release), the high-k/metal gate surrounds the channel completely. The higher transconductance can be observed in Fig. 6 with increasing release width due to larger effective width. Furthermore, parasitic C_{gd} and C_{gs} in the stacked structure is significantly reduced, leading to higher frequency as more sacrificial oxide is etched. Therefore, full channel release is essential for stacked nanosheets not only for better gate controllability and higher transconductance but also for lower parasitic capacitances.

Sacrificial Oxide Thickness (T_S) - The thickness of sacrificial layer between top and bottom channels also plays an important role in the

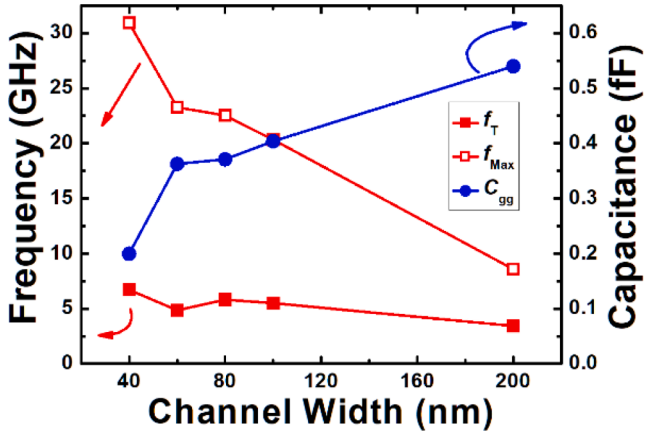

Fig. 4. f_T, f_{Max} and C_{gg} versus channel width of bottom *n*-type nanosheet.

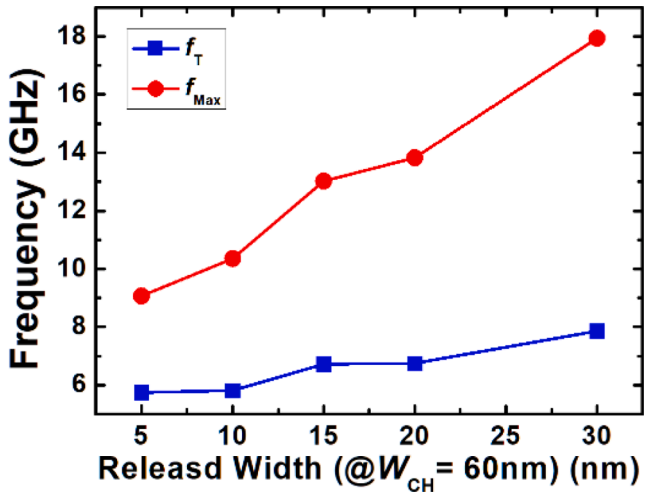

Fig. 5. f_T and f_{Max} versus released channel width of bottom *n*-type nanosheet.

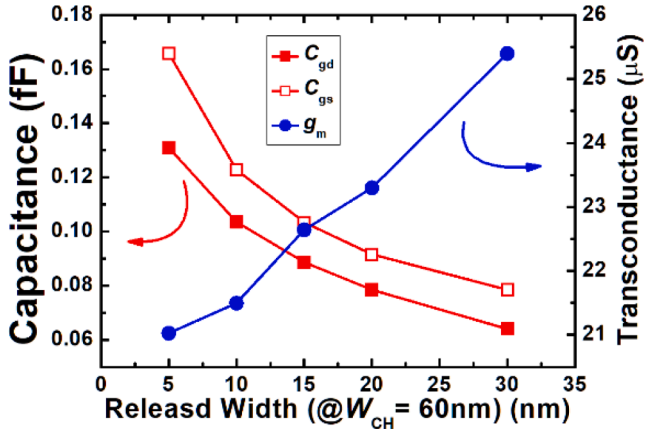

Fig. 6. C_{gd}, C_{gs} and maximum g_m versus released channel width of bottom *n*-type nanosheet.

stacked channel structure. Thick sacrificial layer can make the channel-release process step easier but needs higher aspect ratio isotropic etching technique. On the contrary, thin sacrificial layer may cause channel collapsing after release because of the van der Waals force between the two channels. Thus, a suitable sacrificial oxide thickness is important for maintaining transistor structural integrity. It also influences the device's high frequency characteristics. Fig. 7 shows both f_T and f_{Max} increase with thicker T_S. As the fringe electric field between the two layers becomes weaker with thicker T_S (Fig. 8), the capacitive coupling becomes weaker, thus operational frequency is higher. The simulation results shown in Fig. 9 highlights the fact that g_m increases by 36.9 % due to less back-gating effects from the PMOS, and gate resistance decreases by 34.6 % with less current crowding of the gate metal, when T_S increases from 20 nm to 70 nm (saturation occurs around 50 nm). Meanwhile the fringe capacitance between the two channel layers reduces, leading to 21.9 % lower gate capacitance (not shown). Overall f_T and f_{Max} improve by a factor of 1.71 and 1.96, respectively.

Source/Drain Thickness (T_{SD}) - Since the source/drain thickness is as thin as channel in the original structure, the series resistance of source and drain are pretty high, leading to poor drive current and transconductance. After adopting raised S/D, the on-state current and transconductance have 5.75- and 5.38-fold improvements, respectively (Fig. 10). Both f_T and f_{Max} increase significantly from T_{SD} = 10 nm to T_{SD} = 30 nm, and then increase slightly from T_{SD} = 30 nm to T_{SD} = 50 nm because the reduction of source/drain resistance is negligible when the

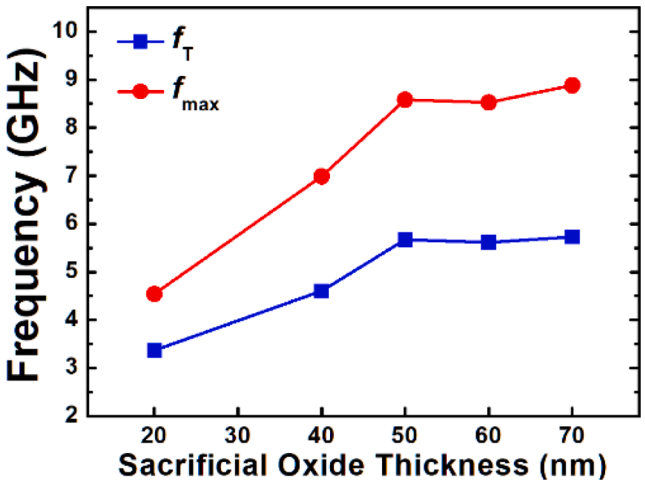

Fig. 7. f_T and f_{Max} versus sacrificial oxide thickness between top p-type nanosheet and bottom *n*-type nanosheet.

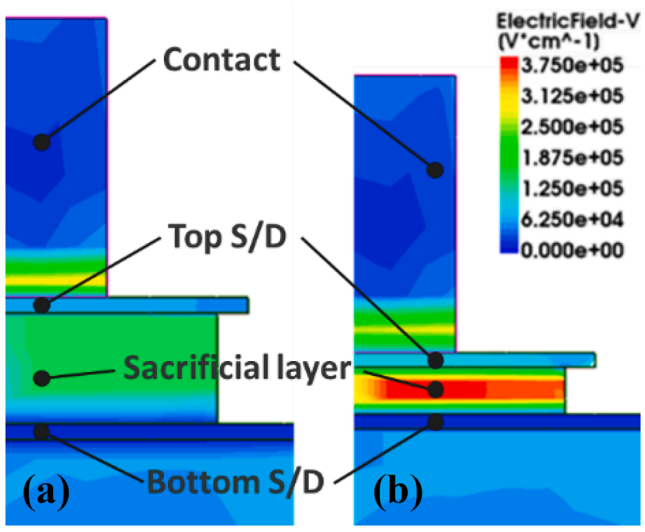

Fig. 8. The electric field between top and bottom source/drain when (a) T_s = 60 nm and (b) T_s = 30 nm.

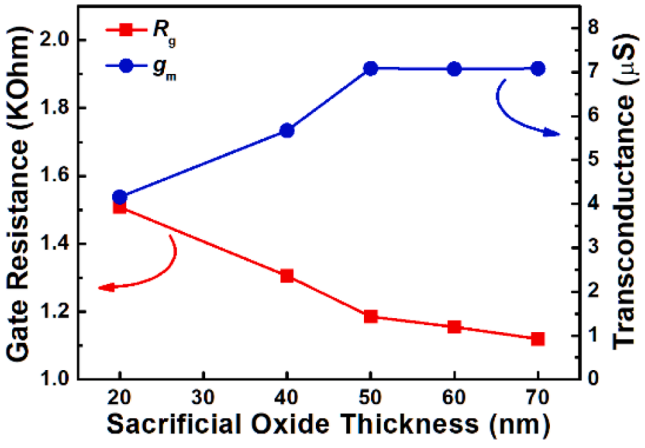

Fig. 9. R_g and g_m versus sacrificial oxide thickness between top p-type nanosheet and bottom *n*-type nanosheet.

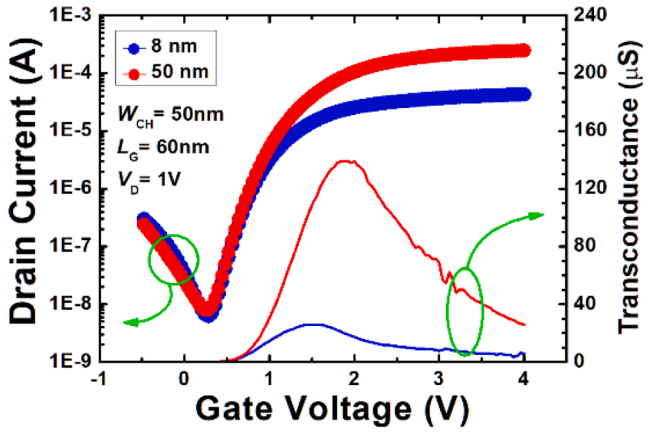

Fig. 10. The I_D-V_G curve and transconductance of bottom *n*-type nanosheet with 8 nm and 50 nm source/drain thicknesses.

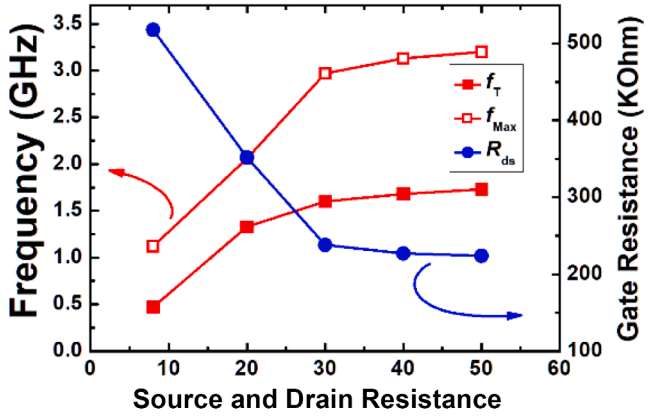

Fig. 11. f_T, f_{Max} and source/drain resistance (R_{ds}) of bottom *n*-type nanosheet with different source/drain thickness.

source/drain thickness exceeds 30 nm (Fig. 11).

Overall Optimization - Table 2 lists the f_T/f_{Max} improvements from each parameter. Narrower channel width, fully released channel, larger distance between the top and bottom devices, and thicker source/drain allow us to achieve a better frequency response for CFET-based RF device. However, the real fabrication process and stability should be considered to realize mass production. Therefore, based on our fabrication experience we anticipate the best conditions for the real devices. For channel width, 60 nm-channel-width devices have higher process stability than 40 nm because of the better channel mechanical intensity. The sacrificial oxide thickness is deposited to be 60 nm instead of 70 nm to avoid high aspect ratio etching. Table 3 summarizes the optimal CFET structure for RF metrics and compares it to the initial un-optimized design point.

Table 2
Summary of TCAD simulation results of change in f_T and f_{Max} after optimizing individual process parameters.

	f_T	f_{Max}
W_{CH} (40 → 100)	−18 %	−31.5 %
W_R (30 → 5)	−29.1 %	−49.2 %
T_S (20 → 70)	+70.5 %	+95.6 %
T_{SD} (8 → 50)	+268 %	+186 %

Table 3
Comparison of RF performance between the calibrated model (Calibration) and optimized model (Optimization).

	Calibration	Optimization
W_{CH} (nm)	60	60
W_R (nm)	30	30
T_S (nm)	20	60
T_{SD} (nm)	8	50
f_T (GHz)	5.3	19.8
f_{Max} (GHz)	6.45	54.41

4. Conclusion

In this work, we successfully investigated the impacts of various structural components (W_{CH}, W_R, T_S, T_{SD}) by TCAD simulation. Finally, we optimize all 4 parameters as part of a performance step-up effort to obtain an optimized CFET structure for RF without adjustment of the process flow, and in the meantime take the real fabrication scenario into consideration. f_T and f_{Max} are improved by 3.74 and 8.44 times, respectively. Thanks to the flexibility of heterogeneous integration of logic, memory, and analog/RF devices on a single chip, we expect to overcome the technology scaling bottleneck due to physical limitation and the increased interconnect delays that naturally occurs with technology scaling using CFET technology.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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