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Switching limits of top-gated carbon nanotube field-effect transistors ☆

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ABSTRACT

The performance limits of carbon nanotube field-effect transistors (CNFETs) based on a recently reported process are studied by computational techniques at temperatures between 300 K and 4 K. The impact of band-to-band tunneling (BTBT) and source-to-drain tunneling (SDT) is examined for devices with varying gate length through the use of simulations based on the non-equilibrium Green's function (NEGF) formalism, and calibrated to measurements. Additionally, the case of junctionless chemical doping profiles is analyzed in contrast to electrostatic doping recently reported for test structures. The switching limits of CNFETs are further explored for devices based on carbon nanotubes (CNTs) with more favorable electronic structures.

1. Introduction

Logic transistors based on carbon nanotubes are promising candidates for increasing densities and power efficiency as compared to Si-based complementary metal oxide semiconductor (CMOS) technologies [1–3]. Recent advances in processing have enabled the fabrication of CNT devices with competitive performance and dimensions. Present challenges to further development of carbon nanotube field-effect transistors (CNFETs) call for workflows involving coordinated experimental and simulation efforts. In previous studies, devices compliant with performance targets for sub−5 nm technologies have been reported, and an efficient quantum simulation framework capable of describing relevant device physics was developed and demonstrated [4,5]. Recently, the accuracy of the simulations has been validated against measurements of devices using top-gate electrodes to modulate doping in lead extensions [6]. In this work, we explore the switching performance limits imposed by tunneling mechanisms in such test structures with varying temperature and gate length. Given practical device technology must minimize power consumption by implementing complementary logic, we extend our study to include devices employing solid-state doping [7]. We consider the case of junctionless doping, as it both simplifies the fabrication process and circumvents challenges in fabricating sharp junctions in ultra-scaled devices [8]. We compare switching in electrostatically doped devices to chemically doped junctionless devices, and further explore CNFETs switching limits by studying the impact of employing CNTs with a smaller diameter.

2. Simulation methodology

A coupled mode-space NEGF solver coupled with a $\vec{k} \cdot \vec{p}$ electronic Hamiltonian is employed to simulate the electrical properties of CNFETs with top-gate geometries. The simulations are performed using the Q^* quantum device simulator enabling efficient and accurate treatment of electrostatics and charge carrier transport for CNT-based devices arranged in arbitrary 3D geometries, including quantum mechanical treatment of phonon scattering and electron tunneling phenomena [9]. Electron transport properties are computed using a self-consistent Poisson–Schrödinger-NEGF approach, where a recursive algorithm is employed to compute the device Green's function [10]. Elastic and inelastic scattering from electron–phonon interactions are described using the formalism and coupling parameters reported in [11]. Carrier injection from end-bonded metal contacts is described by self-energies computed from metallic CNT Hamiltonians [12]. A Schottky barrier height for holes of 0.2 eV has been fitted to match measured ON currents, and is employed in all simulations.

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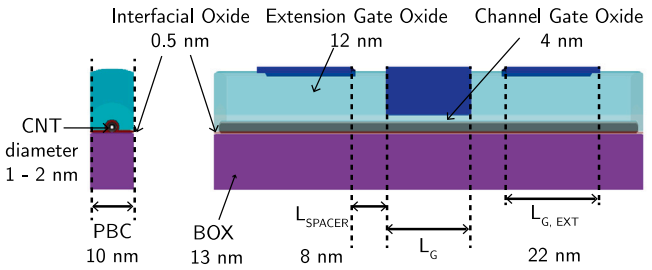

Fig. 1. Schematic of the top-gate device geometry studied. Electrodes located along lead extensions serve to realize electrostatic doping and are omitted when simulating devices with chemical doping. Top oxide is high-κ ($\varepsilon_r = 24$), bottom oxide is SiO_2 ($\varepsilon_r = 3.9$), interfacial oxide is Al_2O_3 ($\varepsilon_r = 8$). Schottky contacts to source and drain electrodes are modeled at both ends of the CNT. Periodic boundary conditions (PBC) are employed along the width direction.

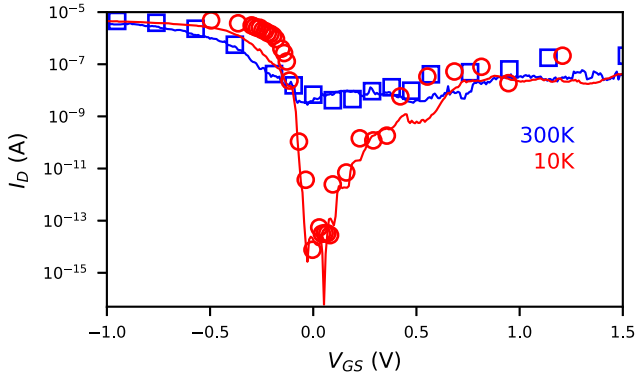

Fig. 2. Current–voltage characteristics of p-type devices at temperatures of 300 K (blue) and 10 K (red). Drain–source bias is $V_{DS} = 0.3$ V. Full lines correspond to measurements, and symbols correspond to simulations.

The devices studied in this work are based on (13, 0) and (25, 0) zigzag CNTs with diameters of approximately 1 nm and 2 nm, respectively, arranged in the top-gate configuration shown in Fig. 1. Boundary conditions applied to electrostatic equations at the contact metal-CNT junctions allow an explicit description of their influence on the electric field throughout the device. Periodic boundary conditions are applied along the width dimension to simulate devices with a finger density of 100 CNT/μm. Electrostatically doped devices are comprised of intrinsic CNTs, where degenerately doped regions are induced along lead extensions to form carrier reservoirs on either side of the channel by top-gate electrodes (Fig. 1). This geometry has been employed to model experimental structures reported in [6]. Devices with chemical doping are modeled without extension gates shown in Fig. 1; a compensating charge homogeneously distributed along the CNT is employed to form a junctionless doping profile. A carrier density of approximately 0.7 nm^{-1} is targeted to match the doping concentrations extracted along lead extensions in electrostatically doped CNFETs.

3. Results

Fig. 2 shows a comparison of simulated and measured electrical characteristics of long-channel p-type devices based on 2 nm diameter CNTs ($E_G \approx 0.45$ eV), at temperatures of 300 K and 10 K. Gate–source bias data from simulations has been shifted and adjusted by a multiplicative factor in order to phenomenologically account for non-ideal gate coupling derived from interface traps. Required multiplicative factors are 1.31 at 10 K, and 1.9 at 300 K. A larger deviation from the simulated subthreshold swing (SS) is found at 300 K when compared to 10 K; this indicates such screening of the gate potential is enhanced at higher temperatures as interface states become increasingly populated

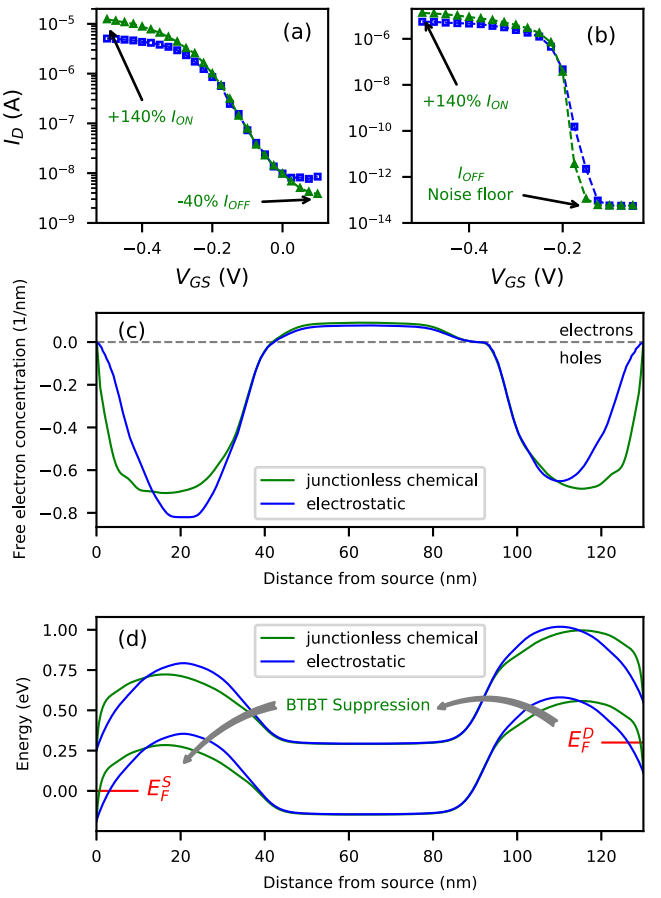

Fig. 3. Simulated current–voltage characteristics of p-type devices at temperatures of (a) 300 K and (b) 10 K for designs with either chemical (green) or electrostatic (blue) doping. (c) Free carrier concentration and (d) Band edges along the length of devices for an OFF state at 300 K. Gate length is 50 nm. Source Fermi level (E_F^S) is at 0 eV, and drain Fermi level (E_F^D) at 0.3 eV.

with electrons. Estimations of interface trap densities yield $D_{it} = 1.3 \times 10^{13}$ $cm^{-2}V^{-1}$ at 10 K, and $D_{it} = 3.7 \times 10^{13}$ $cm^{-2}V^{-1}$ at 300 K [13]. We note excellent agreement between experiment and simulation for OFF currents, I_{ON}/I_{OFF} ratio, and the onset of BTBT conduction ($V_{GS} \gtrsim 0$ V).

Fig. 3 compares the simulated electrical characteristics of devices using electrostatic and junctionless chemical doping at temperatures of (a) 300 K and (b) 10 K. The junctionless chemical doping concentration along the device has been adjusted to match the hole concentration in the reservoir along the drain extension (hole source), as shown in Fig. 3(c). Devices with junctionless chemical doping exhibit larger I_{ON}/I_{OFF} ratios when compared to those electrostatically doped. The fact that chemical doping potentials are distributed along the entire CNT results in band profiles that favor larger ON currents and tend to suppress BTBT in OFF states. Fig. 3(d) compares the CNT band profile along the device length for an OFF state. Junctionless chemical doping induces a steeper band profile near source and drain contacts, significantly reducing the width of the barrier holes must tunnel across to enter or exit the device near the leads Fermi level. This results in larger ON currents when compared to electrostatically doped devices with the same Schottky barrier height. Conversely, partial screening of the gate action by chemical doping results in a more gradual band profile on either side of the channel, which suppresses phonon-assisted BTBT that limits OFF currents at higher temperatures.

Practical implementations of chemical doping would bring about additional effects derived from impurity scattering not considered in this work. A previous study measured mobility reductions of a factor

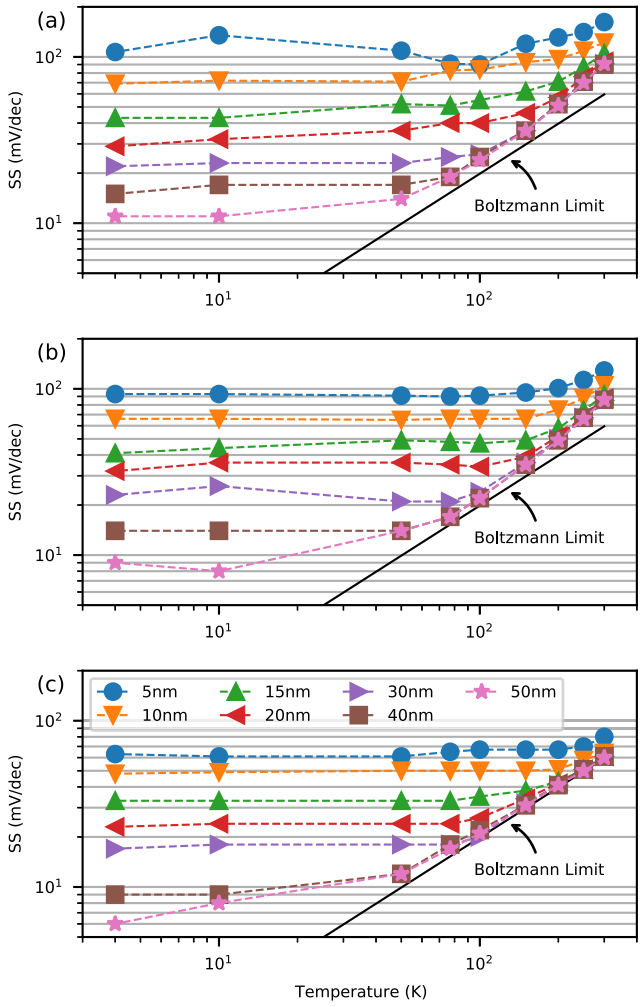

Fig. 4. Subthreshold swing (SS) versus temperature for devices based on 2 nm diameter CNTs with (a) electrostatic doping or (b) chemical doping, and (c) 1 nm diameter CNTs and chemical doping. Lengths reported in legend correspond to channel length.

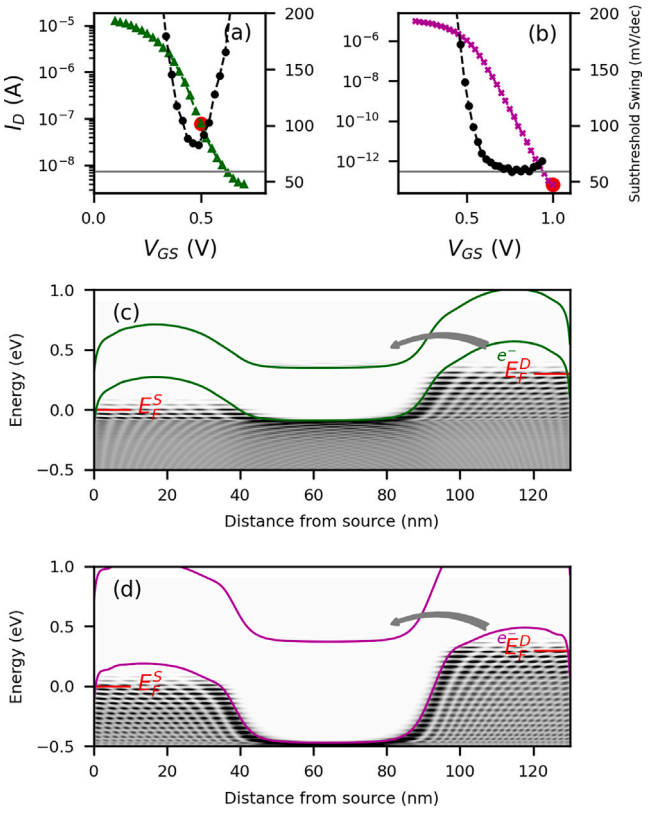

Fig. 5. Simulated current–voltage characteristics (left axis) and SS (right axis) of devices with chemical doping based on (a) 2 nm CNT, and (b) 1 nm CNT. Non-equilibrium electron occupation throughout devices based on (c) 2 nm CNT, and (d) 1 nm CNT. Horizontal lines in (a) & (b) indicate the Boltzmann limit; red circles indicate states plotted in (c) & (d). $L_G = 50$ nm. $T = 300$ K. Source Fermi level (E_F^S) is at 0 eV, and drain Fermi level (E_F^D) at 0.3 eV.

of 3 with respect to intrinsic mobility for CNTs with similar dopant concentrations [14]. Given the high intrinsic mobility of CNTs, the associated penalty to ON currents is expected to be low for short-channel devices. Another study found impurities to have a limited effect on the threshold voltage dispersion of CNFETs, and estimated short channel lengths to have a larger impact on effective carrier mobility than impurity scattering [15].

The band profiles shown in Fig. 3(d) induce significant state quantization at the top of the valence band along lead extensions and at the bottom of the conduction band in the channel, due to confinement along the transport direction. Oscillations in the density of states (DoS) with energy in these regions and variations in their alignment with varying gate voltage result in fluctuations in drain current along the BTBT branch ($V_{GS} > 0$ V in Fig. 2). This effect is more pronounced at lower temperatures, as state broadening induced by electron–phonon interactions dampens DoS oscillations.

The impact of SDT on the SS at varying gate length, temperature, and CNT diameter is illustrated in Fig. 4. Once again we find junctionless chemical doping to be advantageous: steeper slopes present in the band profiles near the channel in electrostatically doped devices result in enhanced SDT as the distance between source and drain extensions reservoirs is shorter than in junctionless devices. Such SS degradation is observed in devices with electrostatic doping at most gate lengths and temperatures, with largest deviations from their chemical doping counterparts occurring at shorter gate lengths and higher temperatures (Fig. 4(a)–(b)).

In contrast, Fig. 4(c) shows the case of devices based on CNTs with 1 nm diameter ($E_G \approx 0.85$ eV) and junctionless chemical doping. Greater electrostatic control is found to be exerted by the gate electrode in these devices, where the long-channel SS closely tracks the Boltzmann limit for temperatures $T \geq 77$ K. Owing to the intrinsically more favorable electronic structure of 1 nm diameter CNTs, SDT is significantly suppressed in these devices, with values below 65 mV/dec at room temperature for gate lengths of 10 nm and longer.

Overall, the electronic structure of 2 nm diameter CNTs results in devices with worse switching performance than their 1 nm counterparts. On one hand, larger SDT rates translate into larger SS at short gate lengths. On the other hand, the relatively small band gap of 2 nm CNTs imposes limits to both OFF currents and SS at temperatures $T \geq 100$ K. As illustrated in Fig. 3(c) and (d), OFF currents require phonon-assisted BTBT from the channel conduction band into the source extension's valence band; the separation in energy between these states requires inelastic phonon scattering processes to intervene in electron transport. OFF currents thus strongly depend on temperature, as can be observed in Figs. 2 and 3. The larger band gap in 1 nm diameter CNTs suppresses phonon-assisted BTBT to the source extension and allows for OFF currents several orders of magnitudes lower, as shown in Fig. 5(a)–(b).

On the opposite side of the channel, a different mechanism imposes a lower limit to SS. Fig. 5(c) shows the non-equilibrium electron occupation along the length of a chemically doped device based on a 2 nm CNT at a gate voltage near threshold ($V_{GS} \approx V_{Th}$). As gate–source bias increases, the channel conduction band begins to get populated with

electrons as it aligns with the valence band in the drain extension. Electrostatic control exerted by the gate electrode thus becomes limited by the screening provided by such free electrons for all subthreshold states, resulting in SS degradation. Fig. 5(a) plots the associated $I_D - V_{GS}$ characteristics, where the SS can be seen to increase with V_{GS} as the free electron population in the channel – and therefore the screening of the gate potential – increases. This effect is also exacerbated at higher temperatures, as illustrated in Fig. 4(b) by increasing deviations from the Boltzmann limit with temperature for $T \geq 77$ K.

Improved switching is enabled by 1 nm diameter CNTs, where the larger band gap suppresses electron population in the channel conduction band. Fig. 5(c)–(d) show states with similar electron population in the channel for devices based on 1 nm or 2 nm CNT, respectively. The onset of free electron gate screening is shifted from near threshold to OFF states with drain currents around 10^{-13}A, as indicated in Fig. 5(b).

4. Conclusion

CNFETs exhibit excellent electrical characteristics promising suitability for sub−5 nm nodes. However, the full potential of this class of devices has yet to be achieved through refinement of processing techniques and design co-optimization. Exploration of design parameters and physical analysis enabled by the use of quantum simulations offers insight into device operation at a wide range of temperatures and down to a few Kelvin. We find critical performance metrics of recently reported device structures may be significantly enhanced to achieve larger I_{ON}/I_{OFF} ratios and improved switching.

The use of junctionless chemical doping profiles is found to improve device performance when compared to electrostatic doping employed in recent test structures. Although realistic implementations of chemical doping would induce additional effects derived from impurity scattering, previous studies suggest their impact on performance would not be critical to the viability of CNFETs. The larger band gaps and reduced SDT rates intrinsic to 1 nm diameter CNTs result in improvements to both SS and OFF currents for all simulated devices, with ideal switching characteristics observed at room temperature for gate lengths of 15 nm or greater. In comparison, CNTs with 2 nm diameter are found to only provide competitive performance for channels longer than 40 nm, and at temperatures below 100 K. Results compiled in Fig. 4 provide theoretical limits to switching in technologically relevant CNFET structures and may serve as a guideline for future investigations. Combination of advances in processing with the insight offered by physical simulations holds the key for driving CNFETs designs to optimal performance.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

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