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Simulation-based study on characteristics of dual vertical transfer gates in sub-micron pixels for CMOS image sensors

Wook Lee [a,*], Seonghoon Ko [a], Jae Ho Kim [a], Yoon-Suk Kim [a], Uihui Kwon [a], HyunChul Kim [b], Dae Sin Kim [a]

[a] Computational Science and Engineering Team, Innovation Center, Device Solution Business, Samsung Electronics Co., Hwasung-si, Gyeonggi-do, Republic of Korea
[b] Semiconductor R&D Center, Device Solution Business, Samsung Electronics Co., Hwasung-si, Gyeonggi-do, Republic of Korea

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ABSTRACT

Recently dual vertical transfer gates (VTGs), used in sub-micron pixels with full-depth deep-trench isolation (FDTI), have demonstrated superior performance in CMOS image sensors such as improvement of full well capacity (FWC) and charge transfer, as compared to a single VTG. In this work, we investigate characteristics of both pixel schemes based on two design examples, which is carried out using extensive 3D TCAD simulation and automated multi-objective optimization flow with various photodiode implantation conditions satisfying certain design specifications. Simulation results reveal that dual VTGs better control electrostatic potentials along the charge transfer path like a 3D fin-shaped transistor. The enhanced gate controllability also makes the VTG off potential insensitive to the nearby doping concentrations, which is not the case for the single VTG pixel, and thus provides more room for boosting FWC in the photodiode design according to the Pareto front analysis.

1. Introduction

Among various sub-micron pixel architectures in CMOS image sensors, the unit cell that is composed of the single VTG with deep photodiode and separated by FDTI structure has gained increasing popularity due to many favorable sensor characteristics, such as high FWC and low crosstalk [1–3]. Recently the dual-VTG scheme has been successfully applied to a 0.6 μm pitch pixel for the first time, and achieved both FWC increase by 60 % and improved image lag as compared to the single VTG [4]. In this work, we analyze the physical origin of these performance gains by comparing each pixel design based on TCAD simulation.

Due to three dimensional nature of charge transfer from the deep photodiode to the shallow floating diffusion (FD) node via the VTG, optimization of these device elements in terms of the pixel layout and process conditions is extremely challenging, not to mention the other in-pixel transistors affecting all each other. Elaborate engineering of doping profile in the photodiode and around the VTG is required such that signal electrons should not see any potential barriers along the transfer path [5]. The deep-junction photodiode is built by a sequence of *n*-type implant with different energies up to a few MeV to ensure high FWC within a limited pixel area. The FWC is defined by the maximum amount of electrons that can be stored in the photodiode well, which can be expressed as.

$$\mathrm{FWC} = \frac{1}{q}\int C_{\mathrm{PD}}\,dV \approx \frac{C_{\mathrm{PD}}}{q}(\mathrm{PDMAX} - \mathrm{TGLSO}) \quad (1)$$

where C_{PD} is the photodiode capacitance. PDMAX is the maximum photodiode potential at full depletion, often referred to as pinning voltage [6], and TGLSO is the minimum shutoff potential when the VTG bias is low. This potential difference (PDMX – TGLSO) can be increased to maximize the FWC. In addition, the potential profile in the photodiode needs to be carefully tuned not to leave any residual electrons for excellent image lag performance.

2. Simulation

Fig. 1 shows schematics of each 2 × 2 pixel layout based on single and dual VTGs. The photodiode is formed deep in Silicon per pixel and separated by the FDTI structure except the center area occupied by the shared FD. The pixel is optimized with three design specifications; (1) the FWC needs to be maximized, or at least be larger than some threshold, e.g., >5000e-, (2) no residual electrons be sensed in the readout operation, (3) the potential hump on the transfer path, if any, be smaller than 100 mV when the VTG is on. Various implantation

* Corresponding author.
E-mail addresses: wook6.lee@samsung.com, wleegt@gmail.com (W. Lee).

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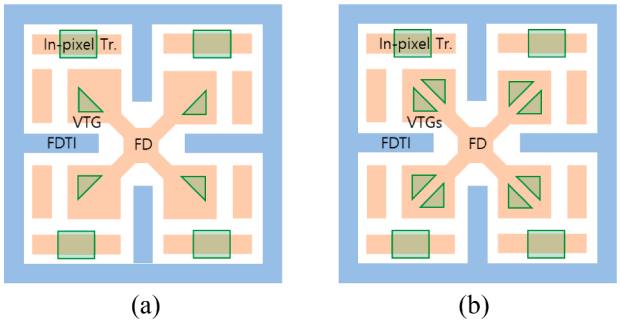

Fig. 1. Schematics of 2 × 2 pixel layout based on (a) single VTG and (b) dual VTGs.

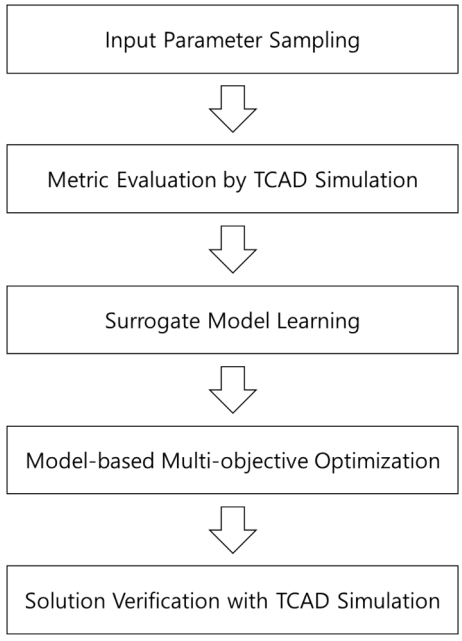

Fig. 2. Automated design flow of machine-learning based pixel optimization.

conditions, i.e., dose and energy, related to the photodiode and the adjacent VTG region, are used as input parameters, and optimization is performed using our in-house automated machine-learning based optimization framework with extensive 3D TCAD simulation to speed up the pixel design and explore the design space effectively [7,8].

As shown in Fig. 2, many TCAD datasets are first generated by Latin hypercube sampling method [9], together with parallel TCAD simulation. Several types of machine-learning models such as support vector machine, random forest, and neural network are trained using these datasets, and an ensemble of a few top-ranked models in the regression task is finalized as a surrogate model. Genetic algorithm [10] or differential evolution [11] is then used to search the optimal process parameters satisfying multiple objectives over the design space based on these surrogate models, and the obtained solution points are double-checked by TCAD simulation.

3. Result & discussion

Fig. 3 (a) shows the comparison of potential profiles for each pixel structure of single and dual VTGs, given the same implant conditions and gate voltage. The dual VTG is nothing but a three-dimensional fin-shaped transistor that controls the transfer of electrons from the deep photodiode to the FD node by exploiting the double vertical gates. Hence, the channel potential in between is better controlled by the gate

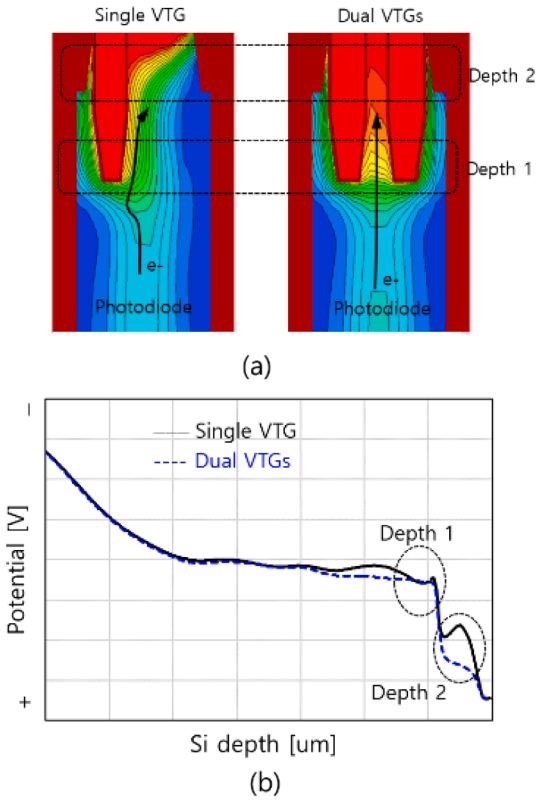

Fig. 3. Comparison of (a) potential profile and (b) electron transfer path in single- and dual-VTG pixels.

Table 1
Simulated electrical characteristics of pixel design examples given in Fig. 3.

Type	Single-VTG pixel	Dual-VTG pixel
FWC	6,250e-	9,202e-
Residual electrons	0	0
TGLSO	−0.04 V	−0.35 V
PDMAX	1.79 V	1.78 V
Max. Potential hump in Depth 1	61 mV	0
Max. potential hump in Depth 2	155 mV	0

voltage than the nearby doping profile. It can be seen that the dual VTG has higher potential values varying more smoothly in this transfer region including *Depth 1* and *Depth 2*, compared to the single VTG. The precise three-dimensional transfer path of electrons from the photodiode and the FD is traced based on the spatial potential gradients, and its potential variations as a function of Silicon depth are also compared in Fig. 3 (b). Electrical characteristics of both pixel schemes are summarized in Table. 1. Not only does the dual-VTG pixel exhibit the better transfer capability as discussed previously, but also FWC increases by 3000e- mainly due to different TGLSO levels.

This FWC increase in the dual-VTG pixel can be better understood by further analyzing full optimization results. As a reference, Fig. 4 shows the result of the single-VTG pixel. Each data point represents one solution with different optimal implant conditions satisfying the aforementioned target specifications. It is important to note that the maximal FWC in the single VTG, which can be achieved without the transfer problem, is basically limited to some extent, regardless of combinations of the implant conditions for the photodiode. In other words, if one attempts to increase the *n*-type doping concentrations of the photodiode to boost FWC beyond the Pareto front in Fig. 4 (a), the transfer characteristics are likely to be degraded out of specification, or since TGLSO also increases proportionally with PDMAX as presented in Fig. 4 (b), it eventually results in no much gain in FWC.

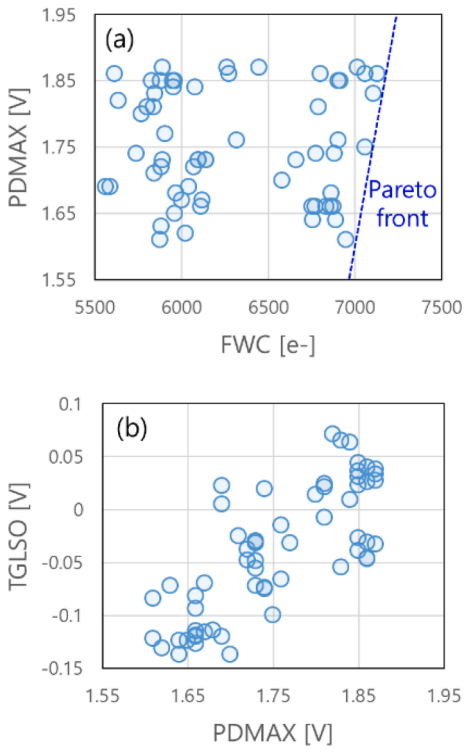

Fig. 4. Pareto front analysis of single-VTG pixel: (a) FWC vs PDMAX (b) PDMAX vs TGLSO.

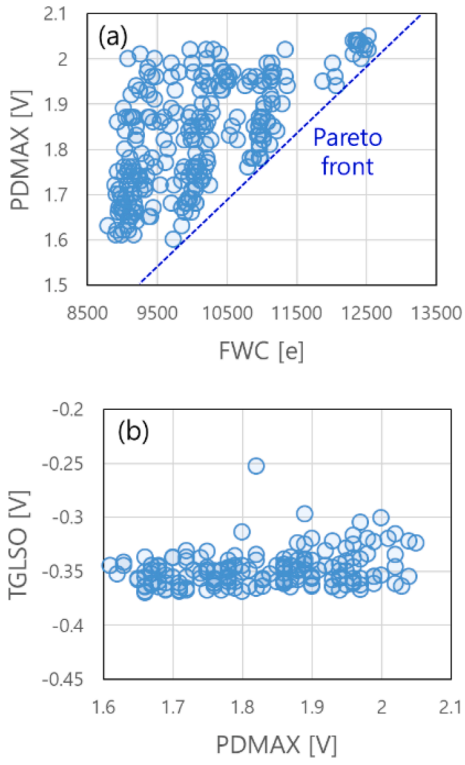

Fig. 5. Pareto front analysis of dual-VTG pixel: (a) FWC vs PDMAX (b) PDMAX vs TGLSO.

Interestingly, this tradeoff can be greatly alleviated in the case of the dual-VTG pixel. Due to the enhanced gate controllability in the dual VTG, TGLSO does not change much around a potential of −0.35 V even with diverse input implant conditions as shown in Fig. 5 (b). However, PDMAX is still dominated by the photodiode net-doping and so it can be controlled independent of TGLSO as illustrated by the Pareto front in Fig. 5 (a). As a result, one can design the dual-VTG pixel to have a higher FWC without sacrificing the charge transfer characteristics.

4. Conclusion

In summary, we conduct comparative study on electrical characteristics of single- and dual-VTG based sub-micron pixels using 3D TCAD simulation and automated multi-objective optimization flow. The Pareto front analysis based on massive simulation data shows that dual VTGs can greatly improve the sensor characteristics in terms of both FWC and charge transfer because of the enhanced gate controllability, which alleviates the conventional performance tradeoff that presents in the single-VTG pixel.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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