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SPICE compatible semi-empirical compact model for ferroelectric hysteresis☆,☆☆

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ABSTRACT

This paper reports a semi-empirical, SPICE compatible and computationally efficient compact model for ferroelectric capacitors (Fe-CAP) description. This compact model is inspired by the Jiles–Atherton model of ferromagnets, which features significantly smaller computational effort than other state-of-the-art models. It successfully computes the evolution of the memory window and hysteresis of ferroelectric capacitors for any arbitrary signal. We have successfully calibrated this model with the experimentally characterized polarization switching dynamics of fabricated 10 nm silicon-doped hafnium oxide based Fe-CAP.

1. Introduction

Due to its CMOS compatibility and scalability, hafnium oxide (HfO_2)-based ferroelectric field effect transistors (FeFETs) – transistors with a ferroelectric layer embedded in the gate – are investigated as potential next-generation nonvolatile memories (NVMs) [1–5]. Successful integration of FeFETs into advanced technology nodes has triggered the research interest among scientists for deploying it with embedded NVM applications. Henceforth, it is necessary to have a simulation program with integrated circuit emphasis (SPICE)-compatible, computationally efficient compact model to investigate the performance of ferroelectric capacitors for large-scale integration. There have been numerous studies on compact model generation for Fe-CAPs, starting with the phenomenological Landau equation, which describes the ferroelectric behavior by a power-law dependence of polarization and voltage [6]. However, this relationship is not always physically achievable. Moreover, applied FeFET memory models that base on the Preisach model are computationally demanding, which limits their applications for large circuit implementation, such as neuromorphic systems [7,8]. Here, we present a computationally efficient ferroelectric model based on the Jiles–Atherton equations, which is Verilog-A compatible and that reproduces the experimental results with high accuracy.

2. Experimental

For experimental comparison, a 10 nm ferroelectric Si:HfO_2 was prepared. After the initial deposition of a TiN bottom electrode, the Si:HfO_2 layer is deposited using atomic layer deposition, with a Hf:Si cycling ratio of 16:1. After the deposition of the TiN top electrode, the film is crystallized using rapid thermal annealing. Capacitors are formed by Ti/Pt shadow mask deposition and subsequent wet etching. Dynamic hysteresis measurements are performed at 1 kHz using an *Aixacct TF3000 Analyzer*. The metal–ferroelectric–insulator–semiconductor (MFIS) capacitor was produced in a similar manner, except for the TiN bottom electrode. Here, a chemical oxide was grown instead.

The ferroelectric compact model is coded in Python 3 as well as Verilog-A, while the simulation was done in Spectre 6.1.8 circuit simulator using the Verilog-A code. It is a ferroelectric capacitor model only, hence it can be included onto a BSIM model. The ferroelectric thickness, permittivity, and fitting parameter are defined within the model file, or these can be included during simulation. It has two access ports (in and out) for the circuit simulation. For circuit simulation, a ferroelectric capacitor (symbol) is called in the schematic editor, then a supply voltage and a 1 Ohm resistance are connected in series. The change in current at the entry node is measured as a function of the supply voltage. The transient simulation results are collected. The MFIS

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capacitor model was coded in Python 3 using an analytical transistor model [9].

3. Modeling ferroelectric hysteresis

For a deeper understanding of a ferroelectric device, it is essential to be able to model it for all possible conditions of operation. For such a model, a semi-empirical model based on physical equations that can correlate material properties with voltage–current characteristics while giving expected results, was implemented. Ferroelectric behavior is usually solved by calculating the polarization (charge), from which one has to use the derivative to obtain the current characteristics of the device.

Diverse models attempt to describe this behavior, but are showing disadvantages: Hyperbolic tangent based models are only compatible with full-loop operation [10]; Preisach density based models require a large set recurring time-series parameters [8,11,12] while finally, models based on nucleation limited switching [13] have the same problem and are more complex to be extended to arbitrary signals [14–16].

For this reasons, a model developed to described ferromagnetic films based on the *Langevine* function, commonly referred to as the Jiles–Atherton model (paying credits to the original authors) [17] was chosen. Such a model is compatible with circuit simulators, supports various operation points and can be adapted to different devices, since it bases on semi-empirical parameters. Nonetheless, a ferroelectric analogue has not been proposed so far. By implementing the displacement field D (see Eq. (1)), contributing polarization P_0 from the material, the permittivity of free space ϵ_0, the applied electric field E and the Langevine equation (see Eq. (2)), which relates the Brillouin equation to a countless amount of domains, one can create a solvable equation.

$$D = P_0 + \epsilon_0 E \tag{1}$$

$$L(x) = coth(x) - \frac{1}{x} \tag{2}$$

In contrast to the ferromagnetic model (see Eq. (3)), which is based on the magnetic field H and the magnetization M, the sign needs to be inverted in case for ferroelectrics (see Eq. (4)) [18] due to the definition of D (see Eq. (1)). Here, α denotes the inter-domain coupling in the material. A more extensive discussion of the physical origin of this parameter can be found in [17].

$$H_{eff} = H + \alpha M_0 \tag{3}$$

$$D_{eff} = D - \alpha P_0 \tag{4}$$

The polarization has to account for the hysteretic (or irreversible) and anhysteretic behavior, as such, the flow of the solution is split in two: The Langevine equation is used to solve the anhysteretic polarization P_{anh} (see Eq. (6)), while the irreversible polarization P_{irr} (see Eq. (7)) is solved by accounting for the whole polarization P and subtracting the anhysteretic part (see Eq. (5)). The total polarization inside the device is the sum of the ferroelectric and dielectric contributions based on the relative permittivity.

$$P = (1 - c)P_{irr} + cP_{anh} \tag{5}$$

$$P_{anh} = P_S L\left(\frac{D_{eff}}{\gamma}\right) \tag{6}$$

$$\frac{dP_{irr}}{dt} = \frac{(P_{anh} - P_0)}{sign\left(\frac{dD}{dt}\right)k - \alpha\left(P_{anh} - P_0\right)}\frac{dD}{dt} \tag{7}$$

The proposed model uses semi-empirical values obtained by fitting measured devices to describe physical quantities, as shown in Fig. 1 for the herein described model. Such a fitting approach allows for flexibility depending on the measured results. Conventional parameters such as the dielectric constant and thickness of the layer are plugged

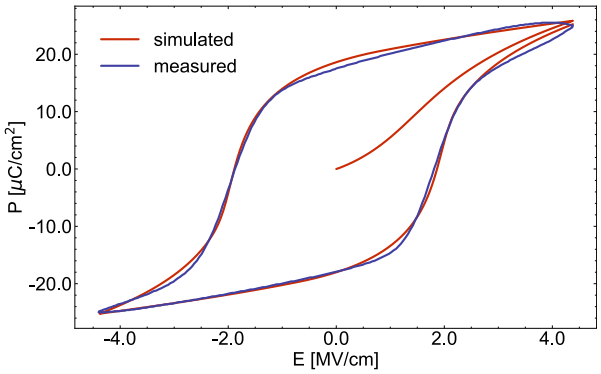

Fig. 1. Comparison of the polarization response of the simulated and measured ferroelectric capacitor. The simulation parameters were optimized via fitting to the experimental data. Minor differences are apparent due to the presence of leakage current in the measured hysteresis. Model parameters are P_S = 47.2 μC/cm², α = 0.70, k = 2.04*10⁻⁵ C/cm², γ = 1.74*10⁻⁵ C/cm², c = 0.04, $\epsilon_0\epsilon_r$ = 9.90*10⁻¹⁵ F/m.

in directly. The parameter that accounts for the amount of polarization due to ferroelectric domains compared to the internal polarization is expressed by c. The saturation polarization P_S is the polarization at which the polarization-voltage curve would saturate. The parameter k denotes the pinning parameter, γ the shaping parameter, c the proportionality factor, and α, as mentioned before, the inter-domain coupling constant.

As shown in Fig. 2a, the model shows sub-loop behavior when applying a triangular drive voltage with varying voltage amplitude. When investigating the influence (see Fig. 2b–e) of the different parameters (c, k, γ, α, and ϵ_r), a better understanding of their meaning is obtained. While c mainly affects the backswitching behavior thus changing between a hard or soft ferroelectric response, k and γ affect the coercive field distribution. The former changes the mean coercive field, thus shifting the behavior towards sub-loop, whereas γ affects the width of the coercive field distribution. Consequently, the slope of the hysteresis curves around the coercive field changes. The influence of the inter-domain coupling constant α, on the other hand, has only a minor influence, compared to the previous parameters, changing the slope of the hysteresis slightly. ϵ_r affects only the slope in the saturated region and not the coercive field, as expected.

3.1. Implementation in VerilogA

As shown in Fig. 3a, the simulation using Verilog-A in Spectre converges numerically stable and the displacement current and displacement current peaks are clearly observable. Furthermore, Fig. 3b visualizes the sub-loop functionality of the model. Consequently, this model can be used with arbitrary signals and the ferroelectric capacitor compact model can be introduced into various circuit simulations.

As this model resembles a complete ferroelectric capacitor and is able to perform arbitrary signal simulation, it can be directly used in conjunction with other device compact models to simulate memory or neuromorphic circuits based on Fe-Cap, ferroelectric random access memory (FeRAM) or FeFET devices.

3.2. MFM and MFIS capacitors

Especially for FeFET devices, the ferroelectric compact model is of major importance to simulate device behavior, to deepen the understanding on the underlying dynamics, and to improve device design. The major difference to the above simulated metal–ferroelectric–metal (MFM) capacitor is that the FeFET gate stack is described by a MFIS stack. Such a device can be modeled as an ideal ferroelectric capacitor (i.e. no effects due to the electrodes) on top of a regular transistor. This

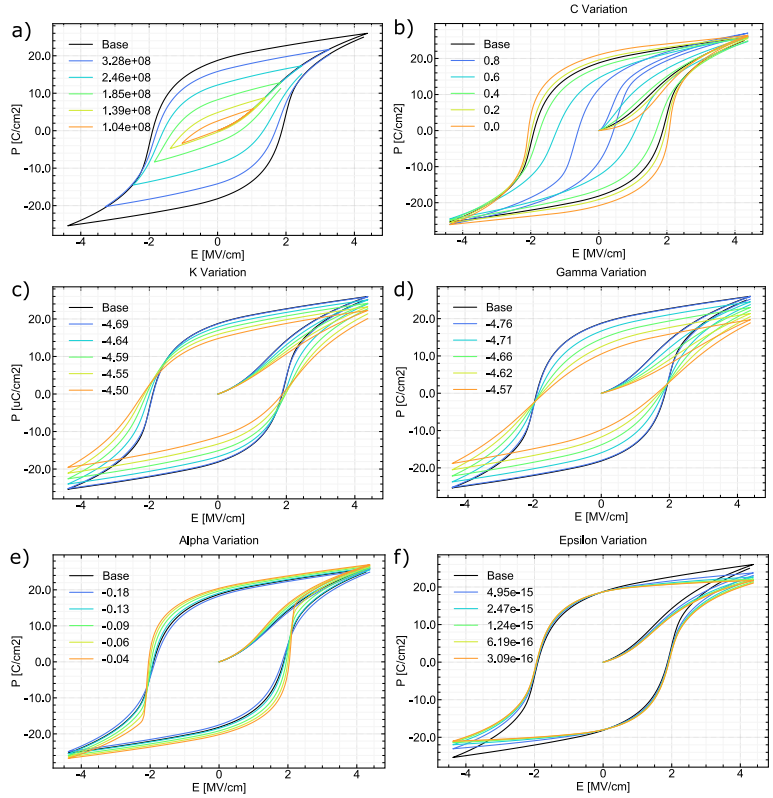

Fig. 2. Influence of the parameters in the Jiles–Atherton-based ferroelectric model. Sub-loop behavior is observed for different voltage amplitudes (a). Influences of the model parameters on the hysteresis shape are provided in (b) to (e). k, γ and α values are provided in exponent (10^x). Influence of the constant relative permittivity is given in (f).

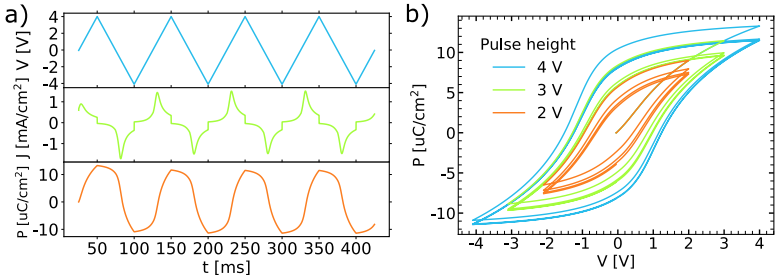

Fig. 3. Verilog-A based simulation of a ferroelectric capacitor. The current and polarization response over time is shown for multiple triangular voltage pulses in (a). The sub-loop behavior is illustrated in (b) for different voltage amplitudes.

approach decouples the phenomena in the device, allowing the use of a capacitor model with a preexisting, e.g. a proprietary, transistor model. A simple MFIS capacitor can be described analytically by Eq. (8) based on the potential drop across each layer. Here, V_{ext} is the externally applied voltage, Φ_{MS} the potential resulting from metal–semiconductor band alignment, Φ_S the surface potential of the semiconductor, V_{IL} the voltage across the interface layer and V_{FE} the voltage across the ferroelectric layer. These terms are defined analogously to the common analytical metal-oxide–semiconductor model [9]. Due to the polarization, the term for the total charge Q_{tot}, however, is modified (see Eq. (9)), resulting in a dependence on V_{FE} in Eq. (8). Q_{fix} denotes to the fixed charges in the interface layer, whereas ϵ_{FE} and t_{FE} resemble the relative permittivity and thickness of the ferroelectric respectively.

$$V_{ext} = \Phi_{MS} + \Phi_S(V_{FE}) + V_{IL}(V_{FE}) + V_{FE} \tag{8}$$

$$Q_{tot} = Q_{fix} + P(V_{FE}) + \frac{\epsilon_{FE}}{t_{FE}} * V_{FE} \tag{9}$$

Based on these equations, the capacitance response of the stack for an arbitrary signal can be calculated. The simulated response (see Fig. 4) behaves qualitatively very similar to the experimentally measured capacitance-voltage (CV) curve. In both cases peaks related to the switching of the ferroelectric are observable at similar voltage amplitudes. Nevertheless, the measured CV curve is also affected by interface traps and trapped charges. To simulate these additional contributions, more refined transistor models are required, which are available for circuit simulations in different technology nodes.

While this combination nicely describes MFIS capacitors and with extended transistor models FeFETs as well, the model, like the other aforementioned models for ferroelectrics, does not contain information on the lateral distribution of domains in the ferroelectric layer. In case of the back-end-of-line (BEoL) integrated FeFETs [19], this is not of relevance due to the metal layer in between the channel and the ferroelectric capacitor. In front-end-of-line (FEoL) integrated FeFETs, however, recent results have highlighted the importance of lateral distribution due to the formation of current percolation paths [20,21]. Consequently, FEoL FeFET models will require a computing-efficient extension of the transistor model to reflect this in dependence on the polarization state generated by the Jiles–Atherton based ferroelectric model.

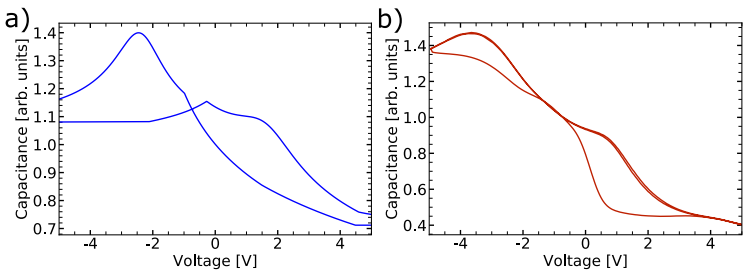

Fig. 4. Comparison of modeled (a) and measured (b) CV curves of an hafnium oxide-based MFIS capacitor. Notice the hysteresis due to the polarization change inside the device.

4. Conclusion

In conclusion, we demonstrated that the ferromagnetic Jiles–Atherton model can be transferred to a ferroelectric model. This semi-empirical model allows for arbitrary signals, enables sub-loop operation, and does not require extensive history parameters. Furthermore, the integration of this model into Verilog-A and a Spectre circuit simulation environment has been demonstrated. Finally, it has been explained how this model can be applied for the simulation of FeFETs, and the analytical integration into a MFIS capacitor model has been proposed.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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