Solid-State Electronics 200 (2023) 108551

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Performance of vertical gate-all-around nanowire p-MOS transistors determined by boron depletion during oxidation

Chiara Rossi [a,*], Alexander Burenkov [a], Peter Pichler [a], Eberhard Bär [a], Jonas Müller [b], Guilhem Larrieu [b]

[a] Fraunhofer Institute for Integrated Systems and Device Technology (IISB), Erlangen, Germany
[b] LAAS-CNRS, Université de Toulouse, Toulouse, France

ARTICLE INFO

The review of this paper was arranged by "Francisco Gamiz"

Keywords:
Nanowire FET
3D TCAD
Process simulation
Device simulation
Oxidation
Boron segregation
Junctionless transistors
Gate-all-around

ABSTRACT

Vertical junctionless gate-all-around nanowire transistors show excellent electrical performance and can be fabricated using a top-down approach in conventional CMOS process technology. Thinning of the nanowires to the desired diameter is obtained by sacrificial wet oxidation. Then, the gate oxide is grown by dry oxidation. These oxidation steps deeply affect the doping distribution in the nanowire due to dopant segregation and self-interstitial injection, especially for p-type dopants. This effect is more pronounced in 3D nanostructures with respect to bulk devices, due to geometry. Modeling the resulting doping distribution is a prerequisite for understanding the electrical properties of the devices and exploring their potential for optimization. In this work, 3D TCAD process and device simulations were performed using Synopsys Sentaurus and the results are compared with experimental data of devices fabricated at CNRS-LAAS. The impact of the implemented process and device models and their capability to predict nanowire properties and device behavior is assessed.

1. Introduction

The gate-all-around (GAA) nanowire (NW) field-effect transistor (FET) represents one of the most promising candidates for the Power-Performance-Area-and-Cost scaling that replaced Moore's law. GAA-NW-FETs show excellent performance, including a great immunity against short-channel effects and, thanks to their 3D layout configuration, can enhance integration and overcome some physical limitations resulting from 2D layout, such as contact placements and interconnect routing congestion [1–7]. Vertical GAA-NW-FETs can be fabricated using a top-down approach with conventional processes and very good control on dimensions and localization. Moreover, the gate length is given by the thickness of the deposited gate material, without the need of high-resolution lithography [8,9]. Thermal oxidation is a key process for the nanowire fabrication. For silicon nanowire, it can be used to shrink the diameter, remove residual damage from the etch process and to grow the gate oxide. Thermal oxidation is also used in SiGe nanowire fabrication to obtain core–shell structures, exploiting selective oxidation of the Si element of SiGe alloys and germanium condensation [10–13].

During sacrificial oxidations of silicon nanowires for diameter thinning as well as during gate oxide growth, dopants segregate into the growing oxide and self-interstitials are injected into silicon [14,15]. Unlike for the case of oxidation of a bulk planar surface, in silicon nanowires, the self-interstitials cannot diffuse efficiently into the bulk. This increases dopant diffusion and segregation loss in the nanorod while the resupply of dopants from the bulk is less effective due to device geometry. With the inhomogeneous dopant distribution in the nanowire deeply affecting the electrical characteristics and performance of junctionless GAA-NW-FETs, dopant diffusion and segregation during oxidation needs to be correctly modeled.

This work discusses 3D simulations of the full process flow for the fabrication of vertical nanowire p-MOS transistors, including the sacrificial oxidation step, with the Sentaurus Process program of Synopsys. Subsequent 3D device simulations, performed with Sentaurus Device, are compared with experimental data of devices fabricated at CNRS-LAAS, obtained by a large-scale CMOS compatible manufacturing process. Firstly, the vertical channel was fabricated by a top-down approach on 4-inch (100) wafer of boron-doped silicon. Dense circular nanopillars of negative resist were patterned by electron beam lithography [16,17] and transferred onto the substrate by anisotropic reactive ion

* Corresponding author at: Fraunhofer Institute for Integrated Systems and Device Technology (IISB), Schottkystraße 10, 91058 Erlangen, Germany.
E-mail address: chiara.rossi@iisb.fraunhofer.de (C. Rossi).

https://doi.org/10.1016/j.sse.2022.108551

Available online 30 November 2022

etching (RIE) resulting in 210 nm high vertical silicon nanowires. Wet thermal oxidation at 850 °C grew 14 nm of sacrificial oxide that was selectively removed from the device in buffered oxide etchant. A second dry oxidation at 725 °C then created a thin gate oxide of nominally 5 nm on the NWs. The oxide on top of the substrate and NWs was removed by dry plasma etching. A 10 nm thick Pt layer was deposited and annealed by rapid thermal annealing (RTA) at 500 °C for 3 min forming Pt-silicide (PtSi). Unreacted Pt was selectively etched in aqua regia. The entire device was covered with a spin-on-glass (SOG) that was etched down to the middle of the channel height, creating the first dielectric spacer [18]. The metallic GAA layer was defined by depositing 18 nm of Cr [9,19,20]. A second SiO_x spacer was defined up to the PtSi contacts. The bottom contacts and gate layer were connected to the surface with vias filled by a 400 nm thick aluminum deposition, also covering the PtSi top contacts. Selective wet chemical Al etch-back was used to define contact pads. Finally, an RTA process under forming gas atmosphere of N_2/H_2(4 %) at 200 °C for 4 min passivated interfacial defects.

2. 3D TCAD simulation of boron segregation during oxidation

TCAD simulation of the process flow used for device fabrication at CNRS-LAAS started with the geometrical definition of a silicon nanowire, on a silicon substrate, with a diameter as obtained by the initial etching (Fig. 1.a). The whole structure is initially homogeneously doped with boron with a concentration of $3.5 \bullet 10^{19}$ cm^{-3}. The first sacrificial wet oxidation (850 °C, 5 min) was simulated and the resulting structure is shown in Fig. 1.b. After the sacrificial oxide stripping (Fig. 1.c), dry oxidation for gate oxide formation (725 °C, 20 min) was performed and the result is reported in Fig. 1.d. Since the oxidation rate depends on the silicon orientation, a diamond-like shape in the nanowire cross-section is expected. This peculiar cross-section shape was initially observed in TCAD simulations also. However, SEM images of nanowires after oxidation like in Fig. 2 always show circular shapes. The circular cross-section was also reported in literature by previous works [21–24]. A possible explanation of this phenomenon has been reported by Ye *et al.* [21]: Due to the increased energy barrier against oxidation of the Si-Si bond at the edges, oxidation at edges is slower than that far from edges. As the oxidation proceeds and the regions far from edges are segmented into additional and finer adjacent surfaces, the energy at the center of the adjacent surfaces increases to the same high value as that at the edge. The same oxidation rate is obtained all around the outer surface of nanowire, leading to a circular shape. The reproduction of the circular shape could finally be obtained also in TCAD simulations, as shown in Fig. 1.e, but required a suitably fine mesh for the nanowire.

The simulated final doping distribution after the two oxidation steps is reported in Fig. 3 for two different nanowire geometries (final diameters of 37 and 28 nm). The doping concentration was computed using the *ChargedPair* diffusion model and the three-phase segregation model [25] with the parameter set from Sentaurus TCAD *AdvancedCalibration S-2021.06*. Process simulations show that the doping distribution in the nanowire changes considerably during the oxidation steps. In particular, it is lowered by about one order of magnitude in comparison with the initial dopant concentration.

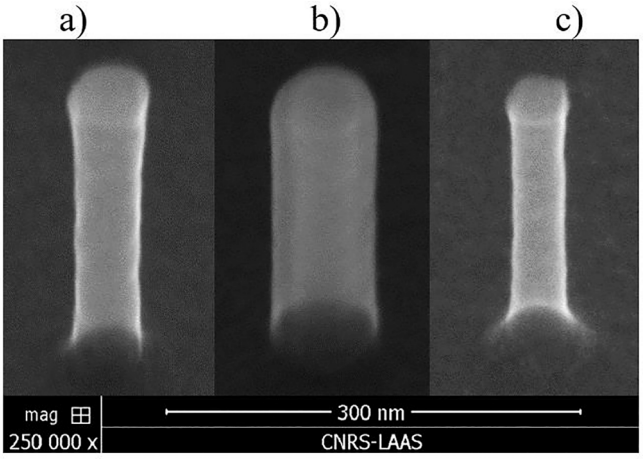

Fig. 2. SEM images of nanowires fabricated at CNRS-LAAS: a) initial nanowire after etching, b) oxidized nanowire after sacrificial wet oxidation, c) nanowire after oxide stripping. The nanowire has a circular shape in the cross-section.

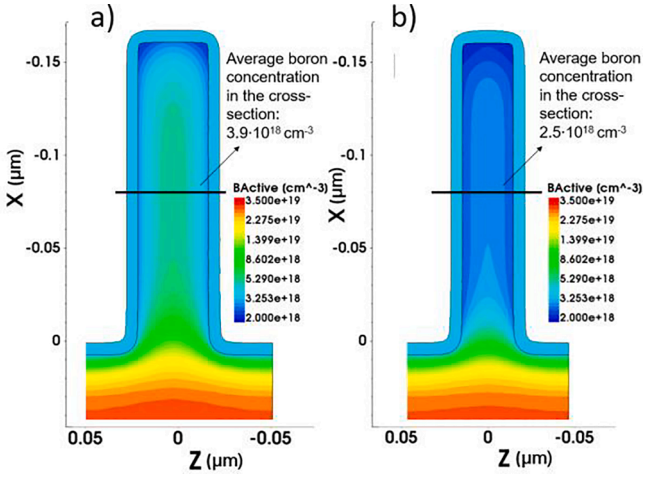

Fig. 3. Electrically active doping concentration in nanowires after sacrificial wet oxidation and gate dry oxidation for two different nanowire diameters: a) 37 nm, b) 28 nm. The graphs show a 2D cut-plane of the 3D simulated structures.

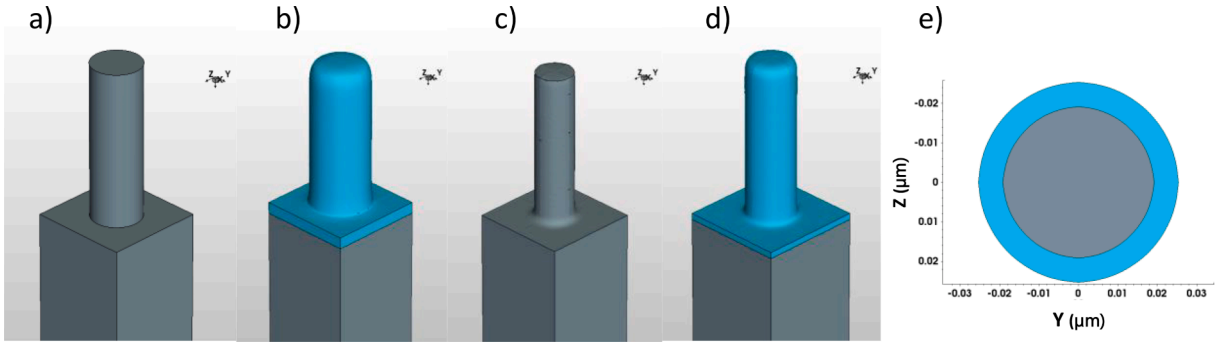

Fig. 1. a) Initial structure after etching of the nanowire; b) nanowire after sacrificial wet oxidation (oxide in light blue); c) thinned nanowire after oxide stripping; d) nanowire after dry oxidation for gate oxide growth; e) cross section of the nanowire after gate oxidation. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Moreover, the decrease is more pronounced for thinner nanowires. In fact, for smaller nanowire diameters, the surface-to-volume ratio increases and so a higher fraction of the total number of dopants diffuses out from the silicon nanowire into the oxide. Plus, for thinner nanowires, the area through which the dopants can diffuse from the highly doped bulk region is smaller, so the resupply of dopants is increasingly suppressed. Thus, the effect of boron depletion will be even more prominent for future device generations.

3. Results of 3D device simulations and comparison with experimental data

Starting from the structure after dry oxidation, as depicted in Fig. 2.d and Fig. 3, the next steps of the fabrication of GAA-NW-FETs were subsequently simulated. The gate oxide at the bulk surface and nanowire top was anisotropically etched and nickel was anisotropically deposited there. Silicidation was then simulated. Models for platinum silicide formation are not available in Sentaurus Process, for this reason nickel silicide was selected. During device simulations, the correct work function for platinum silicide was imposed at source and drain contacts. Convergence of the silicidation simulation posed some challenges, and a mesh adjustment was needed. Moreover, silicidation simulation had to be stopped before the total consumption of the metal to avoid fatal errors with a stop of execution. The next process steps simulated were the deposition of spacers and the gate metal layer. The latter defines with its thickness of 18 nm the gate length. The final simulated structure, ready for 3D device simulations, is presented in Fig. 4. For comparison, a SEM image of a fabricated GAA-NW-FET is presented in Fig. 5.

Fig. 6 reports the transfer characteristic obtained by device simulation of the GAA-NW-FET with a diameter of 37 nm, compared with experimental data. For a better visualization, only each second data point of the measured characteristic is shown. The drain voltage is −0.6 V with the source at 0 V. As gate oxide thickness, 5 nm was taken as determined experimentally, and the gate metal work function was set to 3.5 eV. The experimental data exhibit a higher subthreshold swing (147 mV/dec) compared with simulation results (90 mV/dec) obtained with *AdvancedCalibration S-2021.06* parameters. To investigate the reason behind this mismatch, different parameters were varied in TCAD simulations. The starting point was the analysis of the doping distribution in the nanowire. Fig. 6 shows, in addition to the I–V curve obtained for the doping distribution resulting from process simulation (Fig. 3.a), simulation results for nanowires with different doping concentrations. Namely, these doping distributions were obtained by multiplying or dividing the doping distribution obtained after process simulation with certain factors. The threshold voltage of the transistor changes considerably already for factors lower than 2. Moreover, the doping concentration also changes the subthreshold slope. The simulated threshold

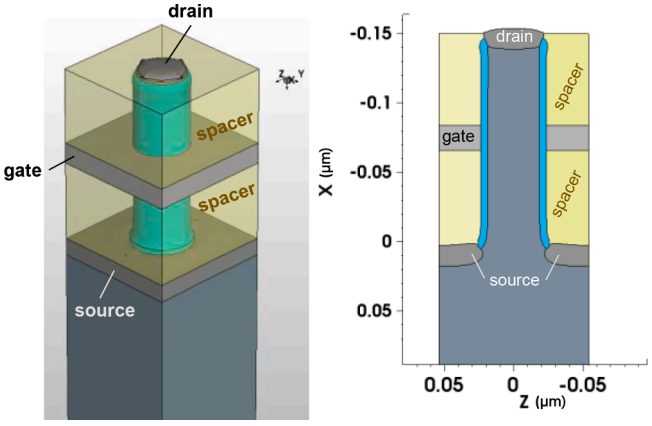

Fig. 4. Final 3D structure of GAA-NW-FET at the end of process simulation, on the right: cross section.

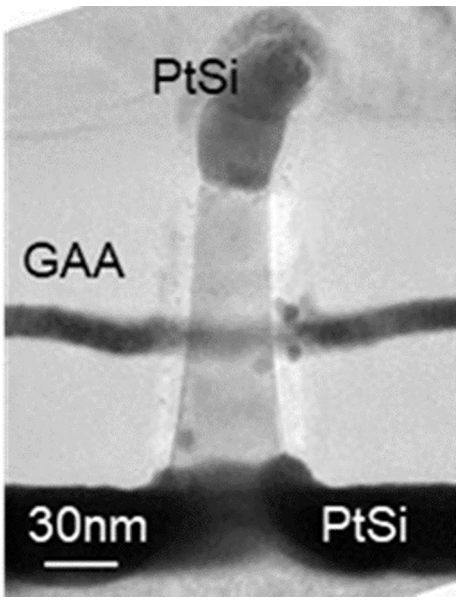

Fig. 5. TEM image of vertical GAA-NW-FET [15] fabricated at CNRS-LAAS.

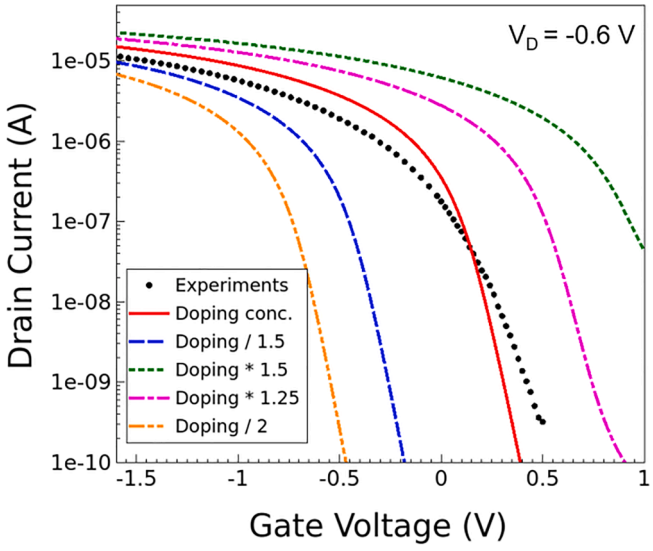

Fig. 6. Simulated I-V characteristics (NW diameter of 37 nm) for different doping distribution and experimental I-V curve. "Doping conc." refers to the doping concentration as plotted in Fig. 3.a.

voltage and subthreshold slope as a function of doping multiplication factor are reported in Fig. 7. This confirms the importance of a precise modeling of boron segregation in nanowires. By increasing the doping concentration, a subthreshold slope as in the experiments can be obtained on the cost of a threshold voltage shift in direction of positive gate voltages. A second influence investigated comes from the models used for the source and drain contacts. Platinum silicide has a work function of about 4.9–5.2 eV [26]. Fig. 8 shows the effect of the silicide work function on the characteristics. It has virtually no influence on the threshold voltage or subthreshold slope but a big impact on the on-current. Another parameter that was studied is the concentration of charges at the silicon-oxide interface, which modifies the threshold voltage as it can be seen in Fig. 9. In summary, these results show that the main influence on the subthreshold slope comes from the doping of the nanowire, whereas the threshold voltage is affected by both the doping and interface charges. This means that boron depletion during oxidation plays an important role in the transistor behavior at and below

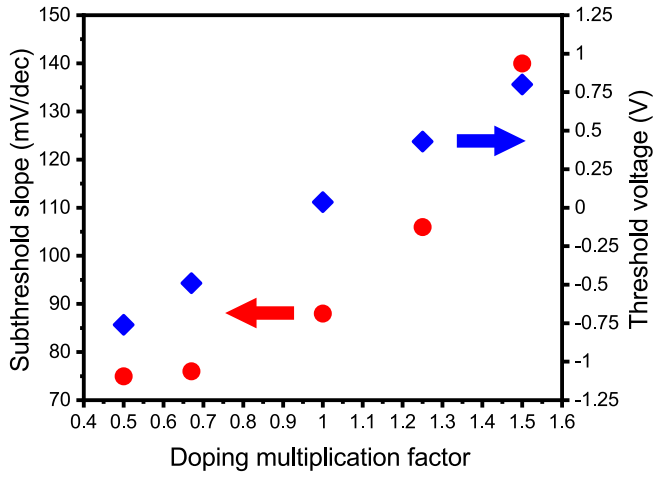

Fig. 7. Simulated subthreshold slope and threshold voltage as a function of the doping multiplication factor, i.e. the factor by which the doping distribution obtained by process simulation was multiplied before being used for device simulation.

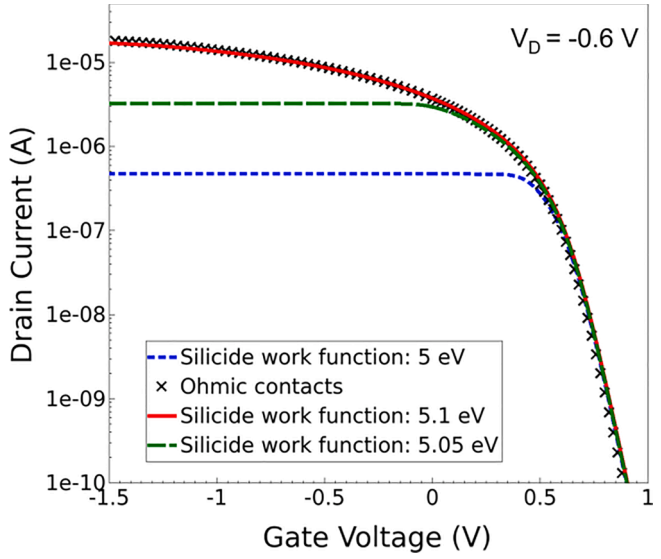

Fig. 8. Simulated I-V characteristics (NW diameter of 37 nm) for different silicide work functions. The doping concentration from process simulation is considered.

threshold. In addition, a change of the gate metal work function would result in a rigid shift of the transfer characteristics along the gate voltage axis.

Fig. 10 reports a comparison of the experimental data and TCAD simulations for a drain voltage of −0.6 V. The simulated I-V curves in Fig. 10 were obtained using a gate metal work function of 3.5 eV and interface charges with an area density of $3\bullet10^{12}$cm^{-2}. The latter appears high considering the forming gas annealing performed and needs to be further investigated. To obtain the experimental subthreshold slope, the doping had to be multiplied by a factor of 1.5. The impact of the oxide thickness on the I-V characteristics is also shown. Considering that the increase of oxide thickness is 20 %, the effect on the transistor behavior is rather low. Experimental results do not show a flat current curve for negative gate voltages, so a silicide work function of 5.1 eV was used. Thanks to these results, we can conclude that TCAD model parameters for diffusion and segregation still need to be improved for a better agreement to the measured electrical data, as the doping distribution in the nanowire appears currently underestimated. In order to obtain a

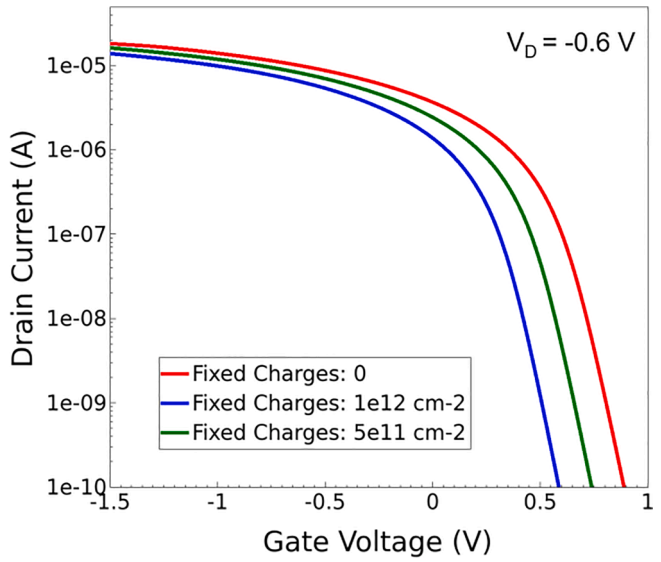

Fig. 9. Simulated I-V characteristics (NW diameter of 37 nm) for different charges concentration at silicon-oxide interface. The doping concentration from process simulation is considered.

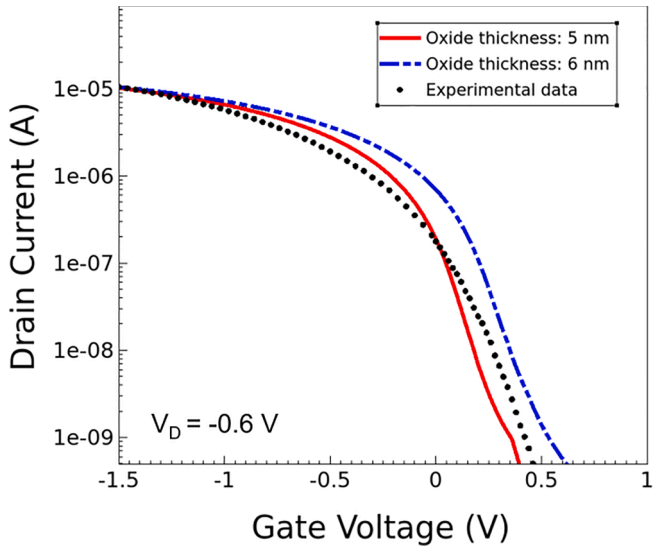

Fig. 10. Comparison of experimental and simulated I-V characteristics (NW diameter of 37 nm). Parameters for simulated curves: gate metal work function of 3.5 eV, interface charges of $3\bullet10^{12}$ cm^{-2}, doping multiplied by 1.5.

more precise estimation of doping concentration in 3D nanostructures, diffusion and segregation parameters need to be recalibrated.

4. Conclusion

We reported on results of full 3D TCAD process and device simulations of vertical junctionless GAA-NW-FETs, with particular emphasis on the effect of boron depletion after oxidation. Vertical nanowires were fabricated at CNRS-LAAS exploiting wet sacrificial oxidation for the thinning of the nanowires. Reproduction of the circular shape of the nanowire cross section after oxidation, as observed experimentally, was achieved in TCAD simulations, but it was only possible with a fine mesh. The doping distribution in the nanowire is deeply affected by thermal oxidation due to dopant segregation and self-interstitial injection. 3D simulation results show a decrease of boron doping in the nanowire of about one order of magnitude, with the decrease being more

pronounced for thinner nanowires. 3D device simulations compared with experimental data showed that the fabricated GAA-NW-FETs have a higher subthreshold swing with respect to simulated devices using *Advanced Calibration S-2021.06* Sentaurus TCAD parameters. The impact on the transfer characteristic of key technological parameters was analyzed, i.e. doping, silicon-oxide interface charges and work function of source and drain silicide. In particular, the lowering or increasing of the doping by a factor of 2 or less changes considerably the value of the threshold voltage and also affects the subthreshold slope. By choosing appropriate parameters, a fit to the experimental data was obtained. The doping distribution obtained during process simulation had to be modified to achieve the experimental subthreshold slope (multiplication by a factor of 1.5), meaning that the Sentaurus TCAD *Advanced-Calibration S-2021.06* parameters of boron segregation and diffusion during oxidation underestimate the doping distribution in the nanowire. In conclusion, these results show the importance of precise modeling of boron depletion during oxidation for a correct prediction of the electrical characteristic of junctionless GAA-NW-FET and call for further work to obtain a set of model parameters for a better estimation of doping in nanowires.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgment

The research leading to these results has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 871813 MUNDFAB. This work was partly supported by LAAS-CNRS micro and nanotechnologies platform, a member of the Renatech french national network.

References

[1] Takato T, et al. High performance CMOS surrounding gate transistor (SGT) for ultra high density LSIs. Technical Digest IEDM 1988;222.
[2] Lu W, et al. Nanowire transistor performance limits and applications. IEEE Trans Electr Dev 2008;55, 11:2859.
[3] Singh N, et al. High-performance fully depleted silicon nanowire (diameter $\leq$ 5 nm) gate-all-around CMOS devices. IEEE Electr Dev Lett 2006;27, 5:383.
[4] Yang B, Buddharaju KD, Teo SHG, Singh N, Lo GQ, Kwong DL. Vertical silicon-nanowire formation and gate-all-around MOSFET. IEEE Electr Dev Lett 2008;29(7):791–4.
[5] Ng R, et al. Vertically stacked silicon nanowire transistors fabricated by inductive plasma etching and stress-limited oxidation. IEEE Electr Dev Lett 2009;30, 5:520.
[6] Ritzenthaler R, et al. Vertically stacked gate-all-around Si nanowire CMOS transistors with reduced vertical nanowires separation, New Work function metal gate solutions, and DC/AC performance optimization. Technical Digest IEDM 2018;508.
[7] Veloso A, et al. Vertical nanowire FET integration and device aspects. ECS Trans 2016;72(4):31.
[8] Moers J. Turning the world vertical: MOSFETs with current flow perpendicular to the wafer surface. Appl Phys A 2007;87:531.
[9] Guerfi Y, Larrieu G. Vertical silicon nanowire field effect transistors with nanoscale gate-all-around. Nano Express 2016;11:210.
[10] David T, Liu K, Ronda A, Favre L, Abbarchi M, Gailhanou M, et al. Tailoring strain and morphology of core-shell SiGe nanowires by low-temperature Ge condensation. Nano Lett 2017;17(12):7299–305.
[11] Long E, et al. Nano-structuring in SiGe by oxidation induced anisotropic Ge self-organization. J Appl Phys 2013;113:104310.
[12] Fang WW, Singh N, Bera LK, Nguyen HS, Rustagi SC, Lo GQ, et al. Vertically stacked SiGe nanowire array channel CMOS transistors. IEEE Electr Dev Lett 2007;28(3):211–3.
[13] Müller J, et al. Engineering of Dense Arrays of Vertical Si1-xGex Nanostructures. Nanotechnology 2022. https://doi.org/10.1088/1361-6528/aca419. in press.
[14] Grove AS, et al. Redistribution of acceptor and donor impurities during thermal oxidation of silicon. J Appl Phys 1964;35:2695.
[15] Fukata N, Ishida S, Yokono S, Takiguchi R, Chen J, Sekiguchi T, et al. Segregation behaviors and radial distribution of dopant atoms in silicon nanowires. Nano Lett 2011;11(2):651–6.
[16] Han X-L, Larrieu G, Dubois E. Realization of vertical silicon nanowire networks with an ultra high density using a top-down approach. J Nanosci Nanotechnol 2010;10(11):7423–7.
[17] Guerfi Y, Carcenac F, Larrieu G. High resolution HSQ nanopillar arrays with low energy electron beam lithography. Microelectron Eng 2013;110:173–6.
[18] Guerfi Y, Doucet JB, Larrieu G. Thin-dielectric-layer engineering for 3D nanostructure integration using an innovative planarization approach. Nanotechnology 2015;26(42):425302.
[19] Larrieu G, Han X-L. Vertical nanowire array-based field effect transistors for ultimate scaling. Nanoscale 2013;5(6):2437.
[20] Larrieu G, Guerfi Y, Han XL, Clément N. N. Sub-15 nm gate-all- around field effect transistors on vertical silicon nanowires. Solid-State Electron 2017;130:9–14.
[21] Ye S, et al. Precise fabrication of uniform sub-10-nm-diameter cylindrical silicon nanopillars via oxidation control. Scr Mater 2021;198:113818.
[22] Fazzini P-F, et al. Modeling stress retarded self-limiting oxidation of suspended silicon nanowires for the development of silicon nanowire-based nanodevices. J Appl Phys 2011;110:033524.
[23] Uematsu M, et al. Two-dimensional simulation of pattern-dependent oxidation of silicon nanostructures on silicon-on-insulator substrates. Solid-State Electron 2004;48:1073.
[24] Han X-L, Larrieu G, Krzeminski C. Modelling and engineering of stress based controlled oxidation effects for silicon nanostructure patterning. Nanotechnology 2013;24(49):495301.
[25] Lau F, Mader L, Mazure C, Werner Ch, Orlowski M. A model for phosphorus segregation at the silicon-silicon dioxide interface. Appl Phys A 1989;49(6):671–5.
[26] Drummond TJ, "Work Functions of the transition Metals and Metal Silicides" Report Number SAND99-0391J (1999). https://www.osti.gov/servlets/purl/3597.