Solid-State Electronics 199 (2023) 108494

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

On the feasibility of DoS-engineering for achieving sub-60 mV subthreshold slope in MOSFETs☆

Jose Maria Gonzalez-Medina [a,*], Zlatan Stanojević [a], Zhaozhao Hou [b], Qiang Zhang [b], Wei Li [b], Jeffrei Xu [b], Markus Karner [a]

[a] Global TCAD Solutions GmbH, Landhausgasse 4/1a, 1010 Wien, Austria
[b] HiSilicon Technologies, Shenzhen, China

ARTICLE INFO

Keywords:
DoS-engineering
Subthreshold slope
Sub-60 mV
Tunnel
Rethermalization

ABSTRACT

We present the operating principle of an ideal Cold Source Field Effect Transistor and check the DoS source engineering impact on its subthreshold slope. The Subband Boltzmann Transport Equation is solved and the resulting transfer curves in the ballistic regime are presented, as well as those including the effects of scattering. The inclusion of scattering reveals its importance in the rethermalization of the cold carriers at the source extension and the degradation in the static leakage of the device. Finally, we show the impact in the SS when substituting the semiconducting source extension by the cold metal.

1. Introduction

In the scaling process of the field effect transistors (FET), several challenges are faced. One of them that still persists is achieving a sub-60 mV/decade subthreshold swing (SS) while preserving a high enough on–off current ratio. There are several designs, such as the Tunnel FET (TFET), that can achieve a good SS, but with an on–off current ratio penalty due to the band-to-band tunnelling process required to turn on the device. Other approach consists of engineering the density of states (DoS) by *filtering* the distribution function (DF) at the source contact. The idea relies on reducing the DoS at the source for high energies, in order to cut-off the Boltzmann tail of the DF. This can be achieved through several process, like (i) band to band tunnelling in Cold Source FET (CSFET) [1,2], (ii) mini-bands in a Superlattice (SLFET) [3], (iii) or a feature of the contact band structure, like the Dirac Source (DSFET) [4–6], among others. In this work, we study and simulate an ideal CSFET device, check the effectiveness of this DoS engineering and compare it to a Schottky Barrier CSFET (SBCSFET).

2. Methods

The device is simulated using the subband Boltzmann Transport Equation (SBTE) implemented in our Nano Device Simulator (NDS) [7]. The SBTE is solved in two or three phase-space dimensions. The SBTE can be transformed into a trajectory-based equation [8]. The Subband Boltzmann Transport equation reads

$$\left[\frac{\partial H_\nu(x,k_x)}{\partial k_x}\frac{\partial}{\partial x}-\frac{\partial H_\nu(x,k_x)}{\partial x}\frac{\partial}{\partial k_x}\right]f_\nu(x,k_x)=\mathbb{S}f, \tag{1}$$

where $f_\nu(x,k_x)$ is the subband distribution function (DF), the index ν denotes the subband index n in two-dimensional phase-space for 3D devices, and the combined subband and lateral $\mathbf{k}$-vector $\nu=(n,k_\perp)$ in three-dimensional phase-space (2D device). The SBTE can be directly discretized on a phase-space-grid, i.e. a tensor-product of the $\mathbf{r}$-space and $\mathbf{k}$-space grids. The Hamiltonian $H_\nu(x,k_x)$ is decoupled along the transport direction x, assuming the wave function to be confined perpendicularly to x and a plane wave along x,

$$\left[\mathbf{H}_{\text{kin}}(k_x)+V(x,y,z)\right]\psi(x,k_x)=E(x,k_x)\psi(x,k_x). \tag{2}$$

where $\mathbf{H}_{\text{kin}}(k_x)$ can be any Hamiltonian, such as effective-mass or $\mathbf{k}\cdot\mathbf{p}$. By solving the eigenproblem in Eq. (2) for each (x,k_x) we obtain the phase-space Hamiltonian $H_\nu(x,k_x)=E_\nu(x,k_x)$. The contour-method extracts trajectories from the Hamiltonian for each point of an energy-grid.

For each energy E and subband ν, we can have one or more trajectories, which are 1D curves in the phase-space: the transmitting trajectories are those that carriers follow when entering the device through the source and exiting at the drain, and vice-versa; other trajectories are reflecting and circular ones. We can denote each trajectory

☆ The review of this paper was arranged by Francisco Gamiz.

* Corresponding author.
E-mail addresses: jm.gonzalezmedina@globaltcad.com (J.M. Gonzalez-Medina), z.stanojevic@globaltcad.com (Z. Stanojević), houzhaozhao@hisilicon.com (Z. Hou), zhangqiang241@hisilicon.com (Q. Zhang), liwei110@huawei.com (W. Li), jeff.j.xu@huawei.com (J. Xu), m.karner@globaltcad.com (M. Karner).

https://doi.org/10.1016/j.sse.2022.108494

Available online 28 October 2022

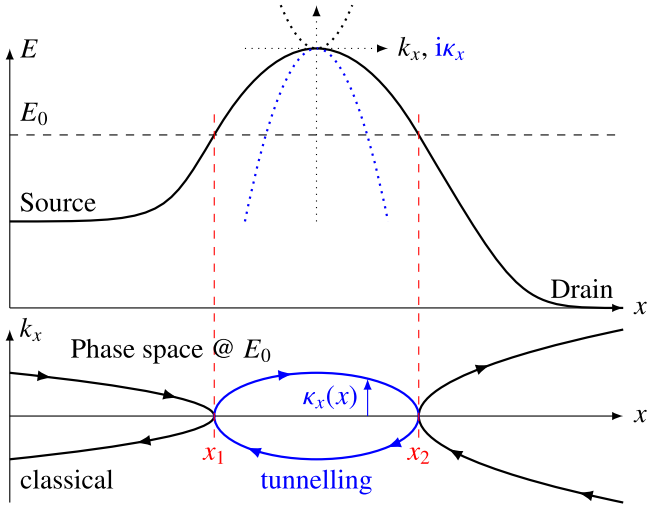

Fig. 1. Usual n-MOSFET potential in off-state along with the local real $E(x,k_x)$ and complex dispersion relation $E(x,\mathrm{i}\kappa_x)$; a cut through the $E(x,k_x)$ landscape at energy E_0 reveals the classical and tunnelling trajectories an electron can take; the classical turning points are marked as x_1 and x_2.

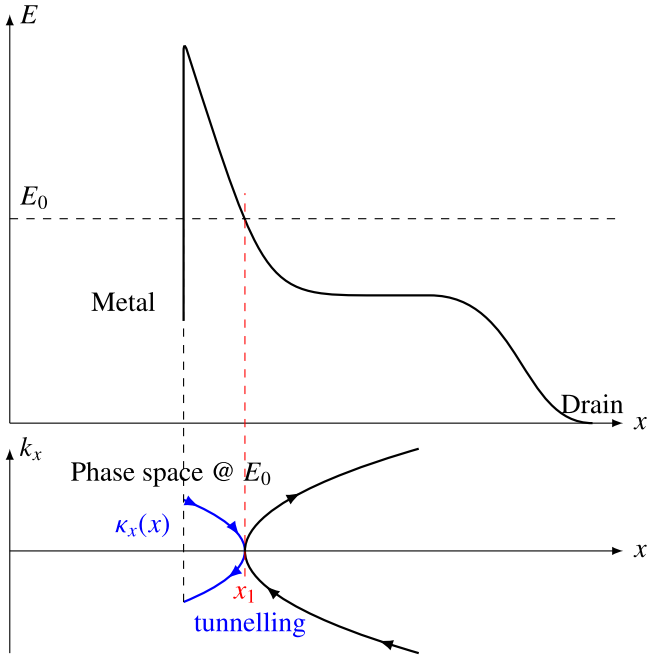

Fig. 2. Potential at a Schottky barrier MOSFET in on-state and phase space at E_0. There is only one tunnelling trajectory between the source contact and the classical turning point x_1.

at E in subband ν using a trajectory index η. The coordinate along each trajectory is the *time-of-flight* t. For every Hamiltonian H_ν, we can assign every point (x,k_x) in phase space to a point (E,η,t) in *trajectory-space*.

Getting back the scattering operator, the transformed SBTE based on trajectory-space reads,

$$\frac{\mathrm{d}f_{\nu,\eta}(E,t)}{\mathrm{d}t} = -\Gamma_{\nu,\eta}(E,t)f_{\nu,\eta}(E,t) + g_{\nu,\eta}(E,t), \tag{3}$$

where $\Gamma_{\nu,\eta}(E,t)$ is the out-scattering rate and $g_{\nu,\eta}(E,t)$ is the particle influx along the trajectory. There are several ways in which Γ and g can be solved. In this work, we ensure a scenario completely free of artificial carrier heating by transforming the elements in the scattering operator into trajectory-space $S_{\nu,\nu'}(\mathbf{k},\mathbf{k}';x) \mapsto S_{\nu,\nu'}(E,E';\eta,\eta';t,t')$. This is done for all scattering processes, elastic and inelastic. In the case of elastic scattering scenario, $E' = E$, the scattering operator is evaluated by integration over (E',η',t') to obtain $\Gamma_{\nu,\eta}(E,t)$ and $g_{\nu,\eta}(E,t)$ directly.

Finally, tunnelling along the transport directions (S/D-tunnelling, Schottky-barrier-tunnelling, band-to-band-tunnelling) can be directly included in the SBTE. In the case of source–drain tunnelling, Fig. 1, the BTE equations at points x_1 and x_2 are coupled, adding a generation term for the electrons at x_2 and a recombination term at x_1 as the charge is transferred from one point to the other. The Schottky-barrier-tunnelling scenario, Fig. 2, sets the metal side following a Fermi distribution, which is truncated for the cold source analysis of this work, and it adds a generation–recombination term only at the semiconductor, keeping the metal in equilibrium conditions.

For intra-band tunnelling, the transmission coefficients are calculated from the *complex subband structure* using the WKB-formula,

$$T(E_0) = \exp\left[-2\int_{x_1}^{x_2} \kappa_x(E_0,x)\mathrm{d}x\right], \tag{4}$$

where $\kappa_x(E_0,x)$ is the complex wavevector in the transport direction. The transmission coefficients are integrated into Eq. (3) as effective rates Γ_{tunn} and influxes into g_{tunn} [9].

3. CSFET results

The working process is shown in Fig. 3(a) and (b): the source has a null DF/DoS above $E_{\text{cut-off}}$; at on state, the barrier at the channel is low enough, so carriers below $E_{\text{cut-off}}$ can freely move. At off state, the barrier at the channel prevents the carrier flow, and this process is accelerated by the narrower window provided by the engineered DoS at the source. With a high enough barrier, ballistic current can be blocked, apart from Source–Drain tunnelling. A Cold Source FET can be ideally designed following this concept. At the source, we set a null DF/DoS above $E_{\text{cut-off}}$, which in this case is 0.1 eV above the source Fermi energy. In this example, below this $E_{\text{cut-off}}$ energy, the transmission probability is 1. The resulting device is presented in Fig. 4(a) and consists of an idealized Silicon nanowire CSFET transistor with ohmic contacts, without additional tunnelling processes or other contact resistances. The geometry details are shown in Table 1.

The ballistic current can have a steep SS in the off state compared to a regular MOSFET (down to 17 mV/decade in this ideal case). The transfer curves result is presented in Fig. 5 for 50 and 700 mV drain bias. The narrower DoS also reduces the on current with respect to the same device without DF filtering, both at low and high bias conditions. This simulation shows how, in an ideal ballistic situation, this concept can fit with the theoretical behaviour of a desirable sub-60 mV/decade. The blocking process can be seen in the distribution function at the energy-space grid depicted in Fig. 6(b), where it is clear that the DoS blocking bans the carriers from flowing above the barrier.

Next, the scattering process is included, thus carriers can heat up and have energies above $E_{\text{cut-off}}$, resulting in a flow of carriers above the channel barrier, as can be seen in Fig. 6(c), and in the current density plot in (a). This process takes less than 1 ps in Silicon [10]. The impact of this in the SS is shown in Fig. 5, where it remains clear that this DoS filtering can have a practically null impact in the device performance with respect to a regular MOSFET in steady state conditions.

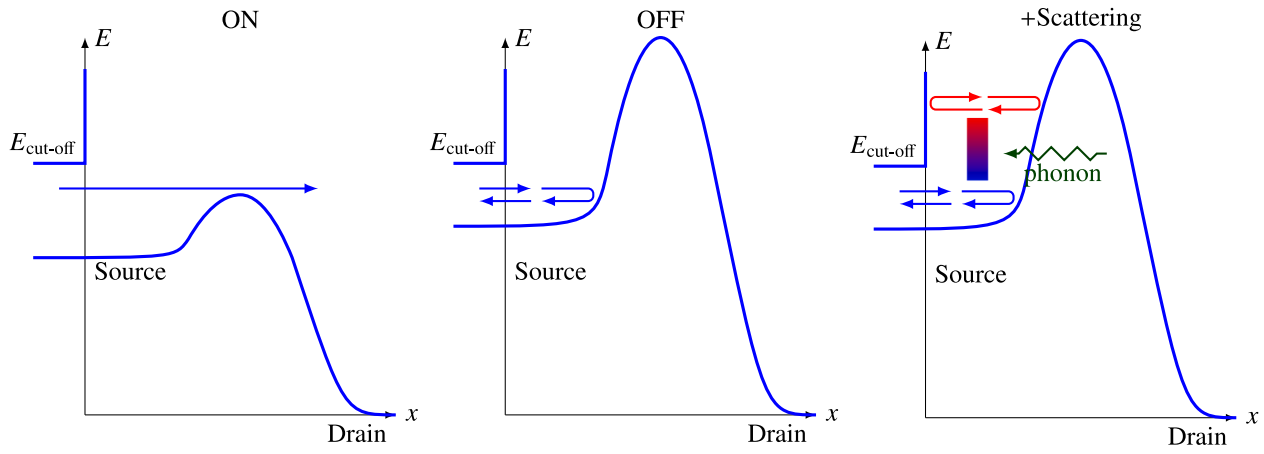

Fig. 3. Working principle of an ideal Cold Source FET device (a) ON state, (b) OFF state in ballistic situation. The inclusion of scattering effect (c) can potentially increase the energy of the carriers at the source.

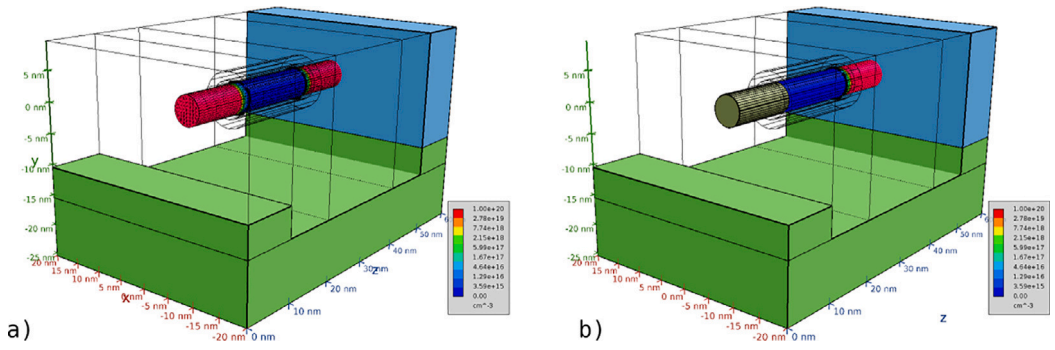

Fig. 4. (a) Simulated Silicon nanowire transistor device that acts as a CSFET. (b) CSFET with source extension substituted by the cold metal.

Table 1
Geometry information of the studied nanowire transistor.

Diameter	5 nm
Spacer length	10 nm
Channel length	20 nm
SiO_2 thickness	0.7 nm
HfO_2 thickness	1.5 nm
S/D doping	10^{20} cm^{-3}
Channel doping	10^{12} cm^{-3}

4. Schottky contact results

One way to avoid the rethermalization of the carriers at the source extension is substituting this semiconducting section by the cold metal (Fig. 4 (c)), resulting in a Schottky contact (see energy plots in Fig. 6(d) to (g)). The tunnelling process is evaluated using the WKB method explained in [7]. As now the current is mostly tunnel current, and as it mainly depends on the barrier thickness and very weakly on the temperature, the SS is mostly restored, as depicted in Fig. 5, blue curve. However, it now has the expected penalty in the on current due to the extra resistance added by the tunnelling (see Table 1).

5. Conclusions

An ideal CSFET implemented in a Silicon nanowire is studied. In presence of scattering, the sub-60 mV slope is only transient and would recover to over 60 mV in a few ps. Steep-slope devices are only useful if they can maintain a sub-60 mV slope over long periods of time, i.e. between switching events, in order to suppress static leakage. Steady-state steep slope only appears in ballistic simulation, but scattering inclusion severely changes the result. Approaches based on DF filtering or DoS engineering of the source in an otherwise regular MOSFET device (CSFET, SLFET, DSFET, etc.) cannot meet this requirement. Alternative SBCSFET restore the steep slope because it becomes temperature independent, but brings back the on current penalty present in tunnel devices.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

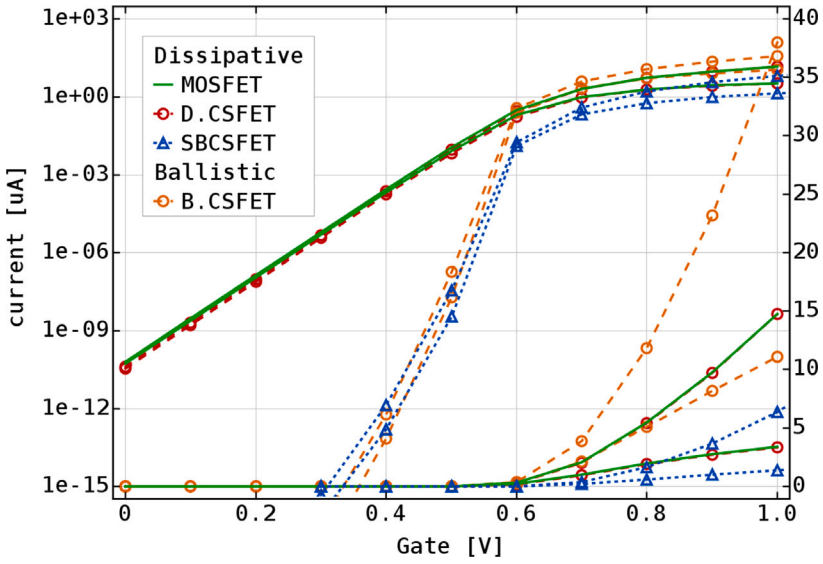

Fig. 5. Resulting transfer curves for $V_{DS} = 0.05$ and 0.7 V in (solid) a regular MOSFET, (dashed) an ideal CSFET in ballistic and dissipative regimes and (dotted) the Schottky contacted CSFET. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

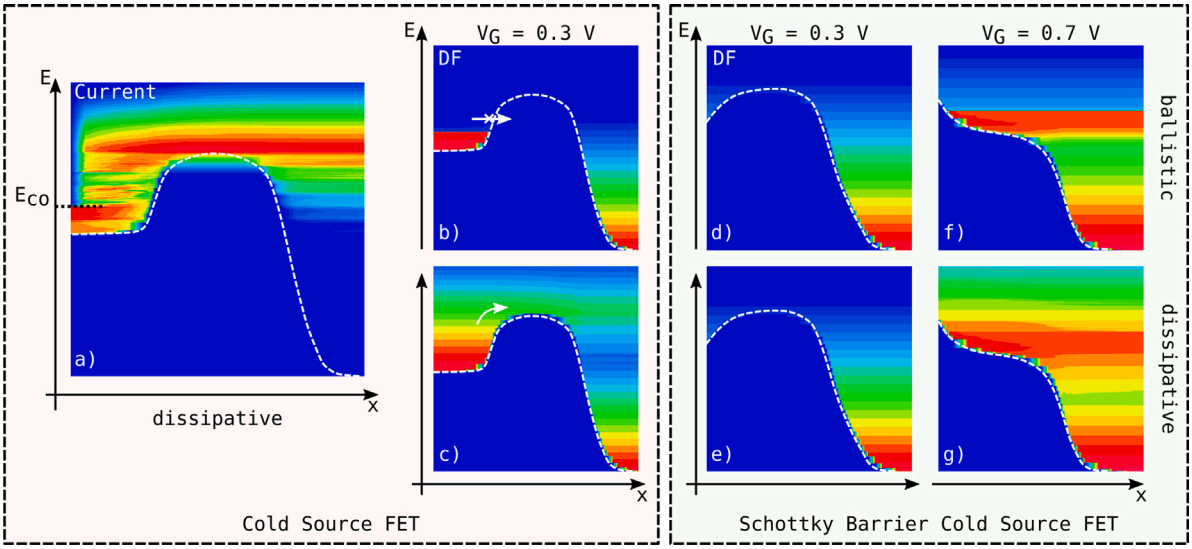

Fig. 6. (a) Current density of a CSFET in energy-space plot at $V_G = 0.3$ V. Distribution function in energy-space for $V_G = 0.3$ V in ballistic (b) and dissipative (c) regimes. The DoS cut-off prevents the carrier at higher energies to flow above the channel barrier only in ballistic regime. Scattering rapidly rises their energy, allowing them to flow. (d) to (g) Similar distribution function plots in a device with a source Schottky contact. The device turns to behave essentially as a Tunnel FET with an extra energy cut-off.

References

[1] Marin EG, Marian D, Perucchini M, Fiori G, Iannaccone G. Lateral heterostructure field-effect transistors based on two-dimensional material stacks with varying thickness and energy filtering source. ACS Nano 2020;14(2):1982–9. http://dx.doi.org/10.1021/acsnano.9b08489.

[2] Gan W, Prentki RJ, Liu F, Bu J, Luo K, Zhang Q, Zhu H, Wang W, Ye T, Yin H, Wu Z, Guo H. Design and simulation of steep-slope silicon cold source FETs with effective carrier distribution model. IEEE Trans Electron Devices 2020;67(6):2243–8. http://dx.doi.org/10.1109/ted.2020.2988855.

[3] Maiorano P, Gnani E, Gnudi A, Reggiani S, Baccarani G. Gate stack optimization to minimize power consumption in super-lattice fets. In: ESSDERC. IEEE; 2013, http://dx.doi.org/10.1109/essderc.2013.6818824.

[4] Qiu C, Liu F, Xu L, Deng B, Xiao M, Si J, Lin L, Zhang Z, Wang J, Guo H, Peng H, Peng L-M. Dirac-source field-effect transistors as energy-efficient, high-performance electronic switches. Science 2018;361(6400):387–92. http://dx.doi.org/10.1126/science.aap9195.

[5] Liu F, Qiu C, Zhang Z, Peng L-M, Wang J, Guo H. Dirac electrons at the source: Breaking the 60-mV/decade switching limit. IEEE Trans Electron Devices 2018;65(7):2736–43. http://dx.doi.org/10.1109/TED.2018.2836387.

[6] Tang Z, Liu C, Huang X, Zeng S, Liu L, Li J, Jiang Y-G, Zhang DW, Zhou P. A steep-slope MoS2/graphene dirac-source field-effect transistor with a large drive current. Nano Lett 2021;21(4):1758–64. http://dx.doi.org/10.1021/acs.nanolett.0c04657.

[7] Stanojevic Z, Tsai C-M, Strof G, Mitterbauer F, Baumgartner O, Kernstock C, Karner M. Nano device simulator—a practical subband-BTE solver for path-finding and DTCO. IEEE Trans Electron Devices 2021;68(11):5400–6. http://dx.doi.org/10.1109/TED.2021.3079884.

[8] Jin S, Fischetti MV, Tang T-W. Theoretical study of carrier transport in silicon nanowire transistors based on the multisubband Boltzmann transport equation. IEEE Trans Electron Devices 2008;55(11):2886–97. http://dx.doi.org/10.1109/TED.2008.2005172.

[9] Stanojevic Z, Strof G, Baumgartner O, Rzepa G, Karner M. Performance and leakage analysis of Si and Ge NWFETs using a combined subband BTE and WKB approach. In: SISPAD. 2020, p. 63–6. http://dx.doi.org/10.23919/SISPAD49475.2020.9241614.

[10] Lundstrom M. Fundamental of carrier transport. New York. USA: Cambridge University Press; 2009.