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Modeling of SiC transistor with counter-doped channel ☆

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ABSTRACT

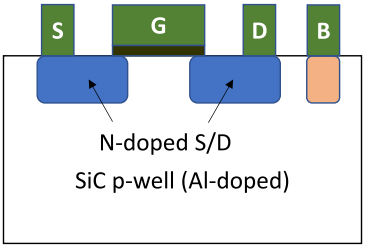
In this paper, we present a modeling framework to simulate the electrical characteristics of SiC MOSFET. Our model also describes the mobility improvement with counter doping in channel. Our analyses show improved drive current and degraded/lower threshold voltage with a counter-doped channel. To this end, we investigate the impact of varying the doping concentrations of the counter-doped region and the underlying p-well for optimum device performance.

1. Introduction

Field-effect transistors built on 4H Silicon Carbide (4H-SiC) are widely used for high-power applications owing to their high breakdown voltage, thermal conductivity, and ability to form native silicon dioxide [1]. However, performance of these devices is considerably affected by the presence of high density of interface traps (D_{it}) at the gate-oxide/SiC interface [2], which lowers the field-effect mobility and increases on-resistance. In this work, we present a TCAD-based methodology to simulate the electrical characteristics of n-channel SiC MOSFETs and investigate the impact of channel counter-doping [2–4] as a viable option to counteract the adverse impact of D_{it}. Our results show that the channel counter-doping improves the electron mobility and the device drive-strength, but at the cost of loss/lowering of the threshold voltage (V_T). Finally, we present a comparison of drive current gain and V_T loss for different concentrations of the counter-doped region to achieve the best possible scenario for practical applications.

2. Device description

The baseline SiC device-under-study (Fig. 1) has a channel length of 10 μm with an oxide thickness of 50 nm. The source/drain (S/D) regions are implanted with nitrogen (N) with a peak active doping concentration of 1e19 cm^{-3}, while the p-well has a peak aluminum (Al) concentration of 1e18 cm^{-3}. The process modeling is performed in close alignment with experimental setup to facilitate accurate model calibration. A box-shaped counter-doped region with 1e17 cm^{-3} N concentration is added to the channel to study its impact on the device performance.



Parameter	Dimension
Channel length	10 μm
Gate oxide	50 nm
Peak Channel Doping	1e18 cm^{-3}
Peak S/D Doping	1e19 cm^{-3}

Fig. 1. Schematic of baseline SiC nMOS (left) and important device dimensions (right).

3. Simulation

The electrical simulations are performed using drift–diffusion models for electron transport [5–7]. Due to the high D_{it} concentration at the gate oxide–SiC interface, remote Coulomb scattering with interface charges/trap has a significant impact on the mobility degradation of carriers and has been taken into account. Process flow for the model calibration has been detailed in Fig. 2. As shown in Fig. 3, a uniform D_{it}

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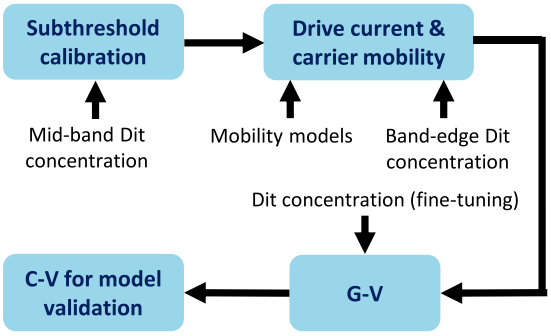


Fig. 2. Flow-chart of model calibration for SiC nMOS.

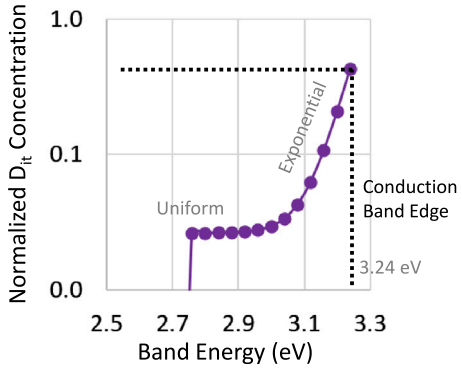


Fig. 3. D_{it} profile used to calibrate model to experimental data. Uniform D_{it} distribution near mid-band and exponential D_{it} distribution close to conduction band-edge used for subthreshold slope and drive current calibration, respectively.

distribution is considered in the mid-band region and the concentration is calibrated to match the measured sub-threshold slope (SS). Calibration for the above-threshold region is performed using a combination of the mobility model parameters and the D_{it} concentration near the conduction band edge, where an exponential D_{it} distribution is assumed following literature reports [2]. Finally, the D_{it} concentration is fine-tuned to match the conductance peak in the G–V characteristics and the C–V is used as final calibration check. Our analyses show that surface roughness scattering is a dominant mechanism, along with high D_{it} concentration at the channel interface, that degrades electron mobility in SiC channels.

We also present two methods to extract the mobility, as shown below, and compare the results:

$$g_m\text{-based: } \mu_{FE} = \frac{dI_D}{dV_G}\frac{L}{C_{ox}V_D W} \tag{1}$$

$$\text{Weighted average: } \mu_{avg} = \frac{\int_0^{s_{max}} \mu(s)n(s)\,ds}{\int_0^{s_{max}} n(s)\,ds} \tag{2}$$

where C_{ox}, L, W are the gate-oxide capacitance, channel length and width, respectively. $\mu(s)$ and $n(s)$ are the mobility and inversion-charge density distributions, respectively, at a depth s through the middle of the channel. Eq. (1) uses the device transfer characteristics to extract mobility, while Eq. (2) calculates a weighted average (weighted against the electron density) of the electron mobility distribution, obtained from TCAD simulations at each bias point, through middle of the channel.

4. Results and discussion

The baseline device transfer characteristics in Fig. 4(a) show close calibration between our SiC model and experimental data. The calibrated Dit profile and concentration (Fig. 3) aligns well with published data [2,8]. The band-edge Dit concentration in our model is also fine-tuned to match the conductance peak in the experimentally obtained G–V, as shown in Figs. 4(b). Finally, the C–V trend in Fig. 4(c) acts as a validation check for the final calibrated model. The mobility values obtained from our simulation, highlighted in Fig. 5, are in close alignment with the low channel-mobility values reported in literature for SiC transistors [4,9], validating the significance of our modeling framework. Our analysis shows that scattering with surface roughness, along with the high Dit density, at the oxide–SiC interface is the dominant factor causing mobility degradation in these SiC devices. Counter-doping the channel leads to drive current and mobility improvement. However, our results show that an important factor for consideration is the extent of depletion of the counter-doped region by the underlying p-well. Fig. 6 shows that the counter-doped channel can either be fully-depleted or partially depleted by the underlying p-well, which can lead to entirely different scenarios in terms of performance impact. A fully depleted counter-doped region, as a consequence of relatively high p-well doping (baseline device), leads to a 70% improvement in the drive current (Fig. 7). A combined increase in electron mobility (Fig. 8(a)) as well as a wider conduction path (Fig. 8(b)) accounts for the higher drive current. Counter-doping allows for lower electric field in the channel for the same inversion charge density, in turn,

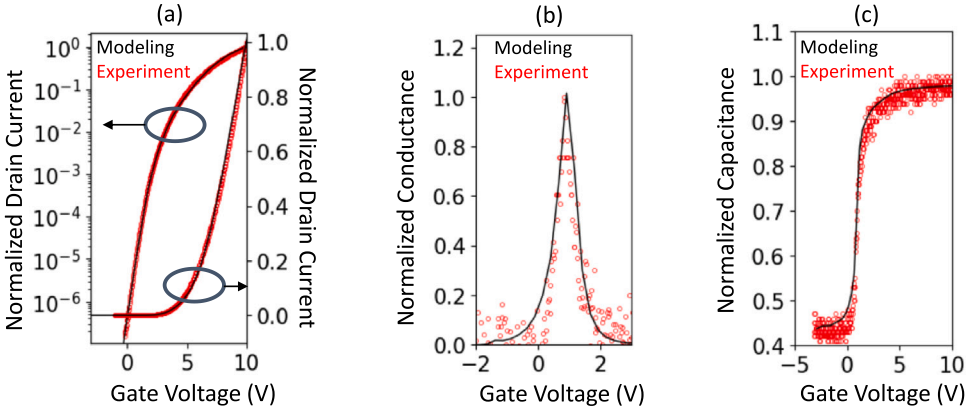


Fig. 4. Final Model calibration vs. experimental data for (a) transfer characteristics, (b) Conductance G vs. Vg, and (c) C–V. The transfer characteristics were used to calibrate mid-band and band-edge D_{it}. The G–V was used to fine-tune the final D_{it} concentration. Final model calibration check using C–V.

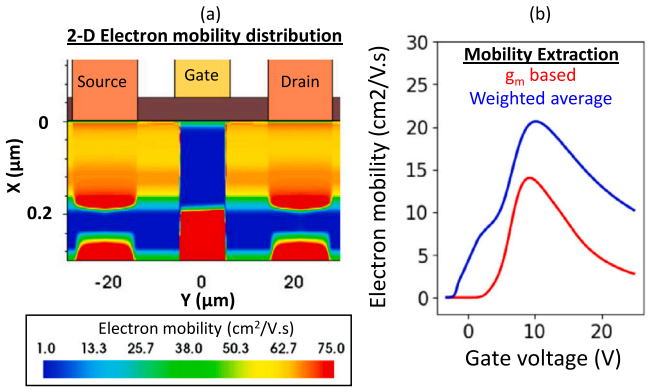


Fig. 5. (a) Electron mobility distribution, and (b) Mobility vs Vg trend in baseline device, along with comparison between gm-based and weighted-average mobility extraction methods.

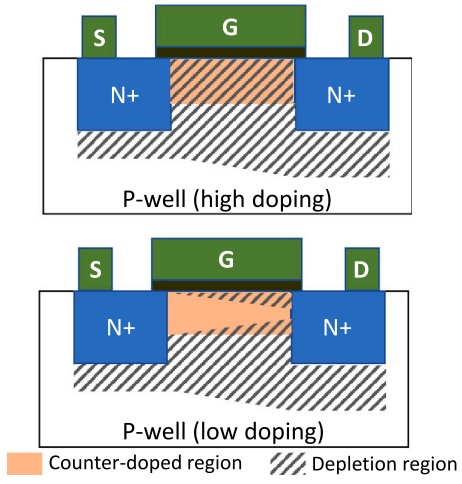
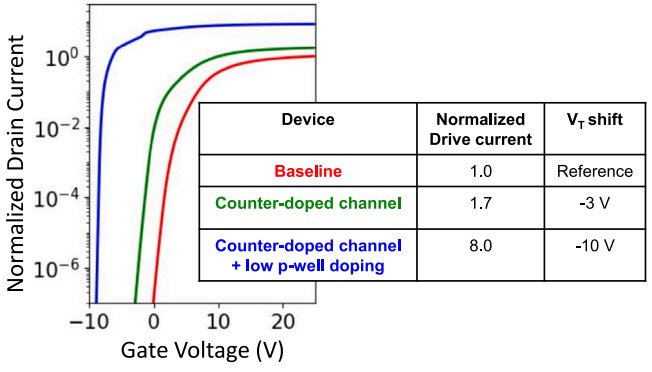


Fig. 6. Channel counter-doped with 1e17 cm^{-3} Nitrogen till a depth of 200 nm. Counter-doped channel is either fully depleted (top) or partially depleted (bottom) depending on the concentration (high or low, respectively) of the underlying p-well.



Device	Normalized Drive current	V_T shift
Baseline	1.0	Reference
Counter-doped channel	1.7	-3 V
Counter-doped channel + low p-well doping	8.0	-10 V

Fig. 7. I-V comparison between baseline device (no counter-doping), devices with partially depleted counter-doped region, and fully-depleted counter-doped regions. Counter-doped channel provides current gain but at the expense of V_T loss/lowering. Gate control loss with partially depleted counter-doped region due to very low VT in presence of buried channel.

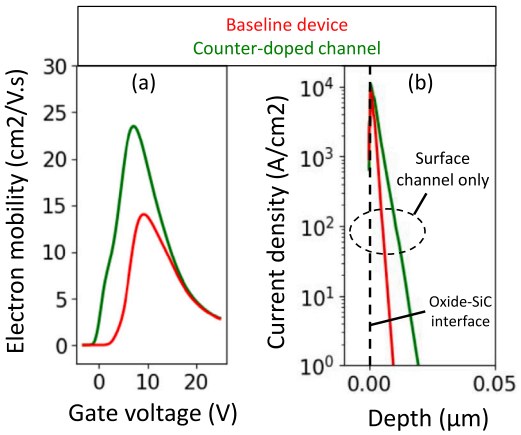


Fig. 8. (a) Impact of channel counter-doping on electron mobility for fully-depleted (high p-well doping) counter-doped region. Mobility improvement due to lower electric field in the channel for the same inversion charge density. (b) Width of conduction channel increases but no buried channel formation. Improvement in drive current with counter-doping due to the combined effect of electron-mobility improvement and a wider conduction path.

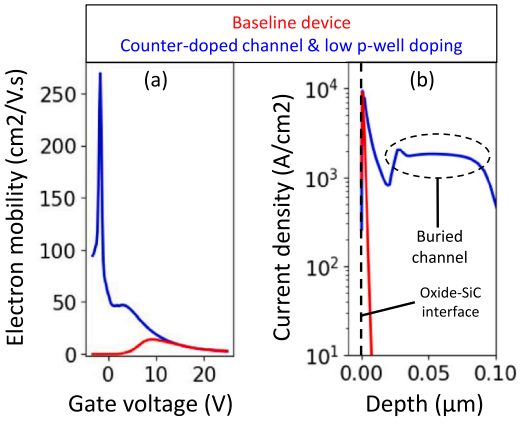


Fig. 9. Impact of channel counter-doping on (a) electron mobility for partially depleted (low p-well doping) counter-doped region. (b) Increase in channel width and formation of buried channel. High peaks in mobility only observed when buried channel is formed.

facilitating higher electron mobility. However, high peaks in mobility above 200 cm2/V.s, as reported in literature [2,4] for counter-doped channels, are achieved only if the counter-doped region is not fully depleted by the underlying p-well, leading to the formation of a buried channel. This is achieved in Fig. 9(a) by reducing the peak p-well doping by an order of magnitude and the formation of a buried channel is observed in Fig. 9(b). However, the resulting 8x increase in drive current is accompanied by a significant loss in the threshold voltage (V_T), as reported in Fig. 7, essentially creating an "Always On" device. On the other hand, the V_T loss associated with a fully depleted counter-doped channel can be recovered by tuning the doping profiles and transistor design. Fig. 10 show that by varying the concentration of the counter-doped region, we can achieve an optimized device design with good drive-strength combined with acceptable V_T loss. It can be seen from Fig. 10(a) that, for as low as 0.5 V V_T loss, a decent 10% improvement in drive current can be obtained by a lower 2e16 cm^{-3}

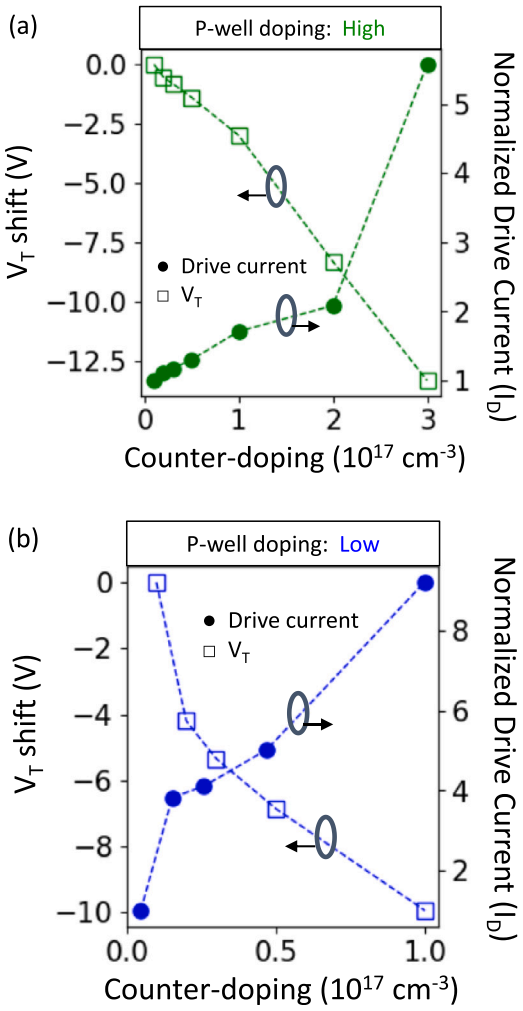


Fig. 10. Varying counter-doping concentration for achieving optimum conditions with (a) fully-depleted counter-doped region and (b) partially-depleted counter-doped region. Drive current improvement with minimal or acceptable V_T loss can be obtained with the fully-depleted channel. High V_T loss in the partially-depleted counter-doped channel case is irrecoverable even after lowering the counter-doping concentration, rendering the design unfavorable for practical application.

counter-doping concentration. Fig. 10(b) also shows that, even at low counter-doping concentrations, the device with low p-well doping and buried channel exhibits significant V_T loss, rendering it unfavorable for practical applications.

5. Conclusion

We present a TCAD model, validated with experimental data and published literature, to simulate the electrical behavior of the SiC planar MOSFET. Electron mobility values in these devices are very low, impacted significantly by the high D_{it} concentration and surface roughness at the gate oxide–SiC interface. Our results show that channel counter-doping indeed improves electron mobility by screening the negative impact of D_{it} and surface roughness, and provides a wider conduction path, leading to improved device drive-strength at the expense of V_T loss. The doping concentration of the counter-doped channel can be varied to achieve the most optimum scenario with good current gain for an acceptable V_T loss. We also highlight that the p-well doping level should be high enough so that the counter-doped region is almost fully depleted. Alternatively, a buried channel formation can lead to very high mobility and current gains but at an irrecoverable loss of gate control.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

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