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Hybrid 2D/3D mesh for efficient device simulation of locally deformed cylindrical semiconductor devices☆,☆☆

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ABSTRACT

In this work, we propose an efficient method to simulate cylindrical three-dimensional devices which have a locally deformed structure using a hybrid two-dimensional(2D)/three-dimensional(3D) mesh. The entire device is divided into several sub-devices. Each sub-device can have either a 2D mesh or a 3D one. The proposed method is applied to cases with and without structural deformation. It has been numerically demonstrated that the simulation becomes much more efficient with the hybrid 2D/3D mesh, while there is no loss of accuracy.

1. Introduction

Recently, as the demand for high-density NAND flash memories in various fields increases, major manufacturers increase the number of stacked layers in the vertical direction to achieve a higher bit density [1–4]. Channel holes are formed through a high aspect ratio etching process, and undesirable geometrical deformation — such as critical dimension variation of the top and bottom cells in the channel hole and distorted or polygonal shape of channel hole cross-section [5,6] – occurs in this process. Due to this geometrical deformation, unexpected electrical behavior during memory operation of a cell has been reported and various efforts have been made to resolve the problem [7,8].

Most manufacturers have adopted the multi-stack process in order to minimize the negative impact induced by the high aspect ratio etching process [9–12]. However, in the multi-stack process, a misalignment between two stacks may occur [13,14]. Due to such a misalignment, the electrical properties of cells near the stack interface can be different from those of normal cells. Therefore, it is expected that a locally tilted structure can affect the conduction current of the 3D NAND string.

When the device simulation is of concern, the performance of a 3D NAND flash memory string can be efficiently predicted by the quasi-2D simulation using the cylindrical coordinate system [7,15,16]. However, if the rotation axis offset occurs due to the misalignment mentioned above, the quasi-2D simulation is no longer available. In this case, it is appropriate to perform the full 3D simulation, but the full 3D simulation suffers heavily from a high computation burden.

In this work, we propose an efficient method to simulate partially deformed structures using a hybrid 2D/3D mesh. A 3D mesh is used for a part with the structural deformation from the rotationally symmetric structure. For all other parts away from the structural deformation, 2D meshes are adopted for efficiency. As an example, the proposed method is applied to a serially connected cylindrical nanowire transistor with and without a local tilt.

The organization of this manuscript is as follows. In Section 2, the proposed simulation methodology is briefly described. In Section 3, numerical results are shown. Finally, the conclusion is made in Section 4.

2. Device structure and simulation methodology

An in-house device simulator has been newly developed from scratch. In contrast to our existing in-house device simulator [17–19], which supports only either a 2D mesh or a 3D one, the newly developed device simulator supports a hybrid 2D/3D mesh. In order to show the feasibility of using a hybrid 2D/3D mesh, a cylindrical 3D device with two control gates and source/drain contacts is tested.

Fig. 1 shows the device structure used in the simulation. The gate length and the spacing between two gates are 45 nm. In addition, the silicon channel radius and insulator thickness are assumed to be 10 nm and 2 nm, respectively. The source/drain doping is about 10^{20} cm^{-3} and an intrinsic channel is assumed.

The entire device is divided into three sub-devices in order to apply our proposed method. Each sub-device can have a 2D mesh or a 3D one. The Poisson equation and the electron/hole continuity equations

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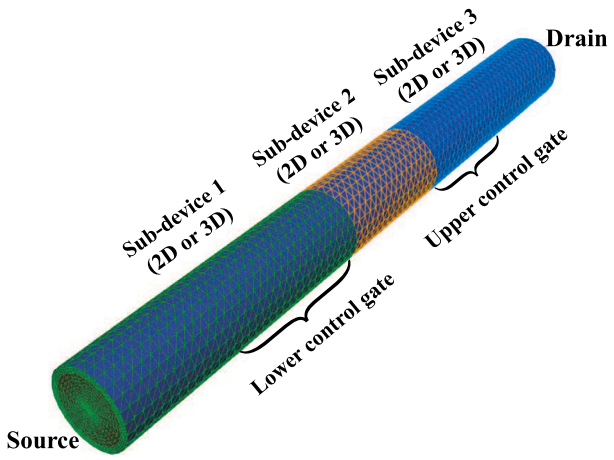

Fig. 1. Simulated device structure. It has two control gates and source/drain contacts. The entire structure is divided into three sub-devices.

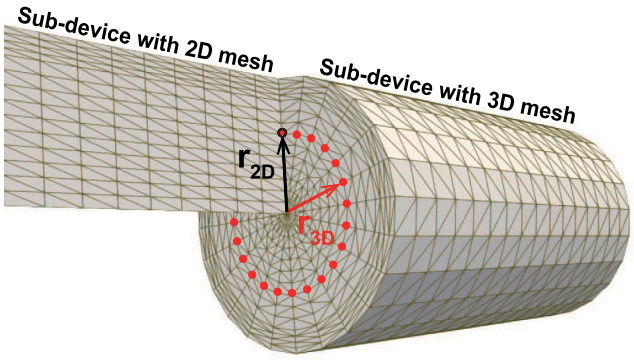

Fig. 2. An interface of two adjacent sub-devices of different dimensions. In this case, there exist a 2D node and several 3D nodes indicated by black and red dots, respectively. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

are solved for these sub-devices, and as a result, the solution variables and the I–V characteristics can be obtained.

One of the most important things in this work is to connect adjacent sub-devices, and the detailed method is as follows. First of all, we need to compute the interface points between adjacent sub-devices. In the case of a 2D/2D interface or a 3D/3D one, interface points can be found in a relatively simple way using vertex positions. In the case of a 2D/3D interface, a point in the 3D mesh (●) is connected to a point in the 2D mesh (●) by finding the radius from the position information as illustrated in Fig. 2. After that, for each sub-device, the Poisson and two continuity equations are implemented using its own mesh. Finally, the equations implemented in adjacent sub-devices are merged using the interface information calculated in advance. Again, in the case of a 2D/2D interface or a 3D/3D one, two interface nodes have the same dimensionality and they can be easily merged. In the case of a 2D/3D interface, there exist a 2D node and several 3D nodes. Equations evaluated at several 3D nodes are merged in an equation at the 2D node. Physical quantities at several 3D nodes follow those at the 2D node. Following this way, the rotational symmetry is enforced even to the 3D interface nodes.

3. Result and discussion

When the entire device in Fig. 1, which is cylindrical symmetric without structural deformation, is divided into three sub-devices, 8 different cases occur in total. Among them, the electrostatic potential profiles for three representative cases are shown in Fig. 3. The quasi-2D/3D/quasi-2D case in Fig. 3(b) clearly reveals the capability of our proposed method.

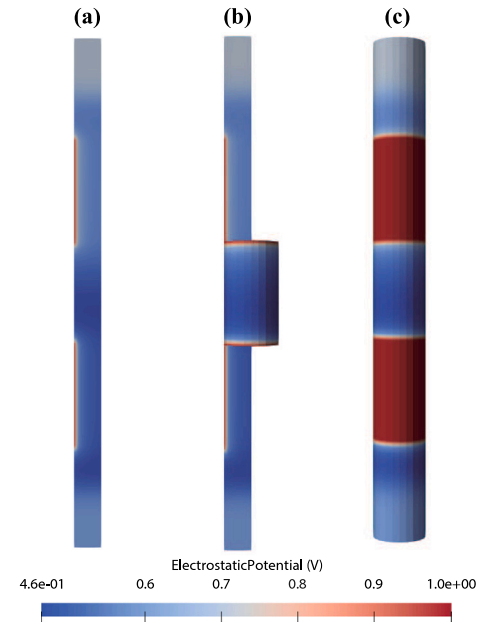

Fig. 3. Electrostatic potential profiles of three representative cases. (a) Quasi-2D/quasi-2D/quasi-2D, (b) quasi-2D/3D/quasi-2D, and (c) 3D/3D/3D.

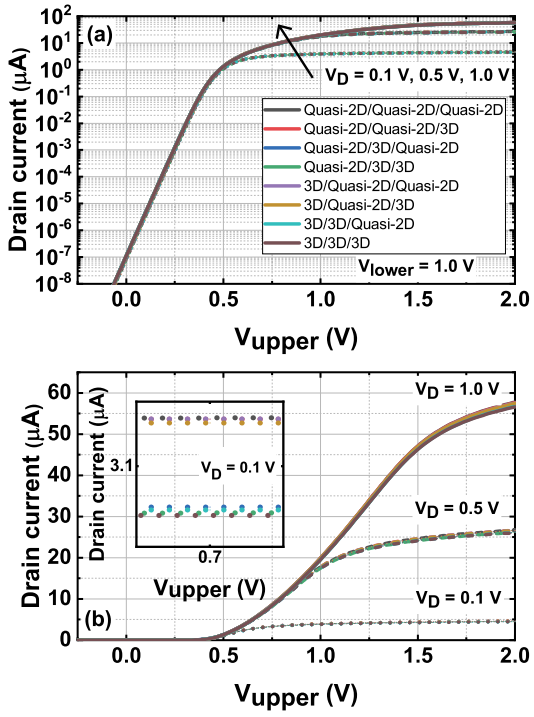

Fig. 4. Calculated I–V characteristics of the eight cases ((a) logarithmic and (b) linear scale). The applied lower control gate voltage is 1.0 V.

Fig. 4 shows the I–V characteristics calculated for 8 cases made with 3 sub-devices. The drain voltages are 0.1 V , 0.5 V and 1.0 V, and the lower control gate voltage is fixed as 1.0 V. Then, the drain current is calculated as a function of the upper control gate voltage (V_{upper}). For this rotationally symmetric structure, the quasi-2D/quasi-2D/quasi-2D

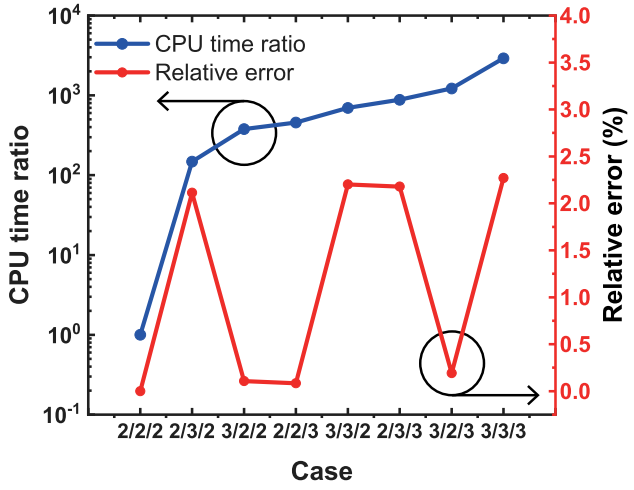

Fig. 5. CPU time normalized to the quasi-2D/quasi-2D/quasi-2D case. 2 and 3 in x-axis represent the quasi-2D and the 3D, respectively. Relative error of the drain current at V_{upper} = 1.0 V is also shown.

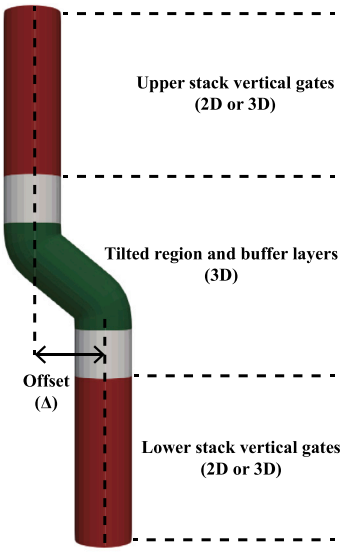

Fig. 6. Simulated 3D device structure which have vertically stacked control gates with rotation axis misalignment (Δ). Additional buffer layers (Gray) are included in these locally deformed cases.

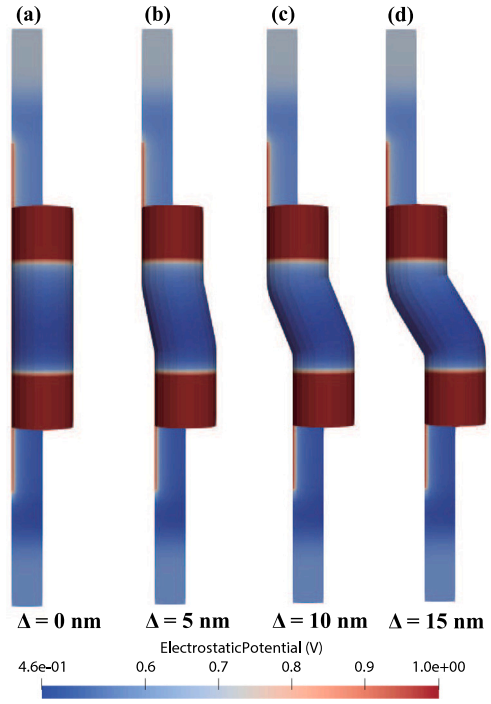

Fig. 7. Calculated electrostatic potential using quasi-2D/3D/quasi-2D sub-devices with the offset (Δ) (a) 0 nm, (b) 5 nm, (c) 10 nm, and (d) 15 nm. The voltage of the drain and two control gates is 0.1 V and 1.0 V, respectively.

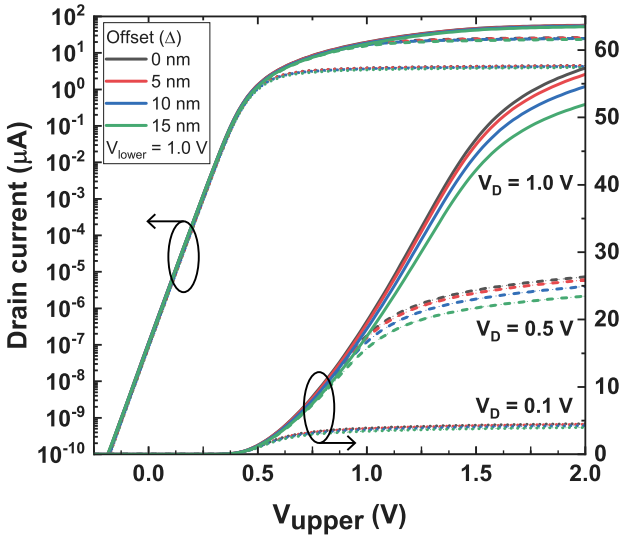

Fig. 8. I–V characteristics for several rotation axis offsets. The drain voltages are 0.1 V, 0.5 V, and 1.0 V and lower control gate voltage is 1.0 V.

case, which is calculated in the cylindrical coordinate system, yields the most accurate result. The 3D/3D/3D result is the most inaccurate result among all 8 cases, and the error is originated from a finite number of points along the angular direction. The inset of Fig. 4(b) shows the drain current when the upper control gate voltage is about 0.7 V. Two groups are clearly identified.

We have investigated the central processing unit (CPU) time to solve the coupled set of equations and the drain current error in all cases as shown in Fig. 5. The CPU time for each case is normalized to that of the quasi-2D/quasi-2D/quasi-2D case. The drain current is measured when the upper control gate voltage is 1.0 V and its error is also referred to the full quasi-2D one. It is confirmed that the CPU time required to solve the coupled set of equations increases rapidly as more 3D meshes are introduced. Compared with the full 3D case (3/3/3), the quasi-2D/3D/quasi-2D (2/3/2) is more than ten times faster. Of course, the difference between them becomes even larger when the sub-devices 1 and 3 contain more nodes. In addition, when the central sub-device (sub-device 2) has a 3D mesh, the drain current error increases sharply. It can be also shown in the inset of Fig. 4(b).

Our method can be applied even when an offset of the rotation axis occurs. Fig. 6 shows a serially connected nanowire transistor with a local tilt, originated from the misalignment between stacks. The rotation axis offset is Δ. Geometrical parameters are equivalent to a symmetrical device. Although the 3D simulation should be performed for the tilted part, the quasi-2D simulation is possible for the parts away from the structural deformation. Unlike the rotationally symmetric device, the electrostatic potential and the carrier densities may be rotationally asymmetric in the space near the local tilt. As discussed in Section 2, the rotational symmetry is enforced at a 2D/3D interface.

To alleviate such an asymmetric distribution of electrical variables, the central sub-device should include some buffer layers (Gray regions in the figure).

Fig. 7 shows the calculated electrostatic potential of a locally tilted device when the offset is 0 nm, 5 nm, 10 nm, or 15 nm. As shown in Fig. 7, the quasi-2D/3D/quasi-2D sub-devices are used for this simulation. Fig. 8 shows I–V characteristics for several rotation axis offsets. The drain current decreases as the offset increases.

In the case of the device structure used in Fig. 7 which has only one control gate in each of the upper and lower stacks, the central 3D part has a significant contribution to the total device volume. For this reason, the CPU time with our proposed method is not much shorter than that of the full 3D simulation. However, for a device which has numerous control gates in each of stacks, for example, state-of-the-art vertical NAND flash memories, a dramatic reduction in overall simulation time can be expected.

4. Conclusion

In conclusion, we have proposed the hybrid 2D/3D mesh for an efficient device simulation. By applying it to a cylindrical device, it has been confirmed that the proposed method significantly reduces the CPU time to solve coupled set of equations without loss of accuracy. The hybrid 2D/3D mesh is expected to be more useful for realistic 3D NAND flash memories.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be available on reasonable request.

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