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Ferroelectric FDSOI FET modeling for memory and logic applications☆,☆☆

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ABSTRACT

In this paper, we present a Verilog-A based compact model for simulating Ferroelectric Fully Depleted Silicon-on-Insulator (Fe-FDSOI) FET. The model can capture the rich physics of ferroelectric (FE) materials and reproduce the important electrical characteristics, such as history effect, the impact of threshold voltage on pulse width and amplitude as well as potentiation–depression characteristics. The FE switching is modeled using Preisach model to capture the Polarization (P)–Voltage (V) characteristics. In addition, we capture the history-dependent minor loop characteristics to obtain multiple states of polarization. This allows the modeling of multiple conductance states, which forms the fundamental prerequisite for neuromorphic applications as well as multi-level non-volatile memories. The underlying baseline FDSOI FET is modeled using the industry-standard BSIM-IMG compact model. The model is then augmented with the physics-based model of FE capacitor to realize Fe-FDSOI FET. Our model is computationally efficient and carefully calibrated to reproduce experimental measurement data.

1. Introduction

FeFET shows great potential for non-volatile memory and neuromorphic applications [1,2]. To fully exploit the functionality of FeFETs, we need efficient compact models to explore the large available design space. However, existing models based on nucleation-limited switching [3] or accurate physics-based solutions of the Poisson's equation [4] require numerical solutions, which is computationally inefficient for large circuit simulations. Single domain L-K equation-based models are fast and easy to simulate but cannot capture the history effect of FeFETs [5]. Thus, compact models based on Preisach equations are best suited to successfully reproduce the trends of memory window, conductance, and history effects from experimentally measured data [6,7]. However, existing Preisach-based implementations require storing a large number of previous turning points to reproduce the history effect which makes it time-consuming and memory-intensive.

In this paper, we present an efficient compact model that stores a smaller number of turning points and can still reproduce all the experimentally observed characteristics. The primary advantage of our model comes from using an R-C element to evaluate the turning points and at the same time store a lesser number of turning points [8] through meticulous assumptions. We particularly simulate Fe-FDSOI devices for their ability to use the back gate for tuning the threshold voltage (V_{TH}). Also, the recently proposed concept of dual-gate FeFETs is particularly promising for its ability to amplify the memory window even at the reduced thickness and write voltage by reading from the back gate [9]. To validate the working of our model, we first calibrate the underlying FDSOI device with experimental data [10] using the industry-standard compact model for the FDSOI technology (BSIM-IMG) [11,12]. Then, we calibrate the FE capacitor using the developed Fe-Cap model to get the required parameters for the realization and simulation of Fe-FDSOI. To explore the design space for memory and logic applications, we simulate the transfer characteristics of the device and the effect of back bias. Further, we demonstrate the pulse-width and pulse-magnitude-dependent switching characteristics of the device. Finally,

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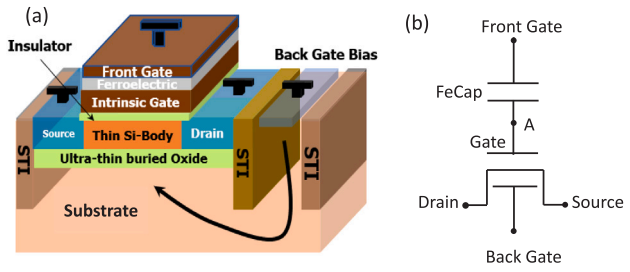

Fig. 1. (a) The structure of the Fe-FDSOI in MFMIS configuration and (b) the equivalent circuit representation.

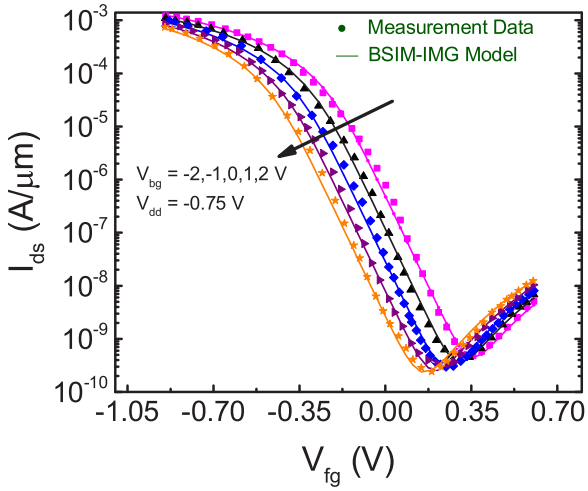

Fig. 2. Calibration of the underlying FDSOI transistor against experimental data from [10].

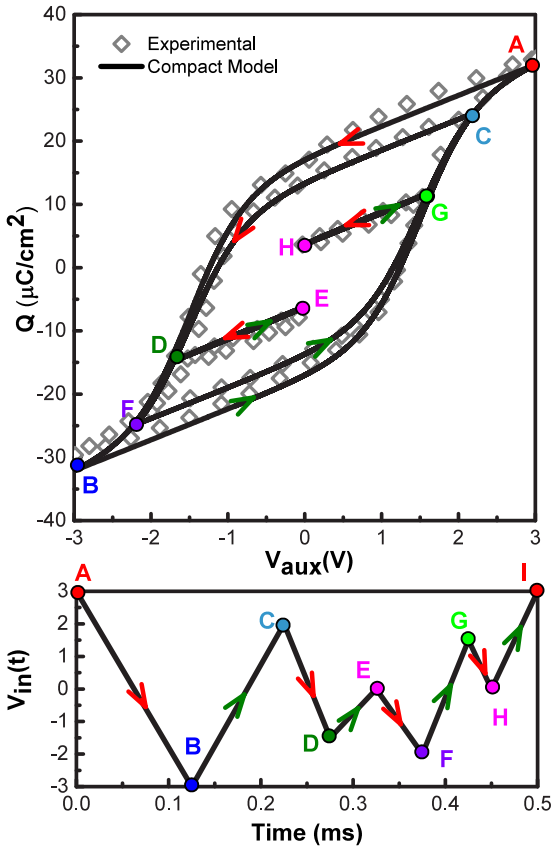

Fig. 3. The validation of the Fe-Cap model against experimental data from [6]. This clearly shows the history effect of the model.

we show the potentiation and depression characteristics exhibited by the Fe-FDSOI which is lucrative for neuromorphic and other emerging applications [13,14].

2. Model description

The structure of the Fe-FDSOI device is shown in Fig. 1. It is an MFMIS (Metal–Ferroelectric–Metal–Insulator–Semiconductor) structure. A growing interest is shown in back-end-of-line (BEOL) compatible FeFET devices which have a lot of potential benefits like high write endurance, reduced interface charge traps, and increased memory window. This, in principle, is very similar to the MFMIS structure where the ferroelectric capacitor (Fe-cap) and the transistor can be treated as separate entities. Because of the equipotential metal layer in between, the Fe-Cap is connected in series with the gate of the transistor. In this work we have considered only MFMIS structure as modeling it is computationally more efficient. We can separately model the Fe-cap and underlying FDSOI FET. We first discuss the model of Fe-cap followed by the overall Fe-FDSOI.

2.1. Fe-Cap modeling

The Fe-FDSOI FET is modeled by separately modeling the Fe-Cap and the FDSOI transistor. Fe-Cap is modeled using the Preisach model which is a macro-level model to capture the polarization (P)–Voltage (V) characteristics [7]. To capture the switching characteristics, an auxiliary voltage (V_{aux}) is calculated. V_{aux} represents the actual voltage to which the ferroelectric dipoles respond after the relaxation. This is given using the equation Eq. (1), which can be emulated using a simple R-C delay network

$$V_{aux} = V_{in} - \tau_v \frac{d}{dt} V_{aux} \tag{1}$$

where τ_v represents the relaxation time for V_{aux} and V_{in} is the applied input voltage at the gate of the Fe-Cap. Then, the polarization corresponding to V_{aux} (P_{aux}) is calculated using :

$$P_{aux} = m \cdot P_s \cdot \tanh(w(V_{aux} \pm V_c)) + P_{off} \tag{2}$$

$$w = \frac{t_{fe}}{2V_c} \cdot \ln\left(\frac{P_s + P_r}{P_s - P_r}\right) \tag{3}$$

where V_c is the coercive voltage of the Fe material, P_s is the saturation polarization, P_r is the remnant polarization, m is the slope of the curve and P_{off} is the offset polarization. The material considered for the simulation is Zr-doped HfO2, and the parameter values are given in Table 1. The upwards (−) and downwards (+) polarization determine the sign of tanh function and the values of m and P_{off} is calculated using polarization history which determines the P–V characteristics of the minor loops. For the main loop, $m = 1$ and $P_{off} = 0$.

The polarization history is determined by tracing the turning points of the V_{in}. The turning points are calculated based on a delayed voltage

Table 1
Values of material parameters.

Parameters	Value
P_r	18.5 μC/cm²
P_s	19 μC/cm²
V_c	1.2 V
t_{fe}	10 nm
ϵ_{fe}	40
τ_v	1.5 μs

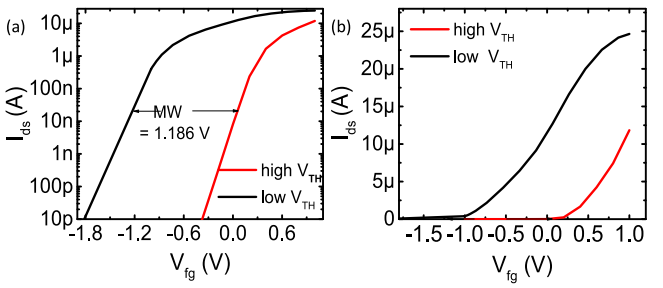

Fig. 4. The simulated transfer characteristics of the Fe-FDSOI device having a width of 100 nm in (a) Log scale, and (b) Linear scale showing a memory window (MW) of 1.186 V.

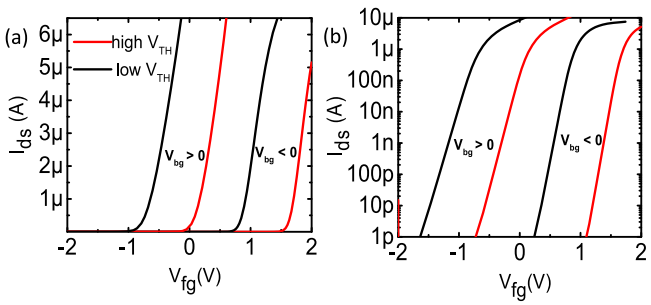

Fig. 5. Effect of back bias on the transfer characteristics of the Fe-FDSOI structure shown in (a) Log scale (b) Linear scale. A positive back bias shifts the graph to the left thus reduces V_{TH} and vice-versa for negative back bias.

(V_{del}) using another R-C delay network. Instead of computing maxima and minima by calculating derivatives of the input voltage, this method helps us to speed up the simulation. The time constant of the R-C delay is chosen very low to not have a significant effect on V_{aux} and is much less than τ_v. If V_{del} is greater than or less than V_{aux}, we correspondingly store the V_{aux} and P_{aux} as the turning up (u) or down (l) points. Thus, m and P_{off} is given by:

$$m_{\uparrow,\downarrow} = \frac{P_{aux,u} - P_{aux,l}}{P_s \cdot (\tanh(w(V_{aux,u} \pm V_c)) - \tanh(w(V_{aux,l} \pm V_c)))} \quad (4)$$

$$P_{off\uparrow,\downarrow} = P_{aux,u/l} - m_{\uparrow,\downarrow} \cdot P_s \cdot \tanh(w(V_{aux,u/l} \pm V_c)) \quad (5)$$

The arrows correspond to the direction of polarization and correspondingly the sign of tanh function. When V_{aux} is less than $V_{aux,l}$ during the downward sweep, or V_{aux} is greater than $V_{aux,u}$ during the upward sweep we assume the second turning point to be the maximum positive and negative voltages. Existing models based on Preisach equations required storing all the previous points. Assuming the minor loop follows a trajectory similar to the major loop (with the terminating voltages being maximum applied positive and negative bias) helps us to get rid of all the previous points and yet successfully approximate the P_{aux}-V_{aux} characteristics. For a more detailed description of the model, please refer to [8].

2.2. Fe-FDSOI modeling

As stated earlier, the underlying FDSOI transistor is modeled using BSIM-IMG and calibrated with experimental data as shown in Fig. 2. The overall Fe-FDSOI is then modeled by solving the charge balance ($Q_{mos} = P_{FE}$*W*L) and voltage balance ($V_{total} = V_{fe} + V_{mos}$) at node A (Fig. 1). The effect of back-bias and other transistor properties is captured automatically in BSIM-IMG [12].

3. Model validation

The model is validated against experimental data from [6]. Firstly, the value of P_r, P_s, and V_c are extracted. Next, an aperiodic, and asymmetric input signal is applied as shown in Fig. 3 to the Ferro-cap. The resulting P_{aux} vs. V_{aux} demonstrates the major loop and minor loops. The model performs well to reproduce experimentally observed characteristics. This demonstrates clearly the historical effect of the ferroelectric material.

Next, we demonstrate the I–V characteristics of the FeFET in Fig. 4 having a memory window of about 1.2 V. The effect of back bias on the transfer characteristics is shown Fig. 5. A negative back bias shifts the threshold voltage of both states to the right, whereas a positive back bias shifts it toward the left. This is especially useful for some memory applications such as ternary content addressable memory to shift the V_{TH} states greater than zero and allow disturb-free hold and read operation [14]. Also recently proposed double-gate FeFET can be simulated using our model which enables a large memory window by reading from the back gate. This is possible because of the thick buried oxide layer in the FDSOI transistor [9].

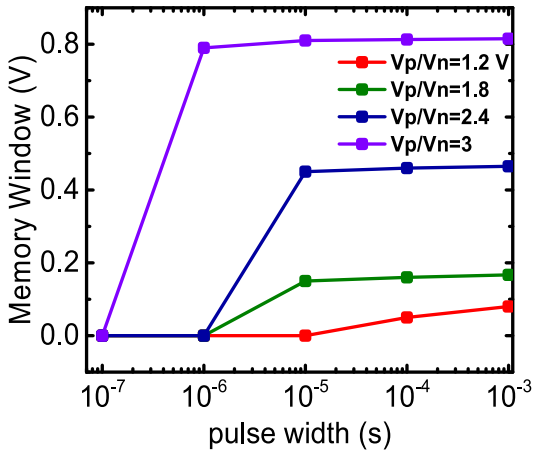

Fig. 6. Variation of memory window with applied pulse width for different pulse amplitude. After the device switches, the variation is very less.

The dependency of pulse amplitude and width on the switching of the FeFET using our model is shown in Fig. 6. A larger amplitude with a smaller width corresponds to a higher memory window and faster switching [6]. Next, we explore the application space of Fe-FDSOI.

4. Model applications

The most interesting property of FeFET is the continuous variation of the V_{TH} states. This forms the basis for most of the applications in FeFET ranging from multi-level-cell storage to neuromorphic computing. Pulse amplitude modulation is stated to be the best method for changing V_{TH} owing to linear and equally spaced states [2]. This effect is also captured using our model and is demonstrated in Fig. 7. Variation in the magnitude of the positive pulse (Vp) or variation in the magnitude of the negative pulse (Vn) sets it into different V_{TH} levels.

FeFET has been demonstrated as a possible solution for neuromorphic and logic-in-memory applications. One key step in neuromorphic computing is the update of weights using systematic potentiation and depression pulses. This is enabled due to the history effect of FeFET where the polarization is stored according to the applied pulse. Our model can predict the almost linear increase and decrease of the channel conductance with the application of these pulses. We calculate the conductance at Vds = 0.1 V after every pulse, as shown in Fig. 8. It shows relatively linear and symmetric characteristics, which is highly desirable.

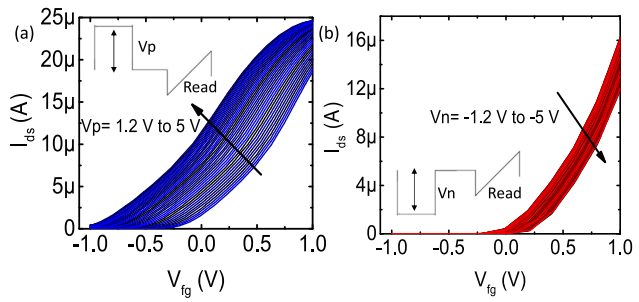

Fig. 7. Varying positive amplitude Vp and negative amplitude Vn to set in different V_{TH} for (a) programming and (b) erase states. The values of Vp and Vn set the device into different threshold voltage levels thus enabling MLC as well as other applications.

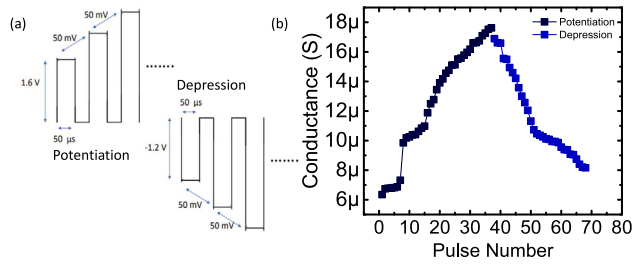

Fig. 8. (a) Applied waveforms for the channel conductivity increase (potentiation) and decrease (depression). (b) potentiation and depression characteristics. The conductance can be mapped directly to neural weights and can be used for neuromorphic applications.

5. Conclusion

We presented a robust and efficient compact model for Ferroelectric FDSOI. Compared to existing compact models our model requires much less memory as it requires storing much lesser turning points. Also, our unique way of calculating turning points without derivatives and using delay at an internal node makes way for speed benefits. We have also demonstrated a glimpse of the range of applications that Ferroelectric FDSOI holds for the future. This paves the way for further development of large-scale circuits, including non-volatile memory, logic, and in-memory applications.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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