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Enabling medium thick gate oxide devices in 22FDX® technology for switch and high-performance amplifier application

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ABSTRACT

In this paper two processes with different source and drain out diffusion into the channel of medium thick gate oxide devices in 22FDX® are compared in terms of HCI reliability (electrical field) and DC/RF performance. The margin to pass HCI reliability of the under-drive device allows a steeper source/drain doping profile which enables further gate length reduction. The steeper doping profile reduces R_{on} significantly while improving the electrostatic behavior due to the longer effective channel. Gate length scaling allows a better trade-off between electrostatic behavior, DC/RF performance, breakdown voltage and reliability. For switch applications the C_{off}*$R_{on,AC}$/V_{max} figure of merit can be reduced while ft and fmax is increased for power amplifier applications.

1. Introduction

22FDX® platform constitutes an excellent choice for RF and mmWave application combined with superior low power logic performance and non-volatile memory [1]. Extension of the platform offering entails trade-offs between device performance and application-specific reliability criteria. In this work, we focus on optimizing the device performance of the medium thick gate oxide device, targeting high-performance amplifier and switch applications. The combination of gate length reduction and modified source/drain doping profile improves on-state resistance while remaining the devices the HCI reliability [2,3].

2. TCAD setup and calibration

Following the calibration strategy of the thin gate oxide devices in [4], medium thick devices have been calibrated based on DC, AC and RF data in SProcess and SDevice including all relevant process steps. Fig. 1 shows the architecture and doping profile of the NFET device featuring an undoped channel and nwell below the BOX. Fig. 2 shows the TCAD to HW correlation for under-, regular- and over-drive device (different V_{DD} and gate length – L_G) and well type below the BOX (SLVT-nwell / LVT-pwell) for typical DC parameters on a single finger structure. P-type back gate embedded into a triple well allows best decoupling from the substrate which is key for stacking in switch devices. V_{tlin} and V_{tsat} are following the gate length dependence, whereas I_{dsat} is driven by the operating voltage. The standard quantum-corrected drift–diffusion with a unique process and device model parameter set is used throughout the study including band-to-band tunneling, impact-ionization and thin-film mobility models [5]. Fig. 3 finally shows TCAD vs HW comparison in terms of F_t, F_{max} and gm for the under-drive device with a satisfactory agreement on a multi-finger structure. The definition of the RF FoMs F_t and F_{max} as well as the switch FoMs C_{off} and V_{max} can be seen in Fig. 3 additionally. With confidence in the initial TCAD ability to mimic measurements, it was used to optimize tradeoffs and obtain state-of-the-art performance.

3. Scaling effects in 22FDX® platform

To ensure low HCI degradation medium thick oxide devices have graded junctions to reduce the electrical field at the drain to gate edge. Fig. 4 shows the doping profile of two processes, P-1 and P-2 with a long, respectively short, extension of the high-doping region towards the gate. The graded junction shows up to 30 % peak electric field reduction under worse HCI conditions (V_{DS} = V_{GS} = 1.2 V) which is important for power amplifier and digital I/O, but less for switch devices. On the other

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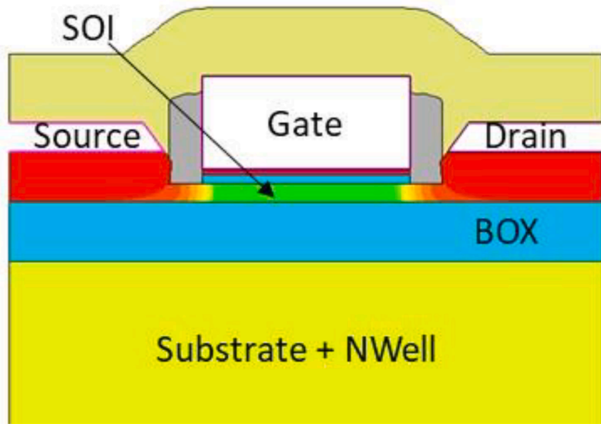

Fig. 1. TCAD device structure and doping profile.

hand, having a more abrupt doping profile improves the threshold voltage roll-off and reduces DIBL, thus enabling shorter gates with good electrostatic behavior (Fig. 5). Since the under-driven device gives margin to pass the HCI criteria (driven by the lower V_{DD}) the more abrupt doping profile of P-2 combining with a shrink in the gate length will still be sufficient. Furthermore, the Drain leakage current and the device linear resistance at constant gate bias ($R_{on,DC}$) is significantly reduced (Fig. 6). The $R_{on,DC}$ reduction is driven by a better channel mobility due to the absence of dopants in the portion of channel under the gate (Fig. 7). Fig. 8 is showing the electron velocity along the channel which is following the mobility increase. At the connection of the source and drain to the channel a local velocity can be observed due to the higher electrical field in these regions. The overlap and magnitude of the source/drain doping is still enough to have a low channel access resistance. P-1 and P-2 processes minimize R_{on} with gate length reduction having same slope, which means P-1 performance is worse, since V_{tlin} scaling is stronger. A better electrostatic behavior of P-2 (lower sub-threshold slope due to larger effective channel) results in the leakage current reduction and slightly higher Vth. The steeper junction does not affect the leakage current of the investigated devices since they work in the sub-threshold regime rather than in GIDL regime. Regarding to the RF FoMs in Fig. 9, F_t shows a stable monotonic upward trend against gate scaling while gate overlap has negligible impact. This means the change from P-1 to P-2 has little impact on Ft. In contrast to the gate length scaling enabled by P-2 it can increase Ft significantly. F_{max} has limited enhancement as the device is scaled down, particularly with P-2 process. This is because the gate resistance contributes to Fmax profoundly even though Ft improvement would benefit to it. However, F_{max} is saturating for the shortest gates. In this paper, 2D TCAD simulations use a gate length dependent lumped resistance at the gate contact to mimic the vertical and horizontal resistance of the 3D structure according to measured and simulated values. Fig. 10 shows that significant improvements in F_t and F_{max} are achieved at high drain current and less, but still visible, at low drain currents for a combination of shorter gates and P-2. The minimum gate length possible will additionally be defined by the application specific reliability criterion and might therefore differ. Here, off-state TDDB might be more important for switch devices with dependencies on breakdown voltage and the electrical field across the gate dielectric.

3.1. Switch application

Depending on the application and design specifications, device selections for switch applications can be different combinations of the gate

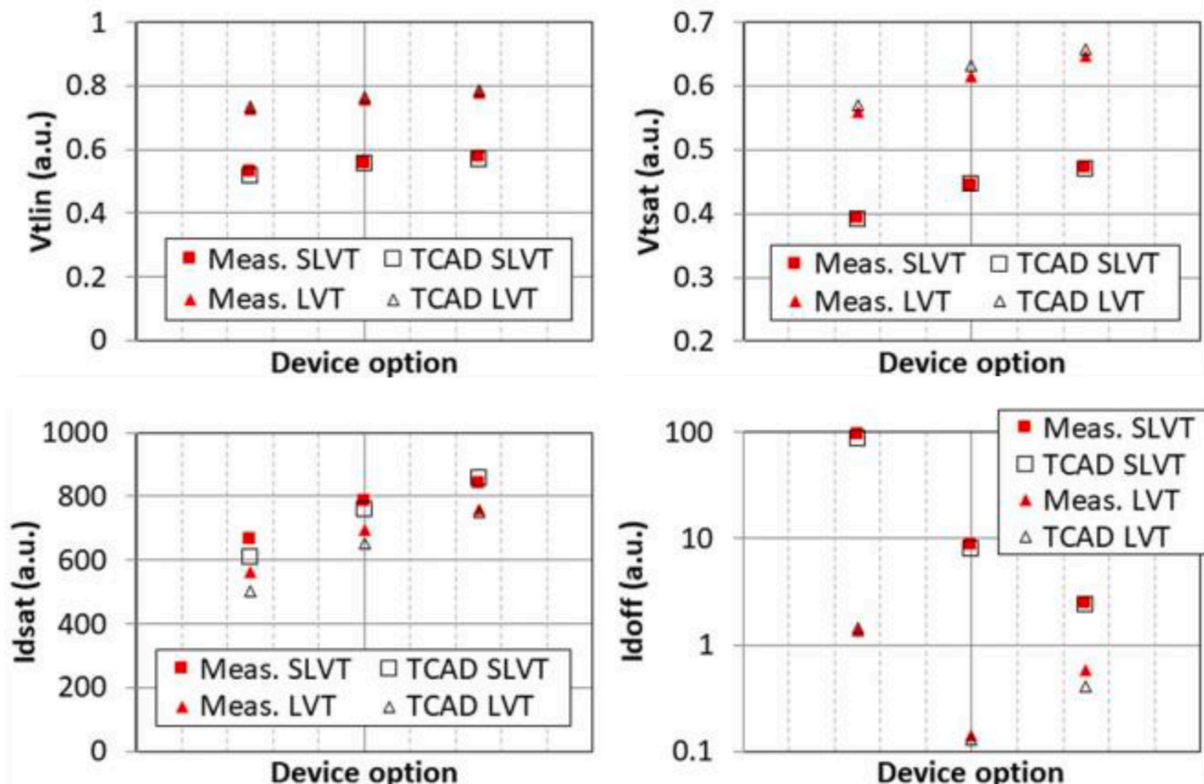

Fig. 2. DC calibration (TCAD – open / HW – filled *sym.*).

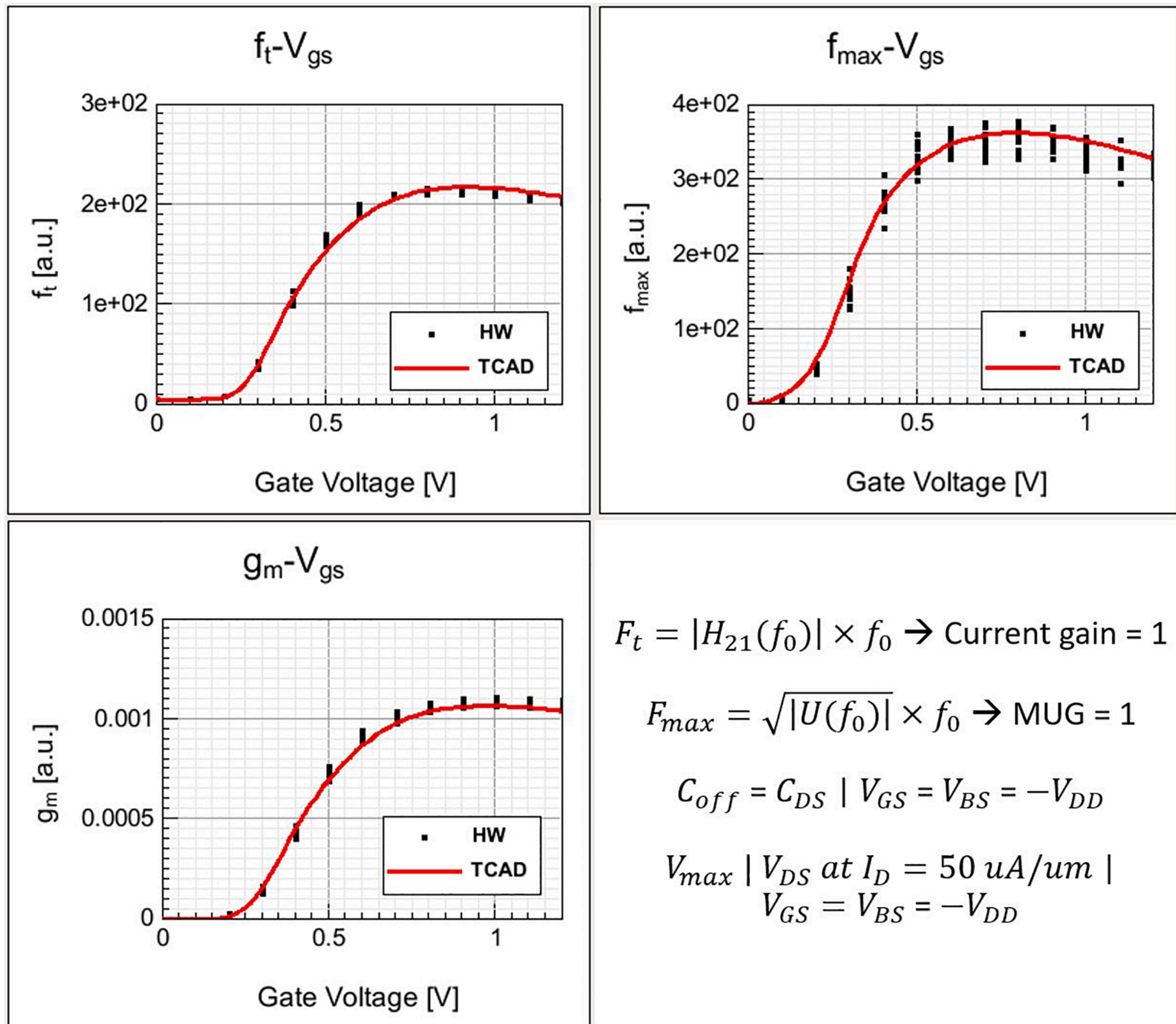

Fig. 3. RF calibration and FoM extraction methods (TCAD - solid line / HW - squares).

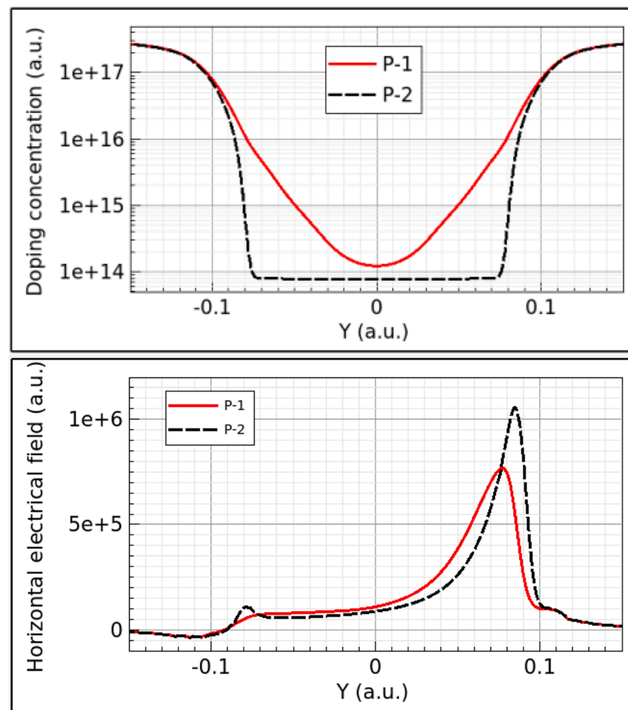

Fig. 4. Doping profile and horizontal electrical field at $V_{DS} = V_{GS} = 1.2$ V for *P*-1 and P-2 process.

oxide thickness, gate lengths as well as back gate constructions. Commonly, devices in the switch application are stacked together to resist high voltage swing exceeding a single device operation voltage. To screen possible device constructions for switches, single devices combined with parasitic elements like decoupling resistors is analyzed in this paper. C_{off} and Ron are extracted from the mixed-mode small-signal simulations. Whereas C_{off} is a measure of the switch isolation calculated out of Y_{12}-Parameter in off-conditions (Fig. 3). In the simulation, the device drain is assigned as port 1 while the source is port 2. $R_{on,AC}$ represents the insertion loss when the switch is on. It is extracted from Y_{12} when V_{DD} at the gate and zero drain voltage applied. Fig. 11 depicts the C_{off}*$R_{on,AC}$ FoM for switch application [6], which is reduced with shorter gates and P-2 process resulting in an improvement due to better isolation (lower C_{off}) and less insertion loss (lower $R_{on,AC}$). The improvement is mainly driven by the Ron lowering, since C_{off} is reduced with P-2 process itself (less drain overlap – less substrate coupling) but does not reduce with gate length scaling. Due to the weak source to drain coupling in FDSOI technology, C_{off} does also not significantly increase for shorter channel length. Furthermore, the leakage current is only marginally increased at the same threshold voltage, but shorter gate length. The drain breakdown voltage can be maintained at a high level visible in the C_{off}*$R_{on,AC}/V_{max}$ metric down to −30 nm L_G. V_{max} is a measure of which drain bias the device can withstand and can be defined as shown in Fig. 3. Going to even shorter gates lead to a slight increase in this FoM pointing to a drop in V_{max} as expected for gate length scaling. The P-1 process shows this increase already for longer gates. Using LVT

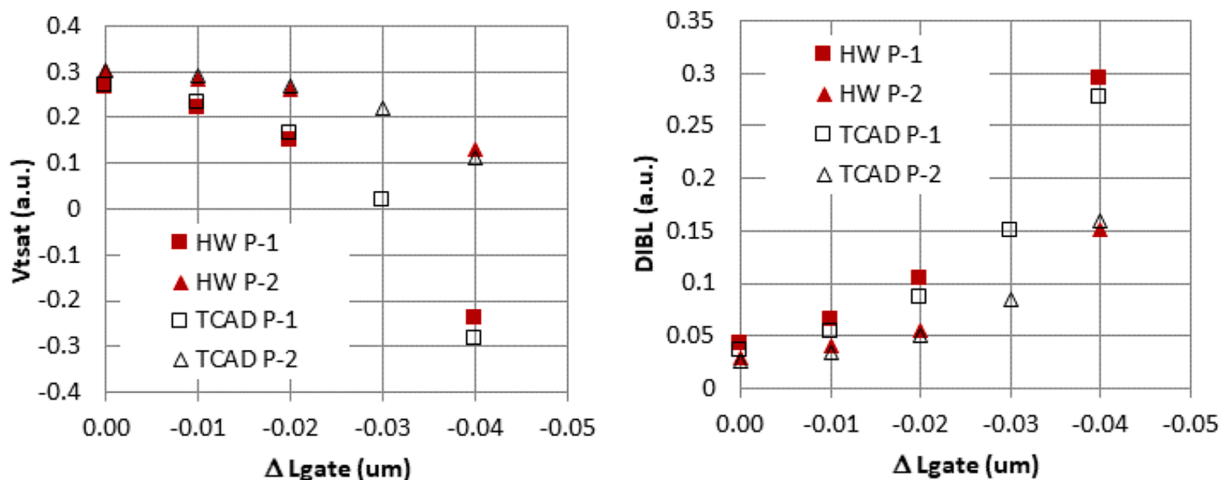

Fig. 5. Saturation threshold voltage and DIBL.

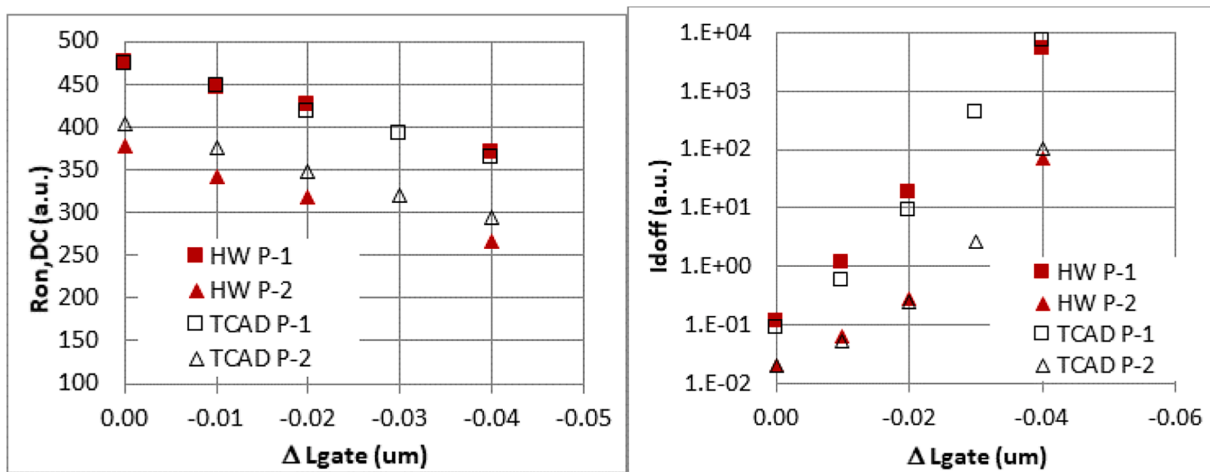

Fig. 6. $R_{on,DC}$ and Drain leakage current.

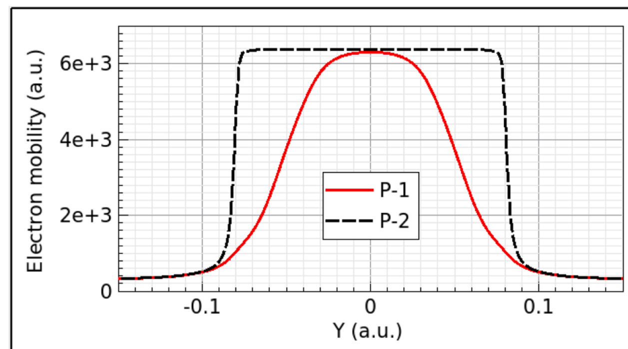

Fig. 7. Electron mobility along the channel (linear regime).

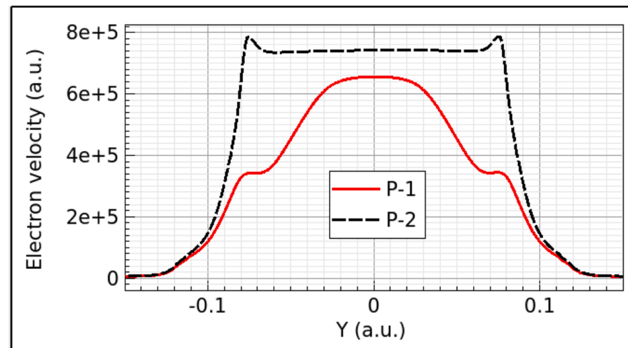

Fig. 8. Electron velocity along the channel (linear regime).

device construction would further reduce the leakage current and increases the threshold voltage at marginally lower C_{off}*$R_{on,AC}$ and C_{off}*$R_{on,AC}$/V_{max}, later FoM saturating for P-2 at about −30 nm gate length due to higher breakdown voltages. At the minimum R_{on}*C_{off}/V_{max} point this FoM is improved by ~ 20 % and R_{on}*C_{off} by ~ 30 %. The simulation data shows encouraging results for a switch device candidate and the device implementation in switch design needs to be further studied.

3.2. *High-performance amplifier application*

Besides the switch application, the power amplifier (PA) is another key design building block for the device performance optimization. Despite the $R_{on,DC}$ discussed previously, the gate capacitance (C_{GG}), miller capacitance (C_{GD}) and leakage current are also important in designing a PA. The steeper doping profile of P-2 reduces the gate-drain capacitance (C_{GD}) and the gate scaling benefits the overall C_{GG}, illustrated in Fig. 12. This does explain the observed increase in F_t. I_{doff} and $R_{on,DC}$ have already been shown to reduce with P-2 process later one also with gate length scaling. Combining the back bias (BB) capability of FDSOI devices, further reduction of the drain leakage (reverse BB) at little cost of $R_{on,DC}$ can be achieved and makes it attractive to PA applications (Fig. 12).

4. Conclusion

The well-known gate scaling combined with a process option which

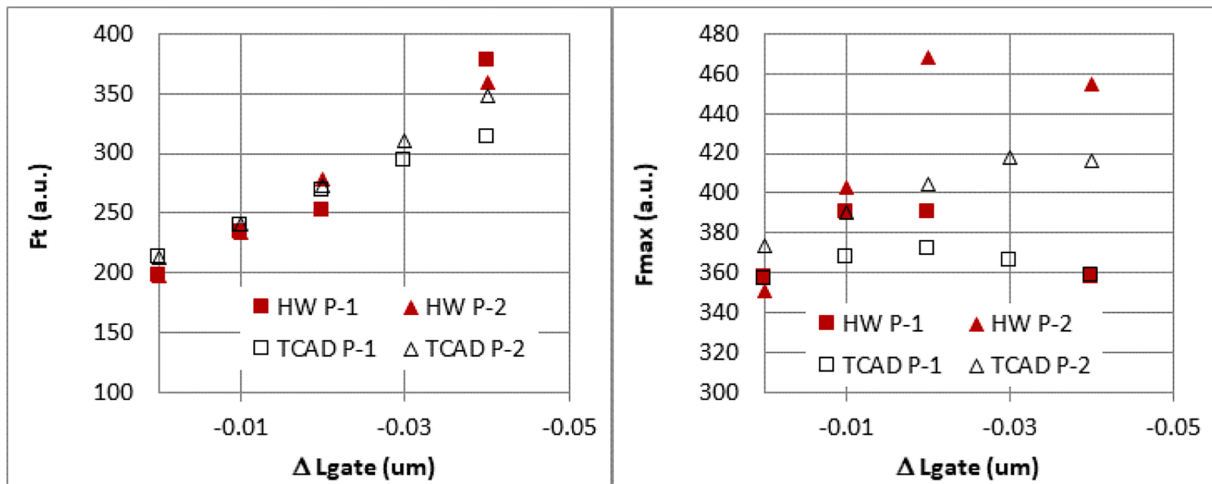

Fig. 9. F_t and F_{max} scaling.

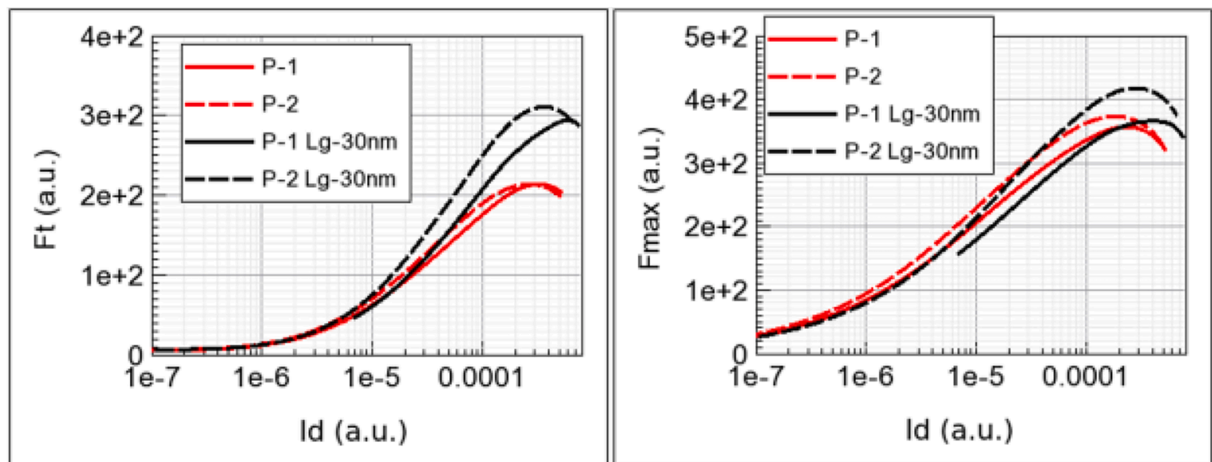

Fig. 10. F_t and $/F_{max}$ vs drain current for *P*-1/P-2 process and two gate length at $V_{DS} = 1.2$ V.

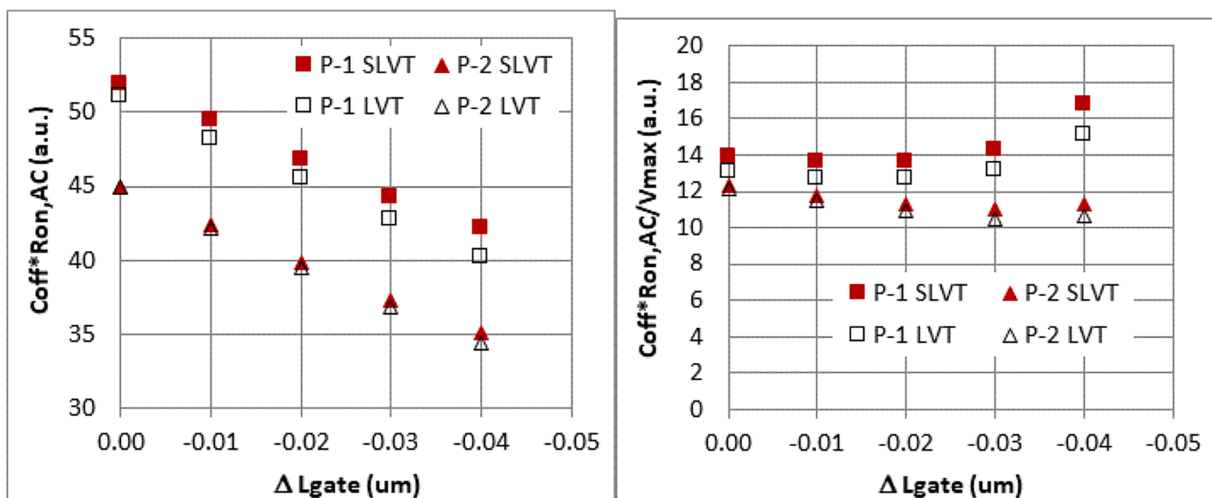

Fig. 11. C_{off}*$R_{on,AC}$ and C_{off}*$R_{on,AC}/V_{max}$ for *P*-1/P-2 process and n/pwell back gate doping.

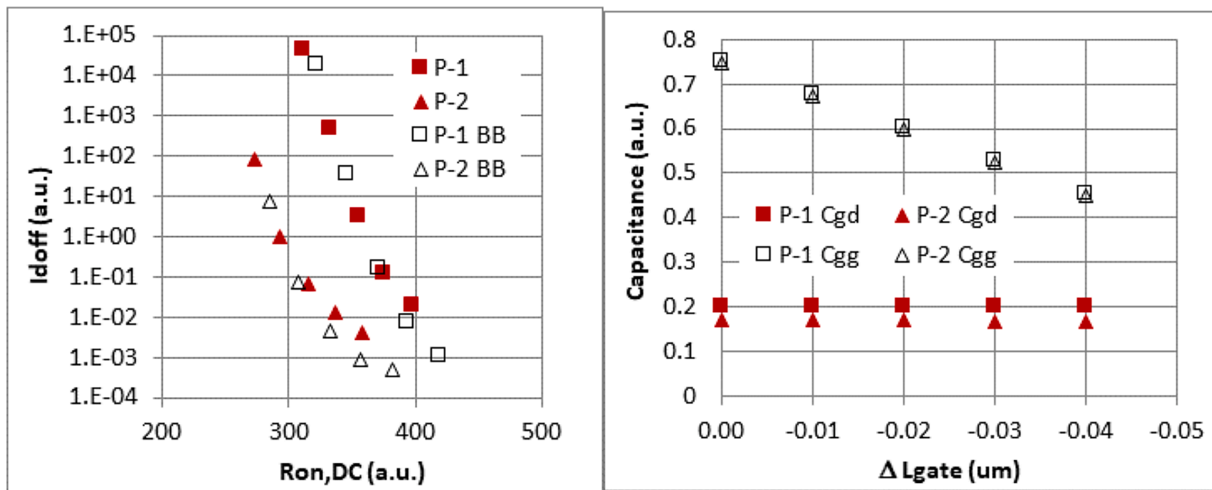

Fig. 12. $I_{doff}/R_{on,DC}$ for V_{BS} = 0 V/-0.8 V(BB) for different gate length and C_{GD} (V_{GS} = 0 V)/C_{GG} (V_{GS} = 1.2 V).

enables steeper source and drain junctions could significantly improve $R_{on,DC}$, F_t and C_{off}*$R_{on,AC}/V_{max}$ while keeping the HCI reliability within the specification. Those single device figures of merit show encouraging results for device usage in switches and high-performance power amplifiers.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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