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DTCO flow for air spacer generation and its impact on power and performance at N7☆

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ABSTRACT

A novel DTCO flow is described with the principal aim to study the impact of air spacer fabrication on the power and performance of a 5-stage inverter ring oscillator at the 7 nm node. The flow incorporates physical and analytical process models from the in-house ViennaPS simulation tool together with device and circuit simulations from GTS Framework's Cell Designer. The air spacer is usually filled by sequential conformal and non-conformal deposition steps. The impact of the thickness of the conformal layer and the sticking probability during non-conformal deposition on the ring oscillator performance is studied here. The air gap, which forms the core of the air spacer, is generated during the non-conformal deposition step. We extract the relative effective permittivity of the air spacer as a function of these two fabrication parameters by solving the Poisson equation to obtain the spacer capacitance. Finally, SPICE model cards are extracted automatically from the TCAD transistor characteristics and the parasitic network is calculated from the full 3D ring oscillator logic cell using a field solver. We apply our framework on two fabrication flows, when the air gap is created before and after the deposition of the first metal contacts layer. We observe that introducing the air gap inside the spacer results in an at-least 15% improvement in the ring oscillator's performance, when the power is kept constant. Further improvements can be achieved by reducing the conformal layer thickness and increasing the sticking probability by increasing the chamber partial pressure or increasing the process temperature.

1. Introduction

The simulation of semiconductor fabrication steps using process technology computers aided design (TCAD) has become an integral component of designing and testing novel devices within the design-technology cooptimization (DTCO) cycle. Understanding even a single fabrication step's impact on the geometry of a desired device can further inform the circuit designer of its impact on the device and circuit performance. This information is then fed back to the fabrications engineer in order to adapt the process for improved circuit performance. However, attempting to implement this feedback loop using experiments alone result in time- and cost-intensive studies, making them largely unfeasible. Therefore, the integration of process simulations with device and circuit simulations through DTCO is essential for the successful design of future semiconductor devices and technologies [1].

In this manuscript, we describe a novel DTCO flow and apply it to study the impact of spacers with an air gap (AG), known as air spacers (ASs), on the circuit-level power and performance at the 7 nm node, using a 5-stage ring oscillator (RO) as a prototype circuit. The effective spacer capacitance, C_{eff}, is a limiting factor in the achievable frequency $f \propto 1/C_{\text{eff}}$ and possible power reduction $P \propto C_{\text{eff}}$ of the oscillator circuit [2]. The primary goal is the reduction of the effective spacer capacitance through the reduction of the effective AS permittivity.

It is essential to understand process variations and the limitations in reducing the capacitance imposed by the fabrication of the AS, when designing the RO circuit. The main fabrication parameters which impact the AG geometry are the (effective) sticking probability s during deposition and the thickness of the conformally-deposited SiN layer t_c which determines the width of the spacer trench prior to the non-conformal deposition step which forms the AG. The probability that an impinging atom sticks to the surface derives from the kinetic theory of ideal gases is shown to be proportional to the partial pressure and inversely proportional to the squared root of the chamber temperature [3]. Therefore, since s is directly related to the fabrication condition in the chemical vapor deposition (CVD) chamber,

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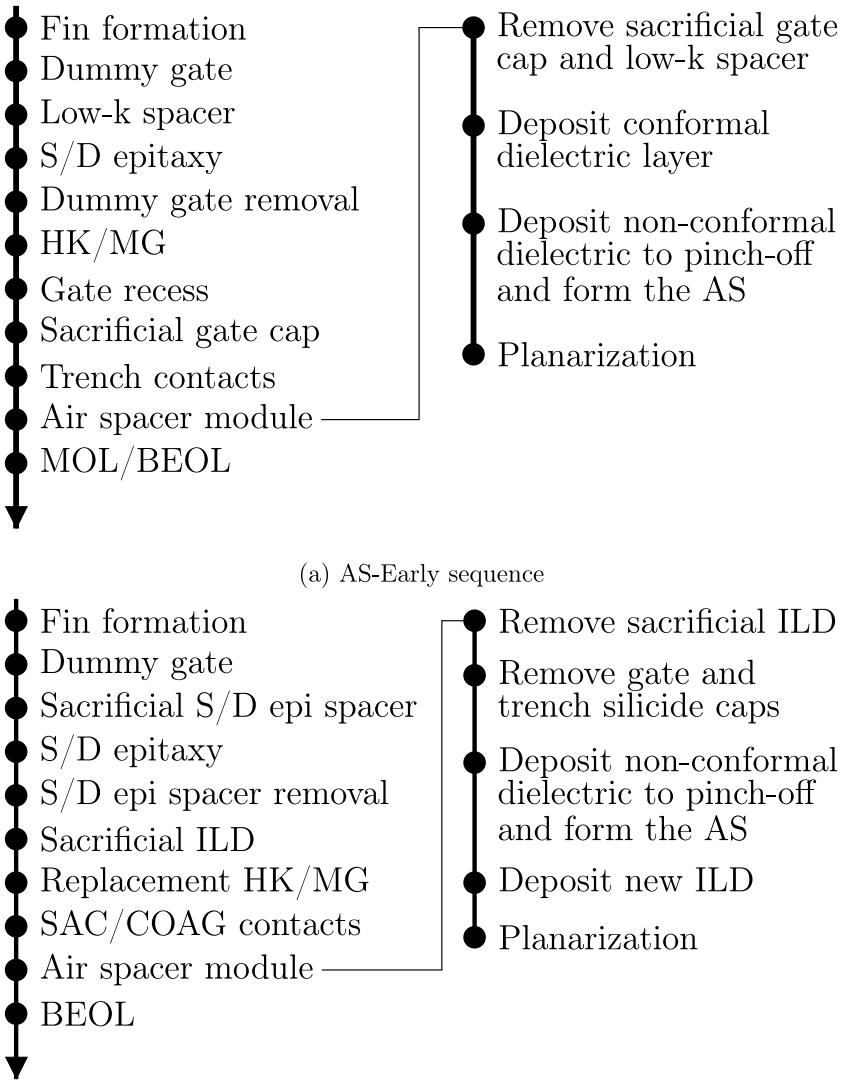

Fig. 1. Fabrication sequence of the key process steps for two types of AS integration, mainly (a) AS-Early and (b) AS-Late. The principal difference in AS-Late is that the air gap is formed after the MOL contacts.

this provides a direct link between circuit-level performance and the fabrication conditions [4]. It is particularly important to study novel fabrication approaches, such as the AS-Late scheme from Cheng et al. [2], in order to ensure that these are still able to provide the benefits observed by well-established techniques.

2. Fabrication sequence

The developed DTCO simulation flow is applied towards the generation of the air spacer for two different fabrication sequences, termed AS-Early [5] (see Fig. 1a) and AS-Late [2] (see Fig. 1b). The principal difference here is that the AS-Late sequence conforms to modern techniques of self-aligned contact (SAC) and contact over active gate (COAG) during middle of line (MOL) contact deposition. With this method, a sacrificial inter-layer dielectric (ILD) is deposited during source/drain (S/D) formation and is composed of a $SiN/SiO_2/SiN$ stack, where only the SiO_2 is sacrificial, while the SiN layers form the initial conformal AS film [2]. After the sacrificial ILD deposition, the high-k/metal gate (HK/MG) is formed. In the AS-Early sequence, the contacts are formed during the back-end-of-line (BEOL) step [5].

3. Simulation flow

The simulation of the fabrication-induced variation in the RO performance using physics-based deposition models is not feasible, since physical process models require a time- and memory-intensive Monte Carlo (MC) ray tracing and level set (LS) approach [6]. Therefore, we first perform a set of physical simulations in order to generate an analytical model for non-conformal CVD [7], which is based on these physics-based models, as implemented in ViennaPS [8]. The analytical model is subsequently applied in the full DTCO flow in order to study the impact of the relevant fabrication parameters on the circuit performance. The critical steps in the workflow, as shown in Fig. 2, are described in this section.

3.1. Physical topography simulation

The full physical simulation for the generation of the AG in the spacer is based on a LS-powered topography simulator, together with top-down MC ray tracing for the simulation of non-conformal CVD [9]. Initially, a conformal layer of width t_c is deposited in the spacer trench, which can be modeled using physical or analytical approaches.

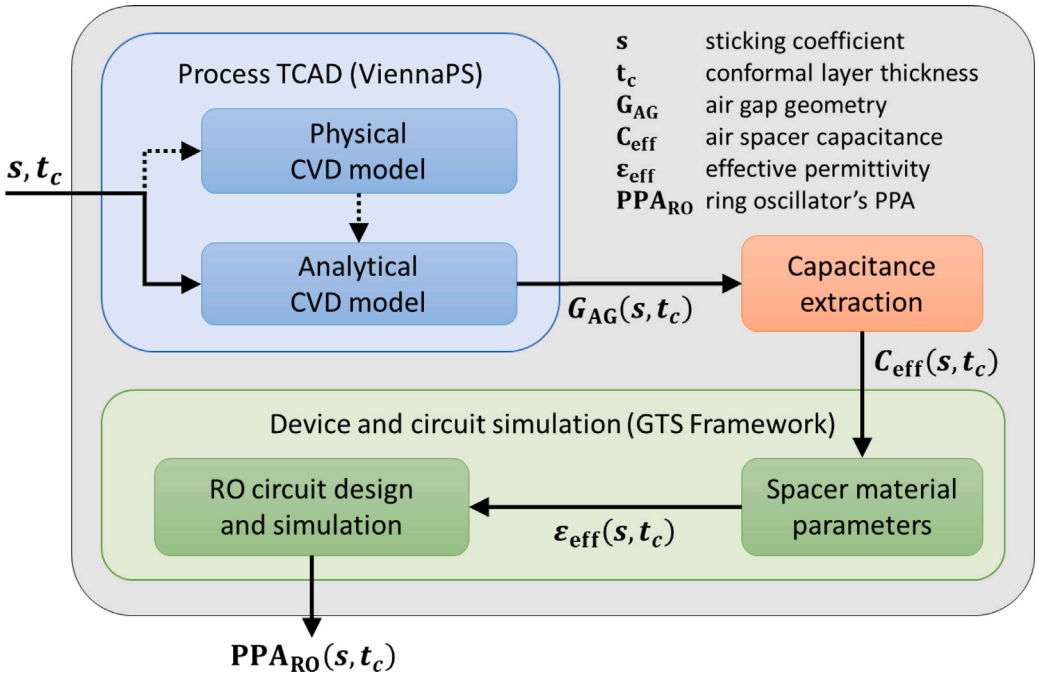

Fig. 2. Flowchart showing the presented DTCO workflow (solid arrow) for AS generation for a 5-stage inverter RO logic cell. The dotted arrow shows the development of the analytical model, which is based on a calibrated physical model. The main input parameters are the sticking probability s and conformal SiN layer thickness t_c, which are used to generate the air spacer geometry G_{AS}. The impact of the studied fabrication parameters (s, t_c) on the circuit power and performance are then provided using a PPA chart.

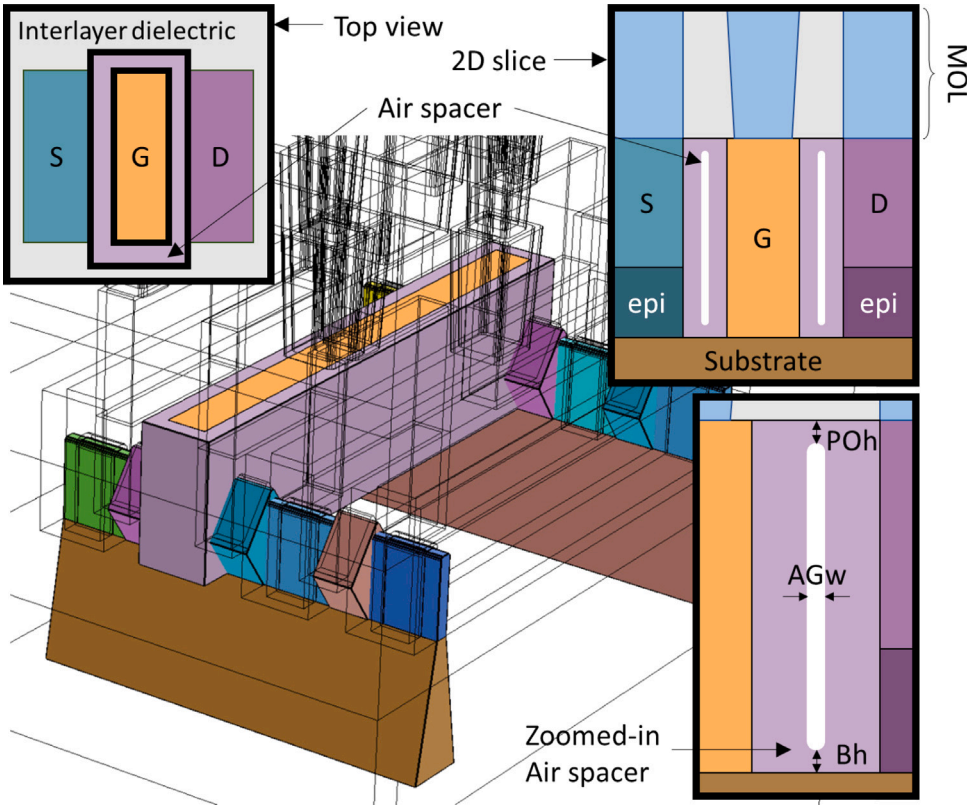

Fig. 3. Inverter cell with highlighted gate line and spacer regions. The insets show the spacer structure between source (S) and drain (D) regions, encircling the gate (G), below the MOL contacts. On the bottom right, the air spacer is shown with typical measurements for the pinch-off height (POh), bottom height (Bh) and the air gap width (AGw). These physical parameters are used to define the geometry of the air spacer G_{AS}.

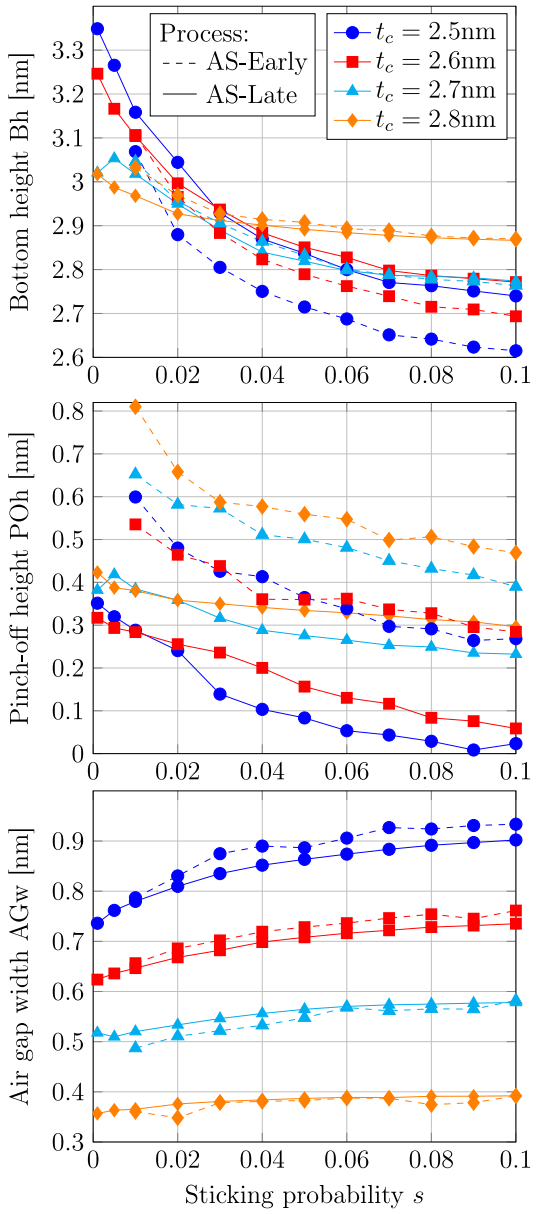

Fig. 4. Impact of s and t_c on the shape of the resulting air spacer geometry, including the bottom height (Bh), pinch-off height (POh), and the air gap width (AGw), as shown in Fig. 3. The symbols and lines show the results using the physical and analytical CVD models, respectively, while the dashed and solid lines show the results using the AS-Early and AS-Late processes, respectively.

After this, non-conformal CVD is applied using a single-particle-type approach, where the particle has a specific sticking probability s which describes its propensity to adsorb onto the surface [10]. Higher s values represent higher non-linearities which ensure that the gap is pinched off at the top. Several physical simulations are performed while varying t_c and s in order to subsequently devise a fast analytical model using the generated geometries.

3.2. Geometrical description of the air gap

The principal aim of the analytical model is to reproduce the geometrical shape of the AG inside the spacer by reproducing the pinch-off height (POh), bottom height (Bh), and air gap width (AGw) from the physical CVD model (Fig. 3). This model also applies a linear interpolation for the air gap's geometrical parameters for s and t_c values

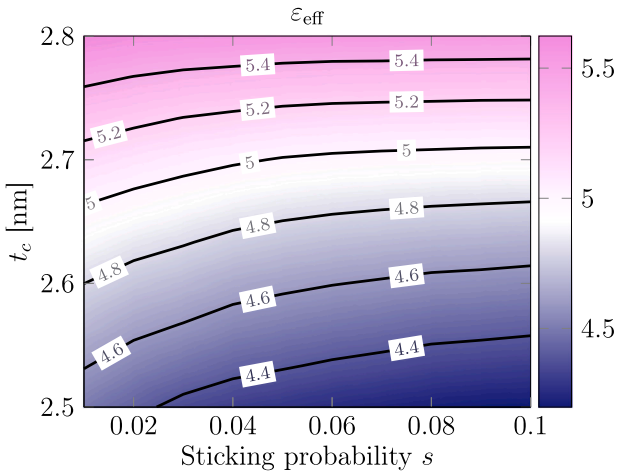

Fig. 5. The impact of the sticking probability s and conformal layer thickness t_c during air gap formation on the effective relative permittivity ε_{eff} of the air spacer using the AS-Late fabrication flow. We have also observed that the AS-Early flow shows very similar results with ε_{eff} ranging from about 4.16 to 5.66 as s and t_c are varied. Therefore, increasing s and reducing t_c leads to lowest ε_{eff} values.

which have not been simulated with the physical model. The air gap's shape is represented using a superellipse centered at $(0,0)$ with radii r_x and r_y along the x and y axes, respectively, using the equation

$$y = \pm r_y \sqrt[4]{1 - \left|\frac{x}{r_x}\right|^4}. \tag{1}$$

3.3. Analytical topography simulation

In our DTCO flow, the complete AS is generated by first assuming a fully-filled SiN spacer and then performing a Boolean operation to remove the AG geometry from the spacer region. The AG geometry follows Eq. (1) while its vertical placement depends on the physically-modeled values of POh and Bh. This method allows to reproduce the physical AS model with high accuracy, as shown in Fig. 4, while requiring a fraction of the simulation time. The analytical model showed a speedup of about 100 times, which is consistent with our previous studies [7].

3.4. Capacitance extraction

The capacitance across the generated AS is calculated by solving the Poisson equation, which allows to extract a relationship between the capacitance and the chosen fabrication parameters. Ultimately, the calculated capacitance is used to extract an effective relative permittivity ε_{eff} of the AS, which contains an AG surrounded by SiN. The range of ε_{eff} we observe for the tested fabrication conditions is from about 4.2 to 5.7, as shown in Fig. 5, while a pure SiN spacer exhibits an ε_{eff} of 7.4, displaying a clear benefit to AS integration.

3.5. Power-performance analysis

With the calculated ε_{eff} values, a PPA of a 5-stage inverter RO logic cell is performed assuming varying fabrication conditions. The SPICE model cards are extracted automatically from the TCAD transistor characteristics and the parasitics network is calculated from the full three-dimensional (3D) RO cell using a field solver. Applying this method, any change in capacitance can be captured in a consistent manner [1,11]. As expected, the results clearly show that the introduction of an air gap (AG) in the spacer results in an improvement in the power and achievable frequency for both fabrication sequences AS-Early and AS-Late, as shown in Fig. 6.

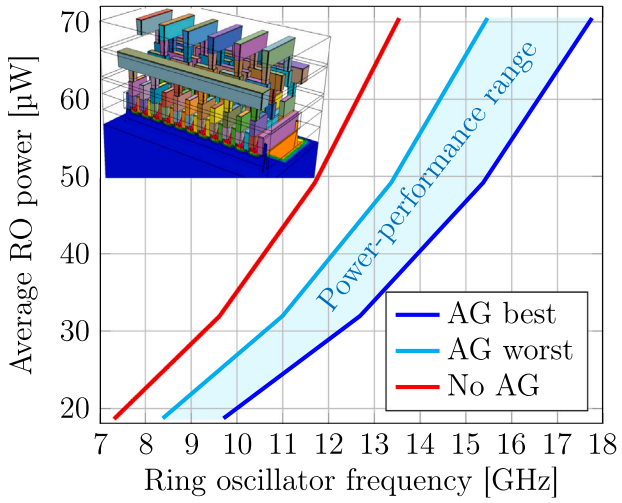

Fig. 6. Achieved power and performance for the RO with no air gap (AG) and with an AG under best and worst tested process conditions. The best condition corresponds to an ϵ_{eff} of 4.2 when $(s, t_c) = (0.1, 2.5\,\text{nm})$. The worst condition has $\epsilon_{\text{eff}} = 5.7$ when $(s, t_c) = (0.02, 2.8\,\text{nm})$ in the AS-Early process. The case with no air gap corresponds to a completely filled SiN spacer. The inset shows the full RO cell.

4. Discussion and conclusion

A newly-developed DTCO framework is applied on two fabrication flows, both of which are compatible with complementary semiconductor-metal-oxide (CMOS) technology. For one, the air spacer is formed prior to the deposition of MOL contacts (AS-Early) [5] and for the second one the air spacer is formed after the deposition of MOL contacts (AS-Late) [2]. From Fig. 4 we note that both flows provide a similar air gap width, while the AS-Late-generated AG is shifted slightly up, due to the pinch-off location being slightly higher. A minimum conformal layer thickness of 2.5 nm was found to be most appropriate because it allows for the pinch-off to stay within the spacer region. Otherwise, it may encroach into the ILD layer between the MOL contacts.

The most significant impact on the spacer's effective relative permittivity comes from the AG width. This parameter is highly driven by the thickness of the conformally-deposited SiN layer. As can be observed from Fig. 5 the lowest permittivity is achieved when the sticking probability is high and the conformal layer thickness is low. These two factors essentially mean that the conformal deposition should set the width of the air gap, while the non-conformal deposition should only close the generated trench.

Finally, we observe the impact of the AS on a 5-stage inverter RO circuit using PPA in Fig. 6. The inclusion of the air gap improves the performance by about 15% in the worst case scenario. With the presented framework, we are able to apply DTCO studies all the way from 3D physical process simulations through to geometric analysis of the spacer's topography and finally to thorough device and circuit analysis.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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