Solid-State Electronics 199 (2023) 108490

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Characterization and modeling of drain lag using a modified RC network in the ASM-HEMT framework☆

Mohammad Sajid Nazir [a,*], Ahtisham Pampori [a], Raghvendra Dangi [a], Pragya Kushwaha [b], Ekta Yadav [b], Santanu Sinha [b], Yogesh Singh Chauhan [a]

[a] Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur, 208016, India
[b] Micro Electronics Group, Space Applications Centre, Indian Space Research Organisation, Ahmedabad, India

ARTICLE INFO

Keywords:
Advanced SPICE model (ASM) HEMT model
AlGaN/GaN high electron mobility transistor (HEMT)
Current degradation (CD)
Dynamic R_{ON}
Drain lag
Gate lag
Parasitic backgate
n_{2Deg}

ABSTRACT

Gallium-Nitride High Electron Mobility Transistors (GaN-HEMTs) are susceptible to trapping effects, significantly degrading device performance. The degradation can be seen in the current–voltage characteristics and also manifests in the form of a shift in the dynamic on-resistance and threshold voltage. In this paper, we present pulsed characterization and empirical modeling of a 250 × 10 μm RF GaN HEMT device. To study the impact of drain-induced trapping, pulse I-V characterization is performed at a fixed quiescent gate voltage of −7 V with varying drain quiescent voltage. An empirical RC network approach is proposed to accurately model the trapping in the device. The model effectively captures the impact of trapping and takes into account the self-limiting behavior of traps. The model is implemented in Verilog-A within the Advanced SPICE Model for High Electron Mobility Transistors (ASM-HEMT) framework. Validation of the model is done with six different quiescent conditions of pulse measurement with on-state drain bias varying from 0 V to 20 V.

1. Introduction

Gallium Nitride (GaN) based HEMTs have garnered considerable attention over the past few decades owing to their promising characteristics — high electron density, a high saturation velocity, a wide bandgap, and a high thermal conductivity.

In spite of its superior characteristics, there are still reliability issues associated with this device. Although efforts are made to improve the reliability of HEMTs [1], there is still a pronounced drawback — these devices suffer from charge trapping [2]. Charge trapping has a significant impact on device performance, as evidenced by the dynamic change in current when the device is operated at different drain-gate voltage biases [3].

It is believed that material defects and electron states at the surface act as trapping centres [4]. Usually, in HEMTs, trap centres can be presented as surface, interface, barrier layer, and buffer layer traps. Various phenomena have been recorded as a result of charges entering and exiting these traps, including Current Degradation (CD), low-frequency transconductance dispersion, gate lag, drain lag, and so on. Gate lag is most widely attributed to surface and barrier traps, while drain lag is attributed to buffer/substrate traps [5]. Traps under the gate predominantly change the threshold voltage, whereas traps in the drain gate access region determine the on-resistance [6].

GaN devices suffer from self-heating phenomena in addition to trapping, and together, the effects include a complex nonlinear dependence with regard to the instantaneous voltages applied at the device ports [7]. Iso-thermal HEMT characteristics are commonly determined using Pulsed-IV (PIV) measurements to avoid any heating effects in the device [8]. It allows one to observe the CD due to charge trapping only. There are several reports on trap modeling using both empirical [9] and physics-based approaches [10]. However, empirical trap models are often used in industry standard models because of their simplicity, accuracy, and robustness. The RC network approach is an empirical way to model charge trapping in devices, as given in [11]. The industry standard model ASM-HEMT [12,13] consists of several mutually exclusive, empirical trap RC models. However, none of the RC networks are able to capture the influence of parasitic back gate effects [14] and the self-limiting behaviour of traps on the process of trapping [15]. A comprehensive empirical RC network model that is able to adequately capture the dynamics involved in the device operation is missing in contemporary literature.

In this paper, we characterize a GaN HEMT device under multiple pulsed conditions and present a modified RC network-based model (Fig. 1), implemented in the ASM-HEMT framework, to capture trapping effects and their self-limiting behaviour. A single network is

☆ The review of this paper was arranged by Francisco Gamiz.

* Corresponding author.
E-mail address: sajidspr20@iitk.ac.in (M.S. Nazir).

https://doi.org/10.1016/j.sse.2022.108490

Available online 3 November 2022

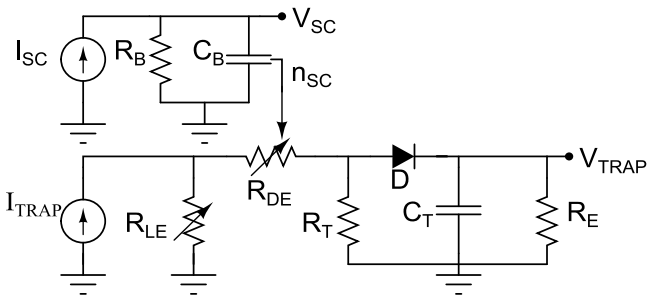

Fig. 1. RC network implemented to capture trapping dynamics. R_{DE} and R_{LE} are bias dependent and drain-access region n_{2Deg} dependent variable resistors.

implemented for trapping and de-trapping, with a diode being used to differentiate the two processes.

The modified RC network is validated with multiple pulsed IV measurements. To capture dynamic current behaviour for different quiescent bias conditions, our implementation incorporates new behavior for various ASM-HEMT parameters, including threshold voltage (V_{OFF}).

The paper proceeds as follows: Section 2 provides details about device characterization, Section 3 discusses the model and results, Section 4 outlines the extraction procedure, and the paper is concluded in Section 5.

2. Electrical characterization

Dual pulse measurements are performed using an AMCAD (AM3200) system (Fig. 2(a)) and the IVCAD suite is used for analysing measured data. Pulsed characterization of an RF GaN HEMT device (Fig. 2(b)) with gate length (L_g = 250 nm), width (W = 250 μm) and number of fingers (NF = 10) is performed. To observe current degradation with respect to time, quiescent voltages were set at (0 V, 0 V) and the device was measured at a bias of (−2.5 V, 10 V) over a pulse width of 20 μsec at a 20% duty-cycle. To study the impact of drain induced trapping, pulsed characterization is performed at a fixed gate quiescent (V_{GSQ}) of −7 V with varying drain quiescent bias (V_{DSQ} = 0 V, 7.5 V, 10 V, 15 V, 20 V and 25 V). For these measurements, a pulse width of 500 ns was applied in 100 ms pulse duration.

Table 1
Following parameters values are extracted after modeling the device.

Parameters	Extracted values
α_{SC} (℧)	1.0 u
α_1 (℧)	1.9
α_2 (V)	25.0 m
α_3	1.8
α_{FB} (V^{-1})	220.0 m
RC1	250.0 m
RC2	158.0 m

3. Model description and results

3.1. Model description

The main points taken into consideration in this study and modeling are:

- The majority of carriers are trapped during the off-stress period.
- When the device is turned on, the model traps additional carriers if the on-state voltage is greater than the stress voltage.
- Trapping in the on-state is mainly contributed by the channel formed under the gate. However, impact on overall characteristics depends on off-state stress conditions. On-state trapping is visible for V_{DSQ} = 0 V, where saturation currents show a flatter response than deeply stressed quiescent conditions.
- Carriers assumed to be trapped in the drain access-region are considered to be drain access-region electrons and electrons injected through the gate.
- Increase in the electric field under the gate is considered as a possible cause of trapping in the gate stack — eventually leading to a shift in the threshold voltage.
- Since surface passivation significantly reduces surface trapping, current degradation in the device can be also be attributed to parasitic backgate formation [14].
- The model includes variable resistors to account for self-limiting and parasitic back-gate formation behaviour — with one resistor being trap-potential dependent and the other 2-DEG-concentration dependent.

While the use of RC networks is a common approach to model trapping related current degradation [16–18], a model that takes the self-limiting behaviour of traps into account is still missing in the literature.

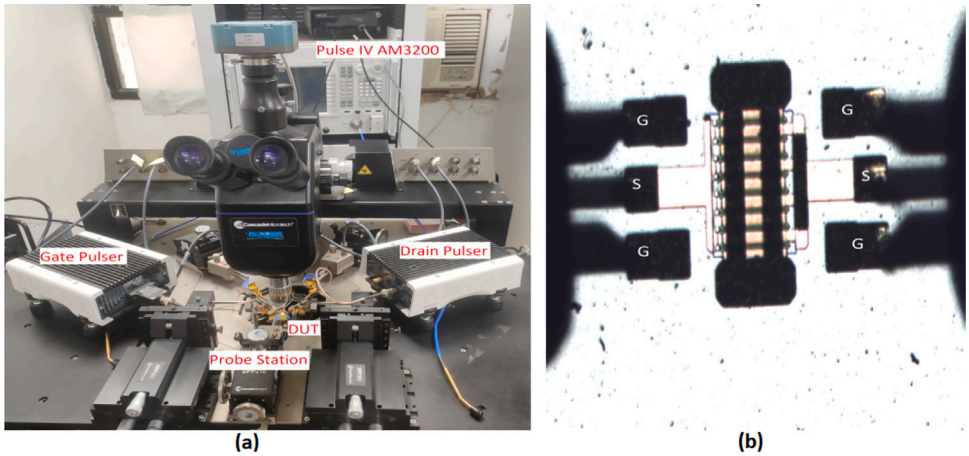

Fig. 2. (a) Measurement setup consisting of AMCAD Pulse IV System (AM3200), Drain Pulser (AM3221) and Gate Pulser (AM3211) (b) Device under Test (DUT).

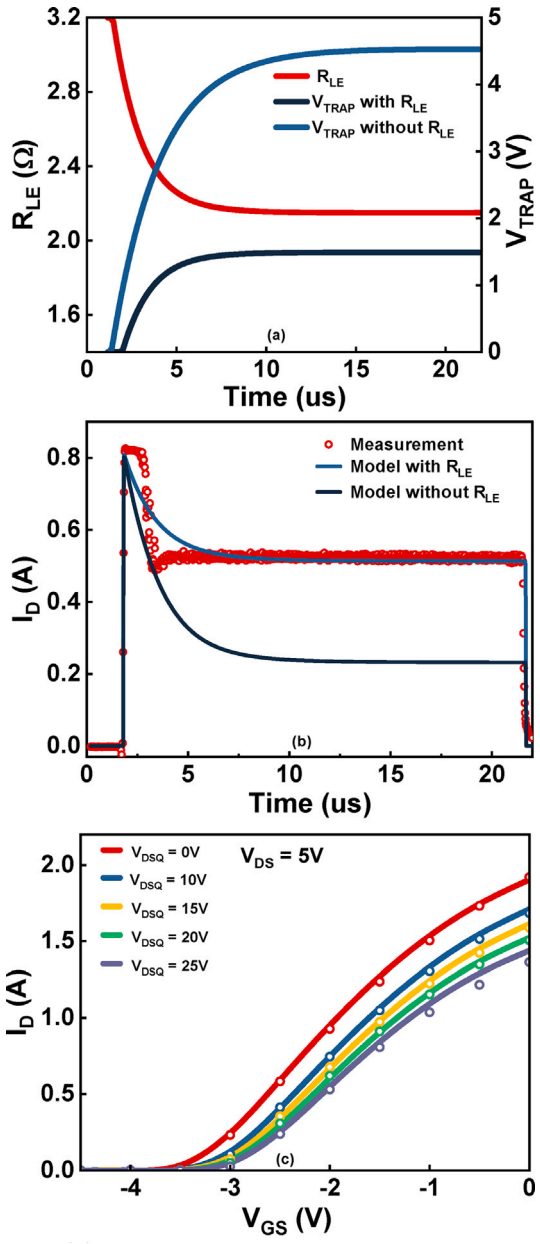

Fig. 3. (a) Behavior of trap potential with and without feedback network (b) Effect of trapping on drain current over a pulse width of 20 μs (c) Drain current vs Gate voltage at V_{DS}=5V for quiescent biases shown in legends.

The self-limiting behavior implies a condition where a trapped carrier generates an electrostatic potential that acts as a barrier for the incoming electrons, resulting in a decreased trapping probability [15]. Equivalent RC networks used to account for trapping without taking the self-limiting behaviour into account may not represent the variation of threshold voltage properly and can easily overestimate the dynamic R_{ON}. In our model, we introduce this effect using a negative feedback $R_{LE} = R_L(1-\alpha_{FB}V_{TRAP})$. Also, following from [14], drain bias induced space charge formation in the substrate can act as a parasitic back-gate (V_{SC}) — degrading the current by reducing the 2-DEG [19], and simultaneously changing the rate of trapping. This effect is included in the model using a variable resistor $R_{DE} = R_D * NS0ACCD/(NS0ACCD-n_{SC})$, where $NS0ACCD$ is the drain access region 2-DEG concentration and $n_{SC} = V_{SC} * C_B/q$.

As can be seen in Fig. 1, the existing RC network model in ASM HEMT [11,16] is modified to take these effects into account by making use of the parameters R_{LE} and R_{DE}. Fig. 3(a) shows the impact of R_{LE} on V_{TRAP} generated over time — as V_{TRAP} increases, negative feedback reduces R_{LE}, thus increasing current flow through R_{LE} and subsequently limiting the increase of V_{TRAP}. Fig. 3(b) shows impact of R_{LE} on drain current transient (DCT). Furthermore, R_E is kept at a higher value than R_T (emission time > capturing time) and a diode is utilised to ensure that the charging and discharging of C_T takes place along distinct pathways.

3.2. Results and discussion

Early on in the development of GaN HEMTs, changes in V_{OFF} were attributed mostly to surface states, which, when occupied, operated as a virtual gate. However, surface trapping is minimised significantly in state-of-the-art devices owing to surface passivation. As a result, the region of interest for studying CD effects remains the barrier, buffer, and substrate. The V_{OFF} shift is caused by V_{GSQ} — provided that electrons trap under the gate region. However, measurements performed in this paper demonstrate a V_{OFF} shift with variable V_{DSQ} at a fixed V_{GSQ} of −7 V. With an increasing V_{DSQ}, the device exhibits a higher R_{ON} and a significant positive shift in V_{OFF}. I. P. Singh et al. [20] have shown that with increasing drain bias, the electric field under gate increases proportionally. The electric field across the barrier substantially increases gate-currents due to Poole–Frenkel (PF) and Fowler–Nordheim tunnelling (FNT) [21]. This increase in gate-leakage currents activates the additional trapping centres under the gate and near the gate-drain region. Due to the drain bias, a change in threshold voltage can thus be attributed to the increased electric field under the gate. Further, R_{ON} of the device is affected by trapping in the drain access-region due to applied V_{DSQ} for a given stress period.

Validation of the proposed network for multiple quiescent conditions is shown in Figs. 3, 4, 5 and 6. Voltage dependent current sources (Eqs. (1) and (2)) and effective trap potentials used to modulate ASM-HEMT parameters are given by Eqs. (3) and (4).

$$I_{SC} = \alpha_{SC} * V(d) \tag{1}$$

$$I_{TRAP} = \alpha_1\sqrt{\alpha_2\ V(d)^{\alpha_3}} \tag{2}$$

$$V_{off1} = RC1 * V_{TRAP} \tag{3}$$

$$V_{off2} = RC2 * (V_{TRAP} + V_{sc}) \tag{4}$$

4. Extraction flow

With the quiescent condition of (V_{GSQ} : −7 V, V_{DSQ} : 0 V) chosen as reference, the initial set of ASM-HEMT parameters is extracted. The quiescent condition of (V_{GSQ} : −7 V, V_{DSQ} : 25 V) is then used to estimate the final values of trap parameters (α_{SC}, α_1, α_2, α_3, α_{FB},RC1,RC2), keeping the basic parameters obtained in the first extraction unchanged. The extracted values are given in Table 1. To simplify the extraction procedure, the trap potential is stored in two variables V_{off1} and V_{off2}. V_{off1} is used to modulate the parameter $VOFF$ and V_{off2} to emulate the effect of trapping on DIBL, mobility, saturation velocity and access region parameters.

5. Conclusion

We presented the characterization and modeling of drain-lag effects in AlGaN/GaN HEMTs using a self-limiting trapping model. The proposed model works well under all quiescent conditions and can be extended for gate-lag by changing the voltage dependence of the current sources from drain to gate.

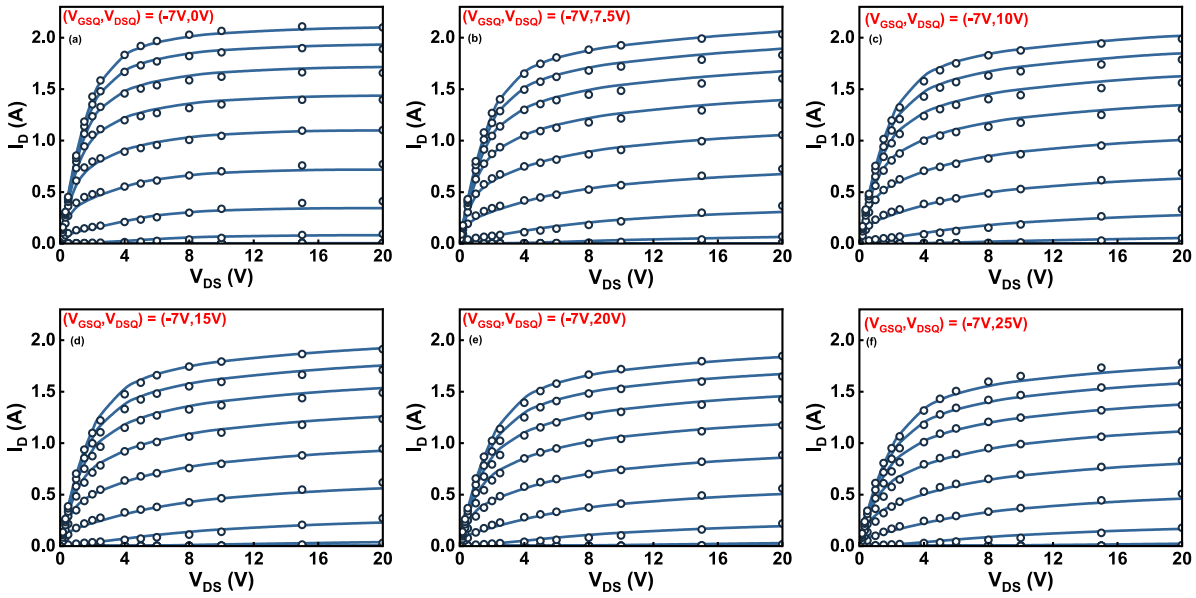

Fig. 4. Measurement (Symbols) and Simulated (Solid lines): (a)–(f) Pulsed output characteristics for V_{GS} (−7 V to 1 V, step = 0.5 V) under the following quiescent bias points: $(V_{GSQ}, V_{DSQ}) = (-7\ \text{V}, 0\ \text{V}), (V_{GSQ}, V_{DSQ}) = (-7\ \text{V}, 7.5V), V_{DSQ} = (-7\ \text{V}, 10\ \text{V}), (V_{GSQ}, V_{DSQ}) = (-7\ \text{V}, 15V), (V_{GSQ}, V_{DSQ}) = (-7\ \text{V}, 20\ \text{V}), (V_{GSQ}, V_{DSQ}) = (-7\ \text{V}, 25\ \text{V})$.

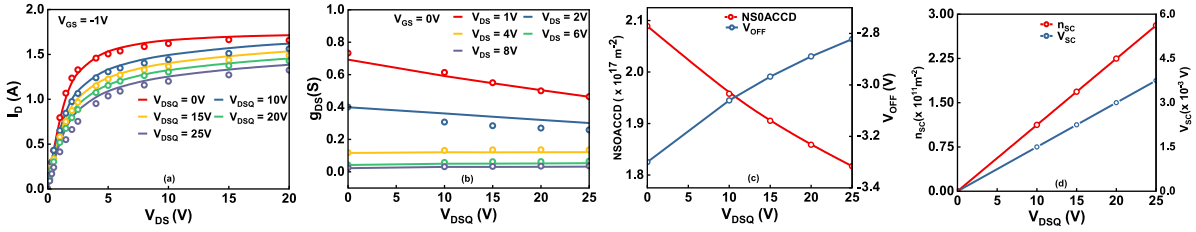

Fig. 5. (a)–(b) Measurement (symbols) and Simulated (Solid lines). (a) Drain current vs. Drain Voltage for quiescent biases shown in the legend. Variation of (b) Dynamic conductance (c) Access region 2DEG concentration and threshold voltage, and (d) potential V_{SC} and parameter n_{SC} with drain quiescent conditions.

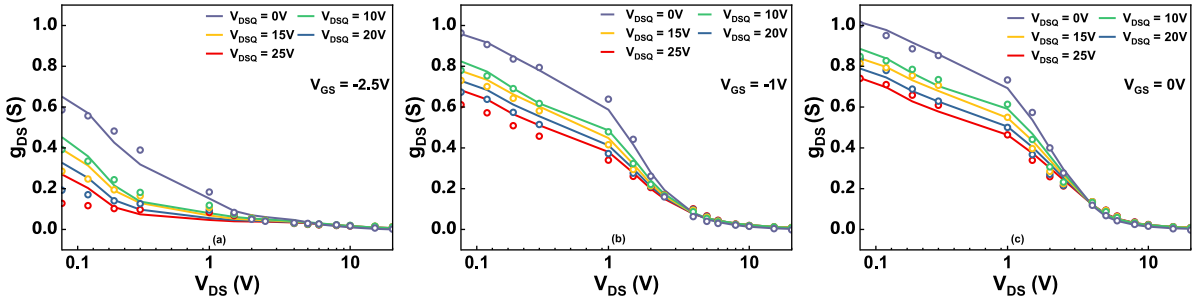

Fig. 6. Measurement (Symbols) and Simulated (Solid lines) (a)–(c) Dynamic conductance of the device at different gate voltages (−2.5 V, -1 V and 0 V).

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Author reports financial support was provided by Space Applications Centre, Indian Space Research Organisaton (ISRO).

Data availability

The data that has been used is confidential.

References

[1] Bisi, et al. IEEE TED 2013;60(10):3166–75. http://dx.doi.org/10.1109/TED.2013.2279021.
[2] Meneghini M, et al. IEEE BCICTS 2021;1–4. http://dx.doi.org/10.1109/BCICTS50416.2021.9682455.
[3] Angelotti AM, et al. IEEE TED 2020;67(8):3069–74. http://dx.doi.org/10.1109/TED.2020.3000983.
[4] Mitrofanov, et al. 34. 2003. p.33–53. http://dx.doi.org/10.1016/j.spmi.2003.12.002.
[5] Syamal, et al. IEEE TED 2016;63:1–8. http://dx.doi.org/10.1109/TED.2016.2533165.
[6] Bisi, et al. IEEE TED 2013;60:3166–75. http://dx.doi.org/10.1109/TED.2013.2279021.
[7] Florian C, et al. IEEE TMTT 2017;65(12):5046–62. http://dx.doi.org/10.1109/TMTT.2017.2723003.
[8] Kellogg K, et al. ARFTG 2020;1–4. http://dx.doi.org/10.1109/ARFTG47584.2020.9071731.
[9] Huang, et al. 2017. p. 248-251, http://dx.doi.org/10.1109/MWSYM.2017.8059087.
[10] Albahrani SA, et al. IEEE TED 2019;66(1):87–94. http://dx.doi.org/10.1109/TED.2018.2868261.

[11] Aamir Ahsan S, et al. IEEE JEDS 2017;5(5):310–9. http://dx.doi.org/10.1109/JEDS.2017.2724839.
[12] Khandelwal S, et al. IEEE TED 2019;66(1):80–6. http://dx.doi.org/10.1109/TED.2018.2867874.
[13] Aamir Ahsan S, et al. IEEE JEDS 2017;5(5):310–9. http://dx.doi.org/10.1109/JEDS.2017.2724839.
[14] Sghaier, et al. MJ 2006;37(4):363–70. http://dx.doi.org/10.1016/j.mejo.2005.05.014.
[15] Wosinski T. J Appl Phys 1989;65(4):1566–70.
[16] Agnihotri S, et al. IEEE INDICON 2015;2015:1–4. http://dx.doi.org/10.1109/INDICON.2015.7443658.
[17] Couvidat J, et al. IEEE/MTT-S IMS 2018;720–3. http://dx.doi.org/10.1109/MWSYM.2018.8439142.
[18] Jardel, et al. TMTT, IEEE Tran. 2007;55:2660–9. http://dx.doi.org/10.1109/TMTT.2007.907141.
[19] Wang, et al. JCS. 2014;13:872–6. http://dx.doi.org/10.1007/s10825-014-0603-y.
[20] Singh IP, et al. IEEE TED 2021;68(2):503–9. http://dx.doi.org/10.1109/TED.2020.3045685.
[21] Apurba Chakraborty, et al. EML 2016;12(2):232–6. http://dx.doi.org/10.1007/s13391-015-5249-9.