Solid-State Electronics 201 (2023) 108586

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

CARAT – A reliability analysis framework for BTI-HCD aging in circuits

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ARTICLE INFO

The review of this paper was arranged by "Francisco Gamiz "

Keywords:
BTI
HCD
HSPICE
Activity awareness
Level Shifter
DVFS
Ring Oscillator

ABSTRACT

Circuit Aging Reliability Analysis Tool (CARAT), a framework that calculates random activity (frequency and duty) aware degradation of FETs to simulate circuit aging under real operating workloads is proposed. Bias Temperature Instability (BTI) and Hot Carrier Degradation (HCD) induced degradation of FETs is calculated in a cycle-by-cycle manner based on actual terminal waveforms grabbed from SPICE. Framework capability is demonstrated by using Level Shifter (LS) under random data-path activity, and Ring Oscillator (RO) under Dynamic Voltage Frequency Scaling (DVFS) conditions. The risk associated with the standard blanket approach is discussed.

1. Introduction

NBTI and HCD remain as key reliability concerns in FETs [1,2], thereby affecting various circuits [3]. Circuit aging can be estimated by assigning a blanket number to all FETs (DC, or AC with some pre-defined duty). Alternatively, activity awareness can be found using an Age-based approach [4], which relies on finding an effective duty and suitable compact models [17,18] for FET degradation. Finding effective duty can be challenging under realistic data-path workloads, more so under DVFS [14,15], while compact modeling is a challenge for BTI due to recovery, which is complex in nature. The presence of Self Heating (SH) further complicates the effective duty approach [5], since it depends on the actual number of on/off transitions.

CARAT uses cycle-by-cycle simulation to determine BTI and HCD in FETs. BTI is calculated by a physics-based BTI Analysis Tool (BAT) [6]. The model has a double interface Reaction-Diffusion (RD) model along with the Transient trap occupancy Model (TTOM) to calculate the degradation. This model helps to find out the time kinetics for the generation and passivation of interface traps (V_{IT}) due to and after the application of stress (Vg and T) [6,19]. Hot-carrier Empirical Analysis Tool (HEAT), a compact model including the time transformation concept is used for HCD (since it has no recovery) [7,20]. The model consists of an empirical equation, capable of handling cycle-by-cycle analysis for complex wave profiles. In our earlier work, CARAT is used to analyze large SRAM array under actual workloads [8]. In this work, the working of CARAT is described, with examples to demonstrate the need for cycle-by-cycle analysis.

2. Carat framework

CARAT presently is a standalone tool that invokes SPICE, Fig. 1. It requires circuit Netlist and Model Cards for FETs. For this work, we used HSPICE [9] and BSIM-CMG model [10] for FinFETs (calibrated with device data [4]).

It has a fully automated Control Framework that runs HSPICE, grabs terminal waveforms and temperature (T) due to SH for each FET (Grabber), shapes waveforms (Pulse Shaper) suitable for BTI and HCD analysis, Fig. 2 (a), run BAT and HEAT for short time (*e.g.*, 1 μs), extrapolate (Extrapolator) short-time individual FET degradation to End-of-Life (EOL), update (MC Updater) Model Cards of each FET, runs

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https://doi.org/10.1016/j.sse.2022.108586

Available online 3 January 2023
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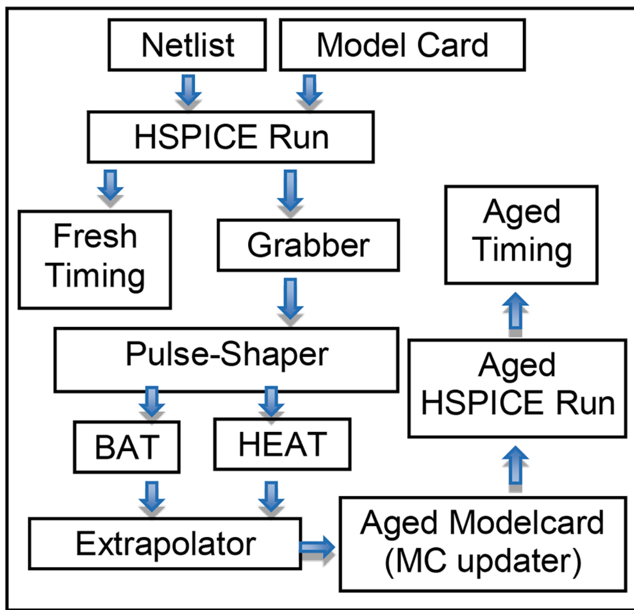


Fig. 1. Schematic illustration of CARAT simulation flow (Control Framework).

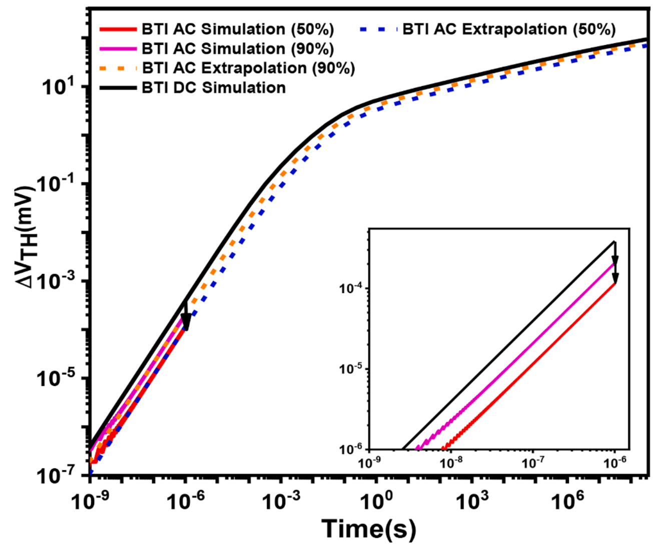


Fig. 3. BTI extrapolation for 50 % and 90 % duty input waveform, with AC simulation till 1 μs and extrapolation to 10 years. (Inset: BTI Extrapolation step from DC to AC at 1 μs plotted).

HSPICE, and compare initial and final runs. It handles process variability, BTI and HCD variability, by having individual BSIM, BAT, and HEAT ModelCards for each FET.

The extrapolation can be done at one go or in several loops (with intermediate CARAT runs) to EOL. Only V_T-shifted aging is used at present (V_T: threshold voltage), although other model parameters can also be aged in the MC Updater module (by using a suitable correlation between different parameters [4]).

Grabbed cycle-by-cycle waveform is shaped as trapezoidal on /off phases for BAT, and staircase transition phases for HEAT, Fig. 2, a low-frequency inverter simulation is used in this case for demonstration. Parameters for BAT and HEAT are obtained by calibration against device data [6,7]). BTI is calculated for PFET only (it is negligible for NFET [11]), and HCD for both FETs. BTI shows recovery but HCD does not. High-frequency inverter simulation for short time is shown, with resulting BTI at different duties, Fig. 3, and HCD at a different frequency, Fig. 4. BTI increases at higher duty but is frequency independent [1], HCD increases with a larger number of on/off transitions due to higher frequency.

Extrapolation is done by using isobias DC simulation reference, after shifting it vertically (Y-axis) over BTI and laterally (X-axis) over HCD short-time AC kinetics. A simple time-power law is not accurate for projection to EOL (as is usually done [12]), since the actual kinetics is substantially different. After extrapolation FET ModelCards are updated,

HSPICE is run again, and pre-and post-aging runs are compared Fig. 5. In this case, the rising edge is more degraded than the falling edge, since PFET has both BTI and HCD and NFET has only HCD. Standard inverter-based RO simulations show similar BTI across different stages (BTI is frequency independent), but higher HCD for the lower number of stages (higher frequency and number of transitions),

Fig. 6, consistent with measurements [13]. It should be noted that BAT and HEAT models can also handle temperature (T) variation over

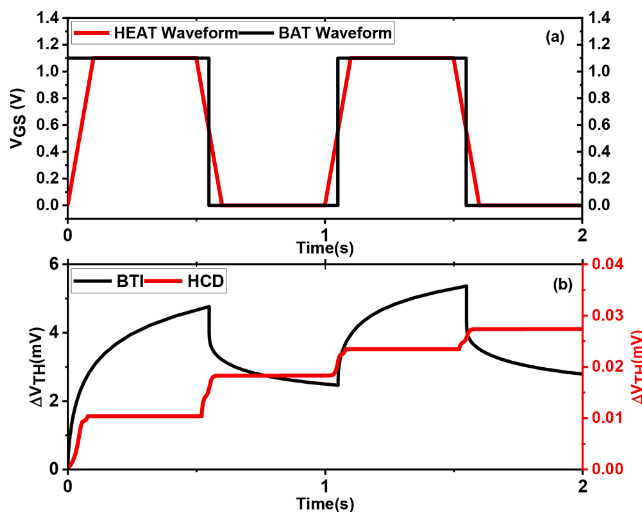


Fig. 2. (a) BTI and HCD pulseshaped waveforms (hspice extracted coincides with HCD) (b) CARAT simulated $\Delta V_{T\text{-}BTI}$ and $\Delta V_{T\text{-}HCD}$ time kinetics for two cycles.

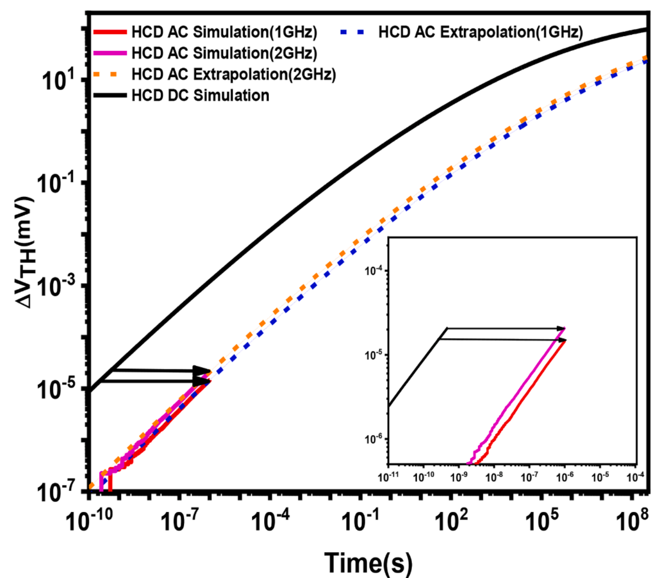


Fig. 4. HCI extrapolation for 1 GHz and 2 GHz frequency input waveform, with AC simulation till 1 μs and extrapolation to 10 years. (Inset: HCD Extrapolation step from DC to AC at 1 μs plotted).

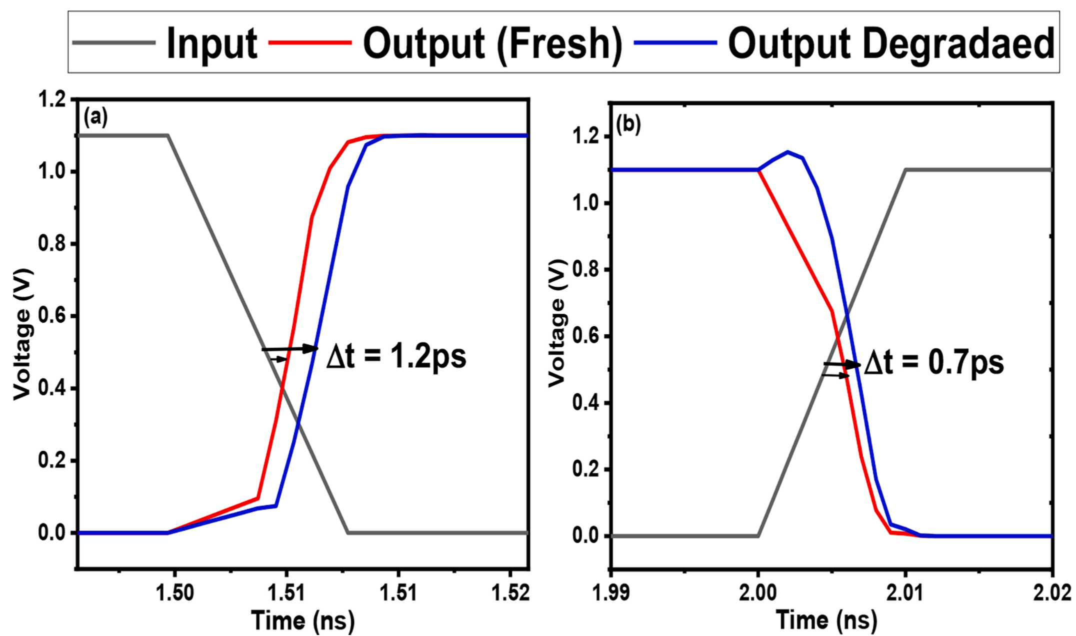


Fig. 5. Input and output waveforms without and with aging, showing delay in (a) rise time and (b) fall time for an Inverter.

Ring Oscillator stage	Frequency (GHz)	BTI Degradation at 1μs (mV)	HCD Degradation at 1μs (mV)	BTI Degradation at EOL (mV)	HCD Degradation at EOL(mV)	Δf (GHz)
7	16.756	1.13E-4	1.19E-4	69.35	52.9	2.375 (14.17%)
11	10.66	1.16E-4	1.03E-4	69.8	50.4	1.472 (13.8%)
21	5.58	1.15E-4	8.39E-5	69.64	46.98	0.74 (13.3%)
31	3.7823	1.14E-4	7.4E-5	69.6	44.98	0.4872 (12.88%)
51	2.3	1.14E-4	6.29E-5	69.5	42.98	0.2878 (12.5%)
101	1.16	1.14E-4	5.04E-5	69.5	39.1	0.14 (12%)

Fig. 6. BTI and HCD degradation for different Ring Oscillator stages at 1 μs and EOL (10Y).

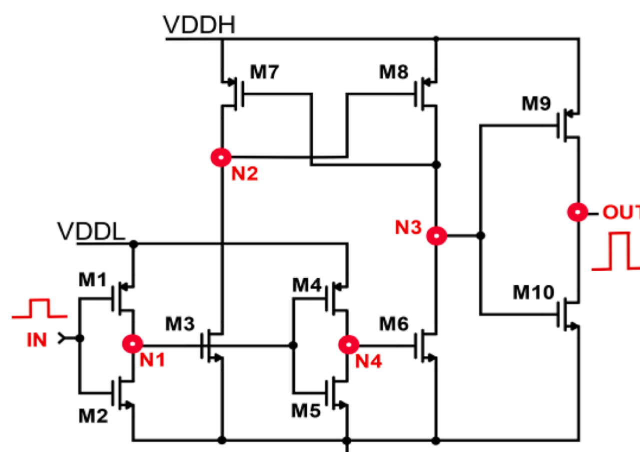


Fig. 7. Schematic of Level Shifter Circuit used to demonstrate activity aware degradation of transistors with CARAT.

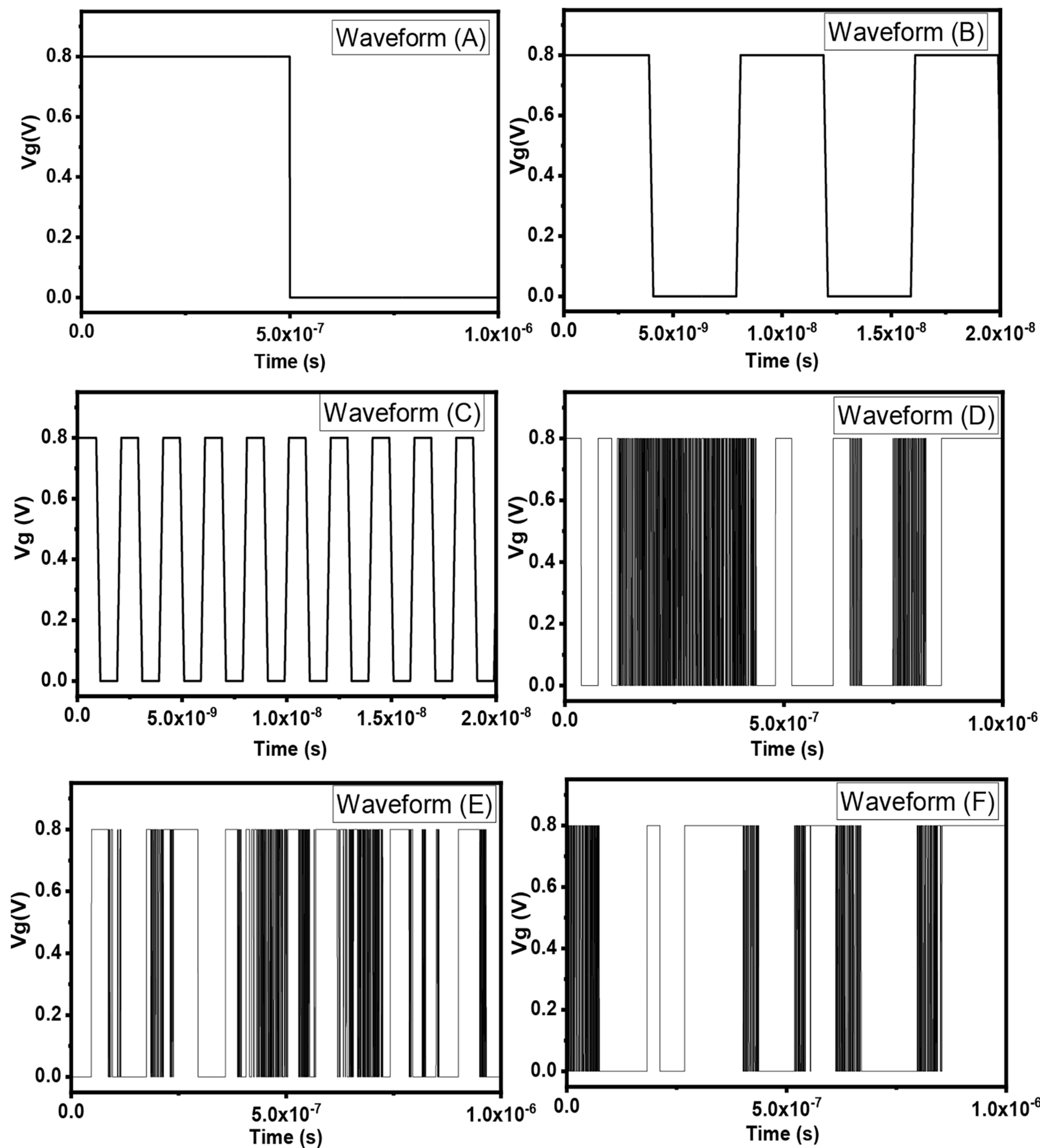


Fig. 8. Input waveforms used to demonstrate activity aware degradation of transistors with CARAT. (Waveform (B) and (C) although only shown upto 20 ns in the figure are repetitive and applied for 1 μs.).

time. So, HSPICE can measure T rise because of SHE [16]; hence the impact on ΔV_T can also be captured. Although, the effect of SHE has not been shown in this paper.

3. Activity awareness

An LS circuit, Fig. 7, is used. Table 1 lists short-time BTI and HCD degradation of all FETs, under different data-path like random activities as shown in, Fig. 8. All cases have effective 50 % duty for 1 μs simulation time: (A) is simple stress and recovery, (B) and (C) are AC with different frequencies but the same duty (only a fraction of the entire pulse duration is plotted), (D) through (F) have mixed frequency-duty combinations.

Whereas, Table 2 indicates the extrapolated degradation till EOL (10 Years) for the above-mentioned cases. Due to the difference in bias rail (V_{DD}), in general, FETs M1-M5 degrade lower than M6-M10. However, for any particular waveform, the BTI and HCD of different FETs can be similar or different, hence the assignment of a single value (based on V_{DD}) is ineffective. In spite of the same effective duty, for Case-A, BTI is highest (longest on/off phases) but HCD is lowest (lowest number of transitions), while Case-C HCD is highest (maximum number of transitions). All other waveforms are in between these two, and BTI and HCD are respectively determined by sequence and duration of subsequent on/off phases and the number of transitions. This makes the effective duty approach ineffective.

4. Dynamic Voltage and frequency Scaling or DVFS

RO (7-stage) is subjected to different DVFS-like V_{DD} waveforms, Fig. 9, and resulting BTI and HCD degradation are obtained and compared to standard analysis using minimum, average, and maximum V_{DD} (of DVFS waveform) for the entire duration.

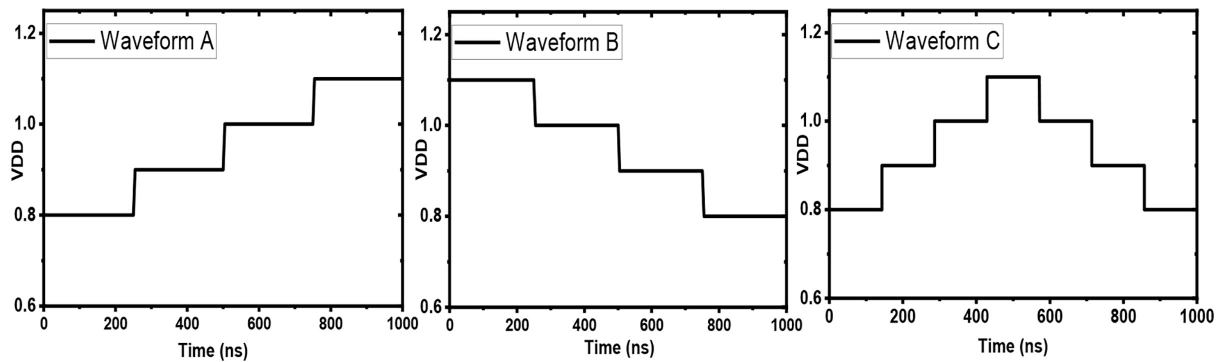
The actual case degrades differently from standard analysis and cannot be reproduced by taking the mean (of maximum and minimum) V_{DD} simulations or from average V_{DD} simulations. It is challenging to reproduce a DVFS-like scenario with an effective V_{DD} approach. Here blanket V_{DD} (maximum) analysis overestimates meaning having to design a circuit with very conservative timing constraints whereas for V_{DD} (average, minimum) the degradation is underestimated compared to activity aware analysis.

Table 1
Degradation of transistors obtained for input waveforms shown in Fig.8 indicating activity aware degradation of transistors in Level Shifter. All simulations done till 1μs with ΔV_{TH} values corresponding to BTI (Top) and HCD(Bottom) in millivolts.

Trx.	BTI (A) (mV)	BTI (B) (mV)	BTI (C) (mV)	BTI (D) (mV)	BTI (E) (mV)	BTI (F) (mV)
M1	5E-6	2.9E-6	2.9E-6	3E-6	3E-6	2.9E-6
M2	0	0	0	0	0	0
M3	0	0	0	0	0	0
M4	4.9E-6	2.9E-6	2.9E-6	3.5E-6	2.9E-6	3.5E-6
M5	0	0	0	0	0	0
M6	0	0	0	0	0	0
M7	1.82E-4	1.20E-4	1.22E-4	1.40E-4	1.16E-4	1.41E-4
M8	1.90E-4	1.16E-4	1.15E-4	1.20E-4	1.22E-4	1.15E-4
M9	1.82E-4	1.20E-4	1.22E-4	1.41E-4	1.16E-4	1.41E-4
M10	0	0	0	0	0	0
Trx.	**HCD (A) (mV)**	**HCD (B) (mV)**	**HCD (C) (mV)**	**HCD (D) (mV)**	**HCD (E) (mV)**	**HCD (F) (mV)**
M1	1E-6	2.6E-6	4E-6	2.7E-6	2.7E-6	2.4E-6
M2	1.6E-6	2.3E-6	3.1E-6	2.2E-6	2.2E-6	2E-6
M3	2.9E-6	12E-6	18.7E-6	12.4E-6	12.3E-6	11E-6
M4	1.4E-6	2.6E-6	4.1E-6	2.7E-6	2.7E-6	2.4E-6
M5	1.2E-6	2.5E-6	3.8E-6	2.6E-6	2.6E-6	2.3E-6
M6	3.8E-6	13E-6	20E-6	13.5E-6	13.4E-6	11.7E-6
M7	8.6E-6	38E-6	62E-6	41E-6	41E-6	36E-6
M8	9.4E-6	38E-6	59E-6	39E-6	39E-6	34.2E-6
M9	2.9E-6	9E-6	14.4E-6	9.5E-6	9.5E-6	8.3E-6
M10	2.3E-6	8.3E-6	12E-6	8E-6	8E-6	7.1E-6

Table 2
Degradation of transistors obtained for input waveforms shown in Fig.8 indicating activity aware degradation of transistors in Level Shifter. All simulations done till EOL (10Y) with ΔV_{TH} values corresponding to BTI (Top) and HCD(Bottom) in millivolts.

Trx.	BTI (A) (mV)	BTI (B) (mV)	BTI (C) (mV)	BTI (D) (mV)	BTI (E) (mV)	BTI (F) (mV)
M1	28.3	24	24.1	24.4	24.4	24.1
M2	0	0	0	0	0	0
M3	0	0	0	0	0	0
M4	28	24.2	24.2	25.4	24.1	25.4
M5	0	0	0	0	0	0
M6	0	0	0	0	0	0
M7	78	70.5	70.7	73.2	69.8	73.2
M8	79	70	69.7	70.4	70.7	69.7
M9	78	70.5	70.7	73.2	69.8	73.2
M10	0	0	0	0	0	0
Trx.	**HCD (A) (mV)**	**HCD (B) (mV)**	**HCD (C) (mV)**	**HCD (D) (mV)**	**HCD (E) (mV)**	**HCD (F) (mV)**
M1	7	10.9	13.3	11.1	11.1	10.5
M2	8.5	10.2	11.9	10.1	10.1	9.6
M3	11.3	21.3	25.6	21.7	21.6	20.5
M4	8.15	11	13.4	11.1	11.2	10.5
M5	7.4	10.7	13	10.8	10.8	10.3
M6	13	22.1	26.5	22.4	22.4	21.2
M7	19	35.83	43.4	37.1	36.9	35.2
M8	19.7	35.9	42.6	36.5	36.4	34.6
M9	10.7	19.5	23.8	19.7	19.8	18.6
M10	9.8	18.5	22.1	18.2	18.2	17.1



Waveforms	Degradation	CARAT (mV)	Minimum VDD (mV)	Average VDD (mV)	Maximum VDD (mV)
Waveform A	BTI	4.02E-5	2.9E-6	1.9E-5	1.1E-4
	HCD	9.2E-5	2.3E-5	5.2E-5	1.2E-4
Waveform B	BTI	3.81E-5	2.9E-6	1.9E-5	1.1E-4
	HCD	6.4E-5	2.3E-5	5.2E-5	1.2E-4
Waveform C	BTI	2.82E-5	2.9E-6	1.4E-5	1.1E-4
	HCD	7.3E-5	2.3E-5	4.6E-5	1.2E-4

Fig. 9. Schematic of DVFS waveforms (top) and resultant degradation in (mV) of each FET in 7-stage RO with CARAT, min, max and average analysis.

5. Conclusion

Realistic data-path like input waveforms and DVFS pose severe challenges for circuit simulation. Such situations are not representable by equivalent duty and V_{DD} simulations, and therefore, cycle-by-cycle simulations are required. The proposed CARAT framework achieves the same by removing pessimism for blanket DC analysis and removing uncertainty for AC analysis depending on duty and frequency. Due to the lack of recovery, a suitable compact model can handle HCD under arbitrary time/V_{DD} segments. Compact model development is very challenging for BTI due to the presence of recovery, which can become very complex under arbitrary time/V_{DD} segments. Hence, a physical framework, BAT, is used. The entire CARAT framework is fully automated and implemented in a parallel mode, significantly reducing run time. At present it is a standalone tool, integrating it inside SPICE would reduce the file size limitations (for grabbed waveforms) and further improve the runtime.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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