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Acceleration of semiconductor device simulation using compact charge model☆,☆☆

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ABSTRACT

In this work, we propose a method to get an initial guess for the semiconductor device simulation with a compact charge model. By using the obtained initial guess, we can perform the device simulation directly at the target bias condition without a time-consuming bias ramping process. In order to verify our method, rectangular Gate-All-Around (GAA) metal–oxide–semiconductor field-effect transistors (MOSFETs) having a long channel length are considered. Results clearly show that the device simulation can be accelerated through our method.

1. Introduction

In the semiconductor device simulation, the target bias condition has to be reached through the bias ramping process, which is typically time consuming. Furthermore, in order to obtain a solution of coupled nonlinear equations, the Newton–Raphson method is typically used and the converged solution is obtained through several Newton iterations. Since Newton iterations appear repeatedly during the bias ramping process, the overall computational time is significantly increased. Therefore, when a good initial guess for the target bias condition is available, the computational time can be significantly reduced.

Recently, in the semiconductor device simulation, many studies using a neural network model have been reported in order to describe the input–output relation or accelerate the simulation [1–6]. We have proposed a method to generate the initial guess through a trained deep neural network [7–10]. The proposed method in [7–10] generates the initial electrostatic potential depending on the device parameters. The efficiency of the proposed method has been demonstrated with several numerical examples.

In this study, instead of a deep neural network which must be trained before the inference, we use a compact charge model to predict an initial guess. The compact charge model for a two-dimensional (2D) metal–oxide–semiconductor (MOS) structure is numerically solved with the one-dimensional (1D) continuity equation. The solution of two coupled equations is used to generate the initial electrostatic potential and the initial electron density, which become the initial solutions of the drift-diffusion model. In order to verify our proposed method, rectangular gate-all-around (GAA) metal–oxide–semiconductor field-effect transistors (MOSFETs) with a long channel length shown in Fig. 1 are simulated.

2. Results for 2D rectangular MOS structures

In our previous study [11], we have proposed a compact charge model for a 2D MOS structure with an arbitrary cross-section. In this work, we use the model in [11] to predict an initial guess. It is expressed as [11]:

$$V_G - \Phi_{MS} + \frac{Q_d}{P\langle C_{ins}\rangle_s} + \frac{Q_e}{P\langle C_{ins}\rangle_s} \approx \langle\phi\rangle_s\,, \tag{1}$$

$$\langle\phi\rangle_s \approx V + V_T \log\left(\frac{\frac{1}{2}Q_e^2 + (1-\alpha_e)\,Q_eQ_d}{q\epsilon P^2 V_T n_{int}\left(1-\beta\exp\left(\frac{A^*}{P^2}\frac{2\alpha_eQ_e+Q_d}{2\epsilon V_T}\right)\right)}\right), \tag{2}$$

where V_G is the gate voltage, Φ_{MS} is the work function difference between the gate metal and intrinsic reference semiconductor, Q_e is the integrated electron charge, Q_d is the integrated doping charge, A^* is the area of the cross-section of the semiconductor region, P is the perimeter of the A^* surface, ϵ is the permittivity of the semiconductor, V_T is the thermal voltage, V is the electron quasi-Fermi potential, α_e is a normalized distance between the electron centroid and the interface, and β is a correction factor to consider an effect of a cross-section. Here,

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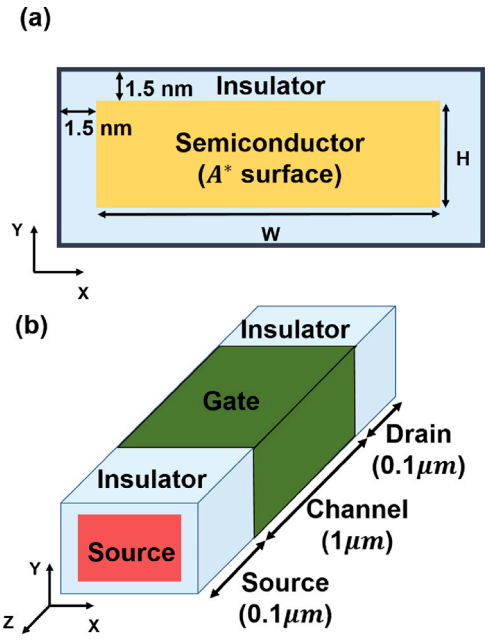

Fig. 1. (a) Cross-section of a rectangular GAA MOSFET and (b) its three-dimensional (3D) structure. The aspect ratio used in this work means a ratio of H to W. Thickness of the insulator is 1.5 nm. The channel length is 1 μm and the source/drain region is 0.1 μm-long. The p-type doping concentration of the channel region is 10^{16} cm^{-3} and the source/drain n-type doping is 10^{20} cm^{-3} in this work.

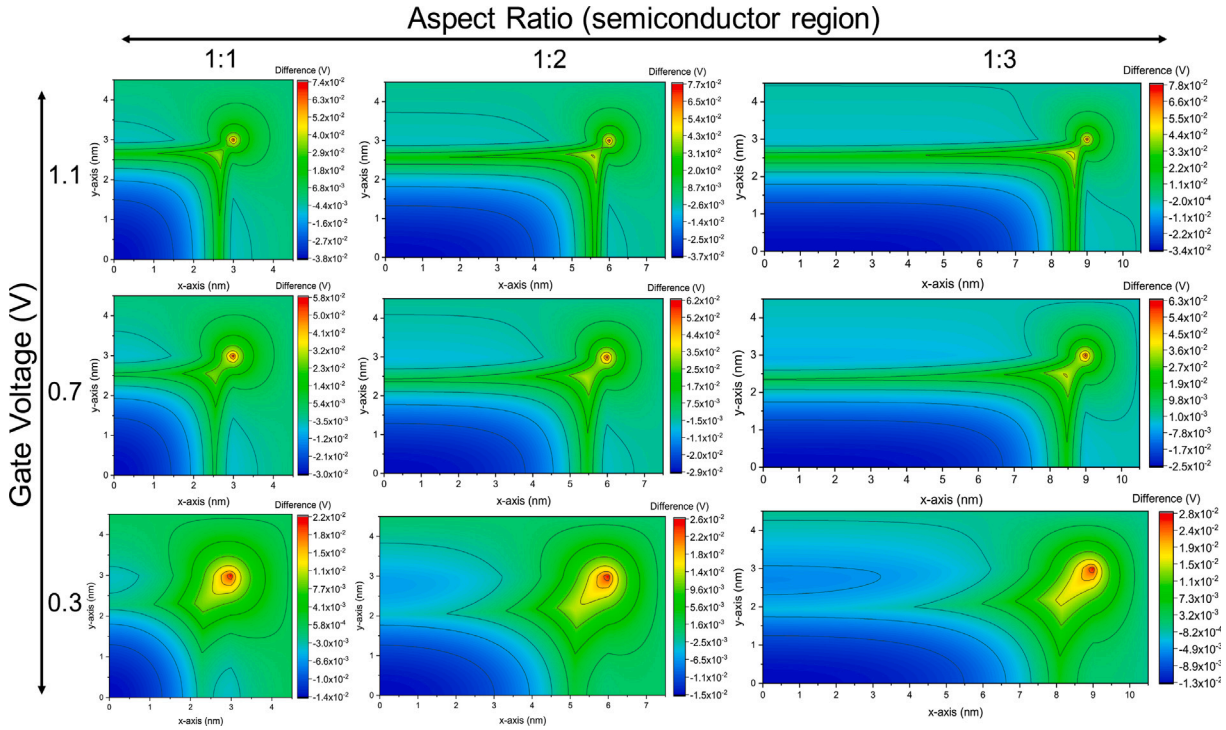

Fig. 2. Difference between the initial guess and the converged solution. Three aspect ratios (H:W = 1:1, 1:2, and 1:3) and three gate voltages (V_G = 0.3, 0.7, and 1.1 V) are considered. Only a quarter of the cross-section is shown. In these examples, the maximum difference is about 77 mV.

$\langle\phi\rangle_s$ and $\langle C_{ins}\rangle_s$ represent the average of the surface potential and the effective insulator capacitance per unit area, respectively. Furthermore, in [11], a generalized coordinate, ψ, is introduced, and it will be used for predicting the initial guess.

Before applying our method to the 3D MOSFETs, the compact charge model is tested in the 2D cross-sections. A procedure to predict the initial electrostatic potential for 2D rectangular GAA MOS structures is as follows. First, for a given cross-section, the linear Poisson equation is numerically solved considering only the doping charge density at a low V_G. From the numerical solution, ψ is calculated and parameters for calculating the compact charge model are extracted. The details of this procedure are described in [11]. Also, the Laplace equation is numerically solved in only the insulator region. The result of the Laplace equation is used to predict the initial potential profile of the insulator region. Then, (1) and (2) are solved at the target gate voltage and Q_e, $\langle\phi\rangle_s$, and $\langle\phi\rangle_X$ can be obtained at the target gate bias. Here, $\langle\phi\rangle_X$ is an average of the electrostatic potential (ϕ) over the cross-section with $\nabla^2\psi$ as a weighting factor [11]. Next, by using $\langle\phi\rangle_s$

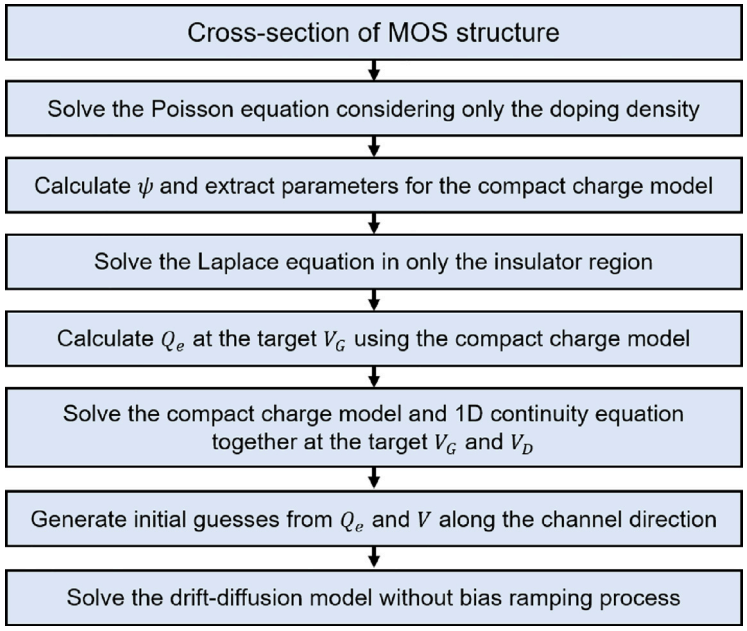

Fig. 3. Flow chart of the overall procedure proposed in this work.

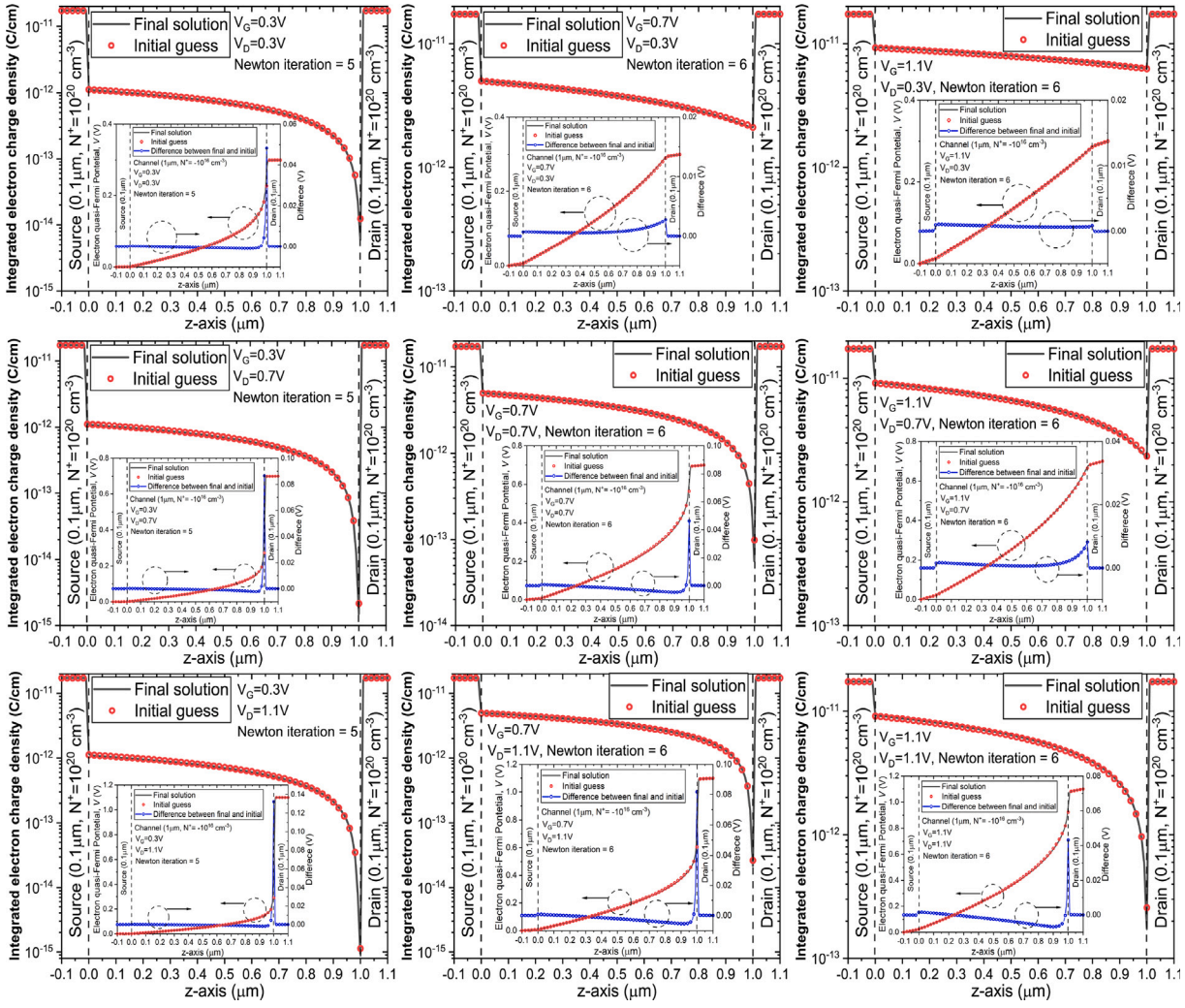

Fig. 4. Initial guesses of Q_e and V along the z-direction compared with final converged results at several bias conditions. The difference of V between initial guess and final result is also shown. Through the method proposed in this work, at most 6 Newton iterations are needed for solving the drift-diffusion model.

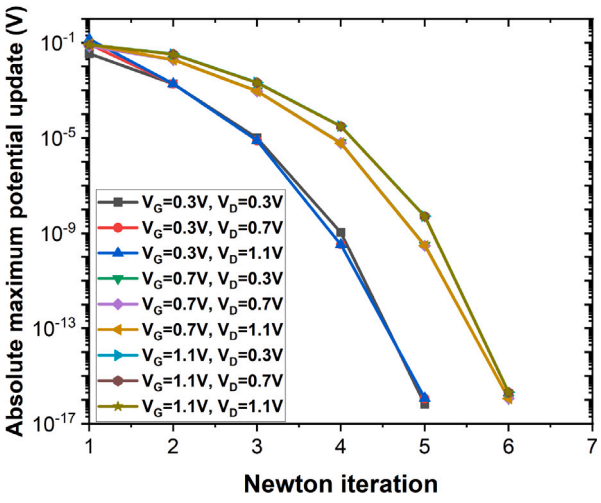

Fig. 5. Absolute maximum potential update versus Newton iteration during calculation of the drift-diffusion model with proposed initial guesses. Our method shows good convergence behavior without any bias ramping process.

and $\langle\phi\rangle_X$, we predict the initial potential, $\phi_{initial}$, for the semiconductor region at the target bias condition as follows:

$$\phi_{initial} = max\left(\left\langle\phi_n'\right\rangle_s(\psi - \Psi) + \langle\phi\rangle_s, \langle\phi\rangle_X\right), \tag{3}$$

where Ψ is the value of ψ at the semiconductor–insulator interface and $\left\langle\phi_n'\right\rangle_s = -\left(Q_e + Q_d\right)/\epsilon P$. Here, max is a function that returns the largest value in given arguments. Through this procedure, $\phi_{initial}$ can be obtained.

Fig. 2 shows differences between $\phi_{initial}$ and the final converged potential. Three different aspect ratios are considered. The maximum difference between the initial potential and the converged one is about 77 mV. By using $\phi_{initial}$, at most 7 Newton iterations are needed at the target bias condition without any bias ramping for solving the Poisson equation of MOS structures in Fig. 2.

3. Results for 3D rectangular GAA MOSFETs

The procedure for 2D MOS structures is extended to 3D MOSFETs. In order to obtain the initial guess for the drift-diffusion model, we solve the 1D electron continuity equation with (1) and (2). The 1D electron continuity equation is expressed as follows:

$$\frac{d}{dz}\left(\mu Q_e \frac{dV}{dz}\right) = 0, \tag{4}$$

where μ is the electron mobility and z is a coordinate along the channel direction. In this preliminary work, a constant mobility is assumed. Before solving the compact charge model and the 1D continuity equation together, ψ is calculated and parameters for calculating the compact charge model should be extracted as with 2D case. And then, (1) and (2) are solved in order to obtain Q_e at the target gate voltage. With these values, by solving (1), (2), and (4) together at the target bias point, we can get Q_e and V along the channel direction. In this work, Q_e of the source/drain n-type region is assumed to be solely determined by the doping concentration. By using the calculated Q_e and V, the initial potential profiles can be predicted from (3). Also, from the initial potential, the initial guess for the electron density can be obtained. These initial guesses are used to calculate the drift-diffusion model at the target voltage without the bias ramping process. The overall procedure predicting the initial guess is shown in Fig. 3.

In Fig. 4, results for rectangular GAA MOSFETs are shown. In this study, as shown in Fig. 1, the channel length is 1 μm and the channel p-type doping concentration is 10^{16} cm^{-3}. And the source/drain region is 0.1-μm-long and its n-type doping concentration is 10^{20} cm^{-3}. The aspect ratio of the cross-section used in Fig. 4 is 1:3 (H = 6 nm and W = 18 nm). Fig. 4 shows the initial Q_e and V along the z-direction compared with the final converged results at several bias conditions. Differences of V between initial guesses and final results are also shown and the number of Newton iterations needed for solving the drift-diffusion model at the target bias condition without any ramping process is found for each case. In these examples, at most 6 Newton iterations are needed to obtain the self-consistent solution. It is much more efficient than the conventional bias ramping method. Furthermore, the convergence behavior of results of Fig. 4 is shown in Fig. 5.

4. Conclusion

In conclusion, we have presented a method to predict an initial guess of the drift-diffusion model at a target bias condition. First, our method demonstrates that an initial potential profile for a 2D MOS structure at a target gate voltage can be generated through our previous compact charge model. For a 3D MOSFET, by using the compact charge model and the 1D electron continuity equation, the initial guess for the semiconductor device simulation is obtained appropriately. With the obtained initial guess, the device simulation is performed directly at the target bias point without any bias ramping. By adopting the proposed method, the number of Newton iterations to get the converged solution can be significantly reduced.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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