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A physics-based TCAD framework for NBTI

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ABSTRACT

A physics-based framework is incorporated in TCAD to model the primary mechanisms responsible for Negative Bias Temperature Instability (NBTI) in P channel High-K Metal Gate (HKMG) MOSFETs. Three underlying mechanisms are treated including interface trap generation-passivation via a Reaction-Diffusion (RD) model and its charge occupancy via an Activated Barrier Double Well Thermionic (ABDWT) model, hole trapping and de-trapping in pre-existing defects in the gate stack are modeled via an ABDWT model, and bulk trap generation-passivation is modeled via a Reaction-Diffusion-Drift (RDD) model. The framework is used to model measured NBTI time-kinetics for DC stress-recovery and various mixed DC-AC gate pulse segments for planar devices. Furthermore, the same framework is also used to test NBTI behavior in 3D FinFETs.

1. Introduction

The threshold voltage shift (ΔV_T) due to Negative Bias Temperature Instability (BTI) is an important issue in P channel HKMG MOSFETs [1]. The NBTI mechanism is controversial and various models are proposed [2–4]. The threshold voltage degradation (ΔV_T) is due to primary NBTI mechanisms, i.e., interface trap generation-passivation (giving rise to an interface trap charge density ΔN_{IT}) at or near the channel/interlayer (IL) interface and its charge occupancy (ΔV_{IT}), trap generation and passivation in the interlayer (giving rise to ΔV_{OT}), and charge trapping in pre-existing defects in the interlayer (giving rise to ΔV_{HT}) [5,7]. Previous NBTI modeling work in the 1D BTI Analysis Tool (BAT) is successfully applied to 2D/3D TCAD with the focus on trap generation and passivation (ΔN_{IT}) using an RD model [10,12] (using Synopsys tools [14,15]). In this work, we extend our NBTI framework in TCAD to improve the modeling of interface trap occupancy (ΔV_{IT}), charge trapping in the interlayer (ΔV_{HT}), and trap generation and passivation and its occupancy in the interlayer (ΔV_{OT}) (Fig. 1). The advantages of modeling NBTI in TCAD are capturing quantum effects, source/drain induced mechanical strain impact in the channel which are essential for scaled devices [10]. The framework (Fig. 1) is validated by modeling the measured data for pMOSFETs in 2D devices (Figs. 4–10). Furthermore, the framework is used to examine the reliability behavior briefly in 3D FinFETs (Fig. 10).

2. NBTI models

The inversion layer hole tunnels to Hydrogen (H) passivated defects at the channel/interlayer interface during NBTI stress, reacts with H passivated defects, breaks, generates interface states, and releases H (Fig. 2a). The released H diffuses and reacts with another H passivated defect inside the interlayer to form H_2, which diffuses away. This is

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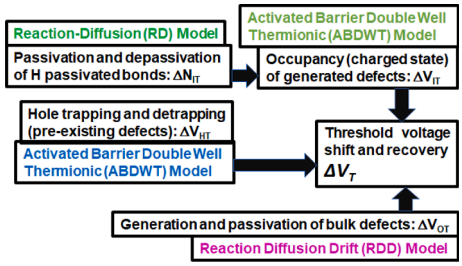

Fig. 1. Schematic of TCAD framework for NBTI during stress and recovery for High-K Metal-Gate devices. The ΔV_T model subcomponents and corresponding models are shown.

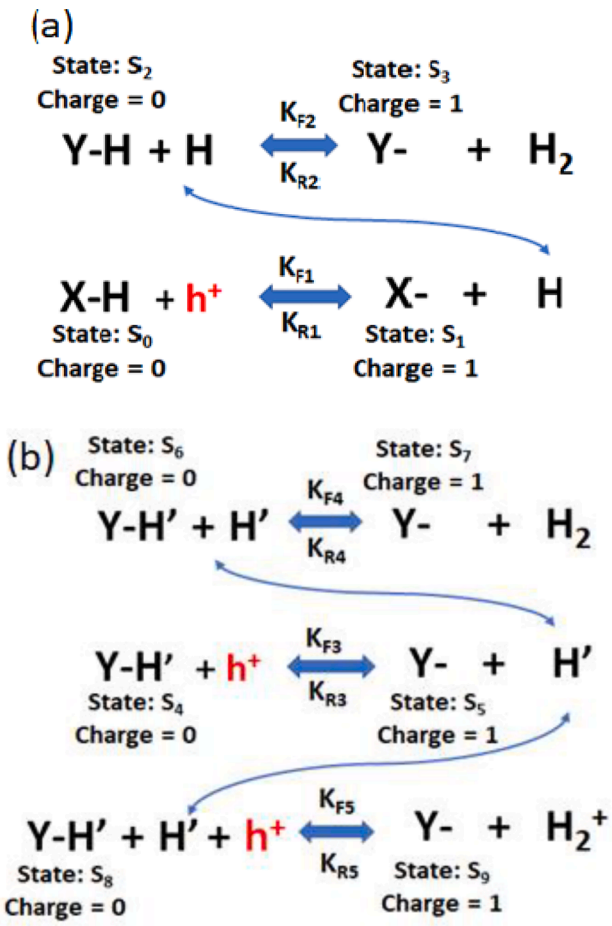

Fig. 2. Multi-State Configuration (MSC)-hydrogen transport degradation model [15], utilizing Capture Emission De-passivation model [15] for defect dissociation used in (a) the RD model for interface traps generation-passivation, and (b) the RDD model for bulk trap generation-passivation in TCAD. H': HydrogenSpeciesA, H_2^+: Hydrogen Ion, H: Hydrogen Atom, H_2: Hydrogen Molecule, h^+: hole.

called the Reaction-Diffusion (RD) model. An anode hole injection (AHI) -related process triggered by a hole generates the trap in the interlayer and releases H, which further diffuses, reacts with another H-passivated defect inside the interlayer, and generates defect states and H-species (H-molecule, H-ion). The generated H-molecule and H-ion diffuses towards the gate. This is called the Reaction-Diffusion-Drift (RDD) model for the traps generated in the interlayer [9] (Fig. 2b). The ABDWT model is used for charge trapping in pre-existing defects in the interlayer (Fig. 3).

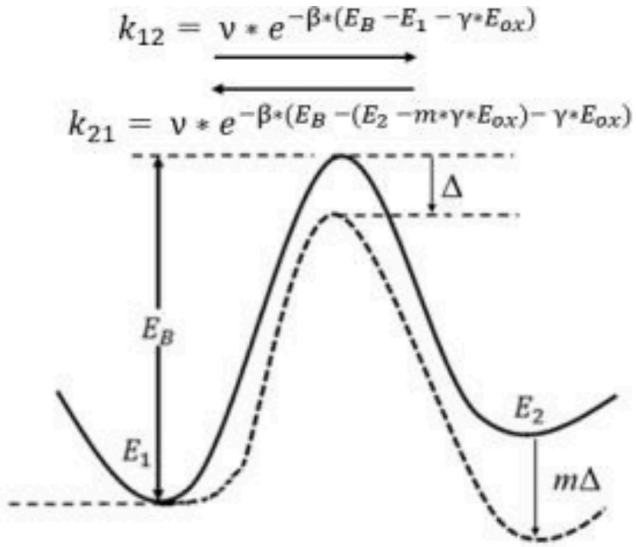

Fig. 3. Schematic of the ABDWT model in TCAD to capture hole trapping detrapping in pre-existing defects, showing thermally activated barrier E_B, with forward and backward transition rates [8].

3. TCAD framework

The device structure is generated in 2D (Fig. 4a) and 3D (Fig. 10a). In the device simulation [15], the defect dissociation by holes during BTI stress utilizes the Capture-Emission De-passivation (CED) model [15]. A multi-state configuration (MSC) is defined for H-passivated defects at channel/interlayer and interlayer/HfO2 interfaces. The MSC-hydrogen transport degradation model is accounted for the reaction between mobile hydrogen species and localized states (H-passivated defects)

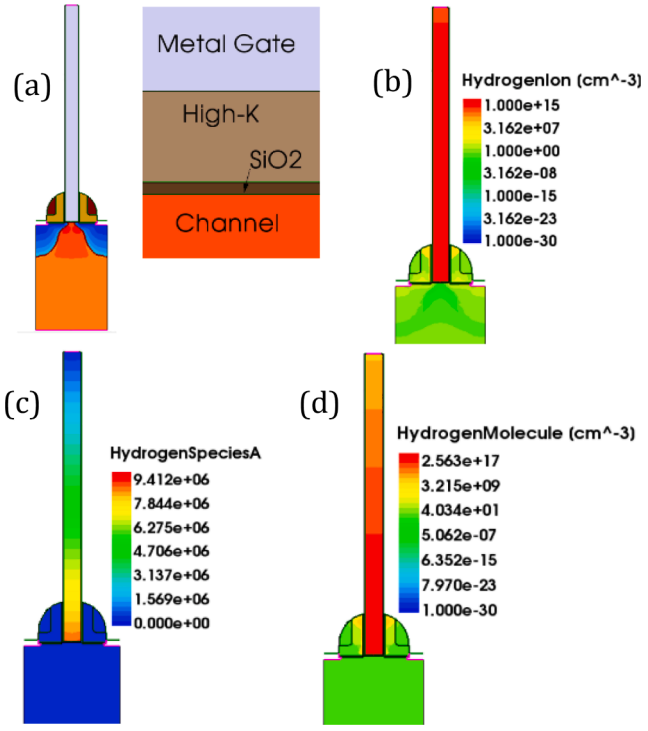

Fig. 4. Device showing gate stack for (a) 2D pMOSFET, and diffusion of different hydrogen species for (b) Hydrogen-Ion (c) Hydrogen SpeciesA (d) Hydrogen Molecule in 2D MOSFET used in RD model and RDD model after 1Ks stress time.

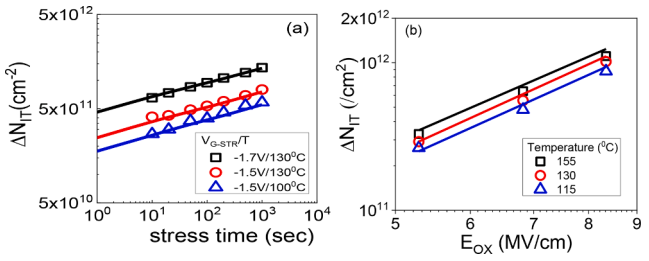

Fig. 5. TCAD modeling of DCIV measured (a) time kinetics of ΔN_{IT}, (b) field dependence of ΔN_{IT} at different temperatures after fixed stress time of 1Ks for the D1 device. Line: TCAD simulation, symbol: measured data.

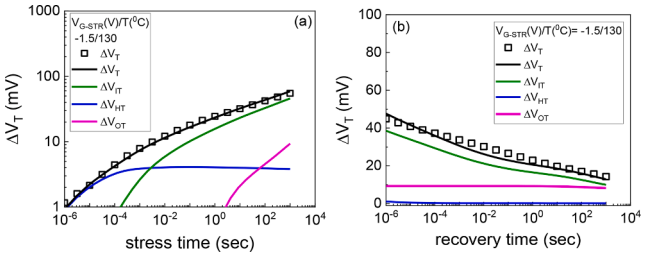

Fig. 6. TCAD modeling of UF-MSM measured ΔV_T of the D1 device during (a) stress, and (b) recovery time kinetics. ΔV_T subcomponents are also shown. Line: simulation, symbol: measured data.

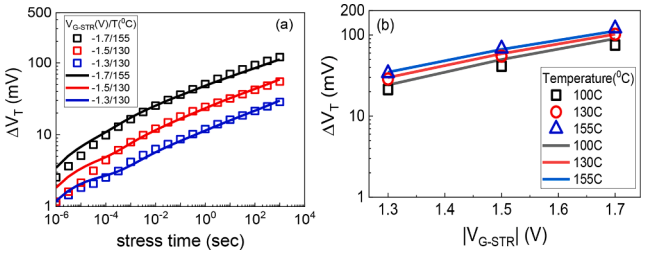

Fig. 7. TCAD modeling of UF-MSM measured ΔV_T of the D1 device during (a) stress time kinetics at mixed stress voltage/temperature ($V_{G\text{-}STR}$/T), (b) $V_{G\text{-}STR}$ dependence of fixed time ΔV_T at different T. Line: simulation, symbol: measured data.

together with the hydrogen transport [15]. The charge associated with each localized state is shown (Fig. 2a). This is the RD model for interface traps in TCAD (Fig. 2a). The key modeling parameters of the RD model are the forward reaction pre-factor at the channel/IL interface (*CPre-Factor*, time kinetics and magnitude of trap generation), field acceleration factor (γ, bias dependence of trap generation), and thermal activation (W_f, temperature dependence of trap generation) [15]. The RD model is combined with the ABDWT model for charge occupancy of generated traps (ΔV_{IT}), which previously has been done empirically via a Transient Trap Occupancy Model (TTOM) [10]. The RDD model utilizes a similar framework as the RD model (Fig. 2b). Newly incorporated Hydrogen species (HydrogenSpeciesA/B/C, HydrogenIon) are utilized to isolate the AHI-related process triggered by holes for bulk trap generation in the interlayer (Fig. 4b-d), which leads to the formation and diffusion of HydrogenSpeciesA, Hydrogen molecule (H_2), and Hydrogen Ion (H_2^+) (Fig. 2b). HydrogenSpeciesA/B/C are treated as hydrogen atoms. For charge trapping in interlayer bulk, the ABDWT model considers a trap with two states E_1 (uncharged) and E_2 (charged) connected through a thermally activated energy barrier E_B which is lowered by the applied bias (Fig. 3). The initial defect density in the interlayer bulk (for the magnitude of ΔV_{HT}) and the barrier energy E_B (for the time kinetics behavior of ΔV_{HT}) are the important modeling parameters for charge

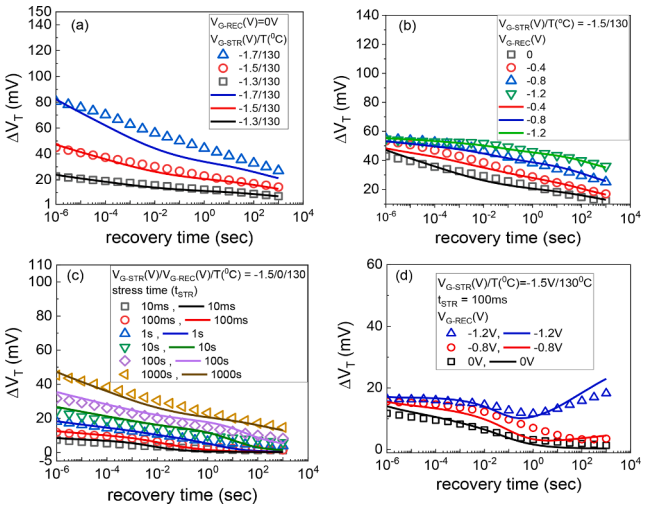

Fig. 8. TCAD modeling of UF-MSM measured ΔV_T of the D1 device showing (a) recovery at 0 V recovery bias, (b) recovery bias dependence, (c) stress-time dependence, and (d) recovery bias dependence after short stress time of 100 ms. Line: TCAD simulation, symbol: measured data.

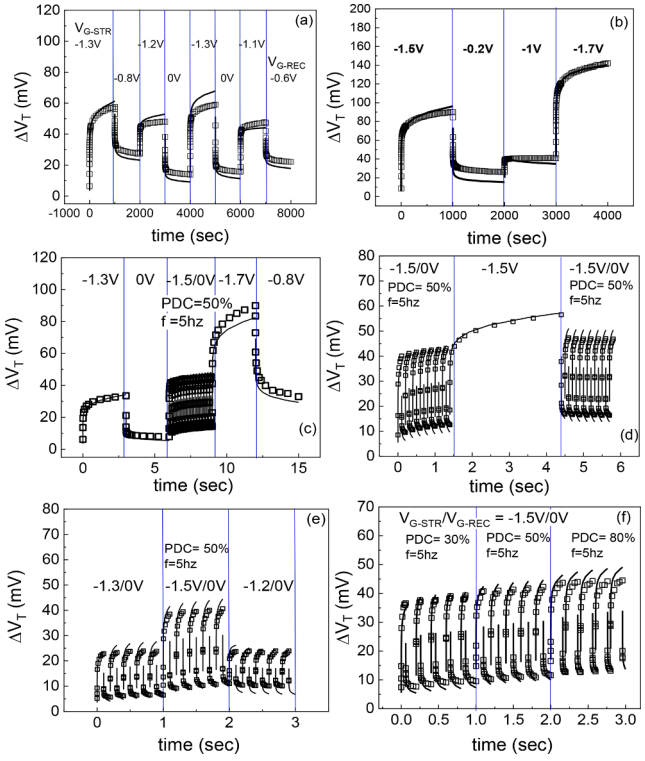

Fig. 9. TCAD modeling of measured ΔV_T of the D2 device (a) (b) DC segments with varying $V_{G\text{-}STR}/V_{G\text{-}REC}$, (c) (d) mixed DC-low frequency (f) AC, and (e) (f) low f AC cycle with variable PDC. Black Line: TCAD simulation, symbol: measured data.

trapping. In the real scenario, traps are located inside the interlayer where carriers can be captured and emitted additionally through tunneling processes. The ABDWT model is effective, connecting both the processes in an effective manner by fit factors and distributions for E_B and E_2 [15]. The backend of 1 μm is used to allow H_2 diffusion (Fig. 4a).

4. Device and measurement details

Gate First (GF) N/P HKMG MOSFETs having ultra-thin thermal IL

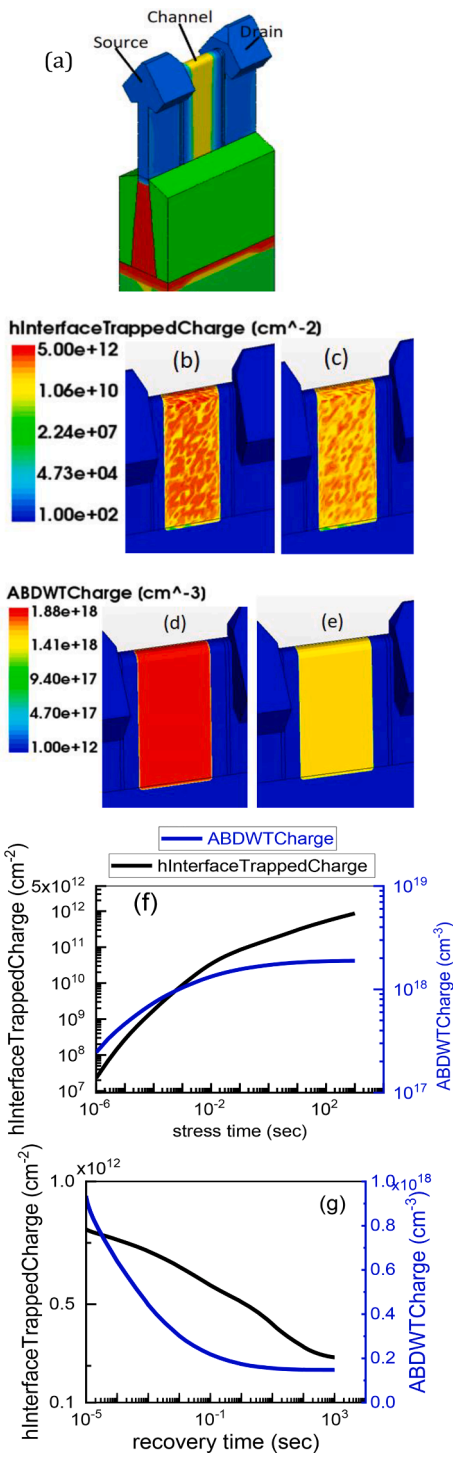

Fig. 10. 3D isometric view of FinFET showing (a) device structure, generated traps in the fin area using the RD and the RDD model at the end of (b) 1Ks stress, (c) 1Ks recovery, charge trapping in the fin area using ABDWT model at the end of (d) 1Ks stress, (e) 1Ks recovery. Corresponding time kinetics is shown during (f) stress, and (g) recovery.

and HfO_2 HK are used [1]. IL scaling is done using thermal process tweak for D1 (3 Å) with lower N%, and N based IL, D2 (1.5 Å), EOT of HK is 4.6 Å. DCIV data (Fig. 5) are with delay correction [11]. The ΔV_T (Figs. 7–10) is measured with a 10 μs delay [5,6].

5. TCAD modeling

The modeling of DCIV measured ΔN_{IT} kinetics at different gate bias (V_G) and temperatures (T) are shown for the D1 device using the RD model (Fig. 5). The calibrated RD model (time slope $n \sim 1/6$, field acceleration factor γ) from DCIV modeling of ΔN_{IT} is utilized in the overall ΔV_T framework for the interface trap generation sub-component of ΔV_T. The measured ΔV_T time kinetics is modeled with its subcomponents at fixed V_G/T during stress (Fig. 6a) and recovery (Fig. 6b). TCAD simulated trap densities and charge-trapping time-kinetics data are converted to ΔV_T model sub-components by multiplying with a capacitance factor (e.g., $\Delta V_{IT} = K^*\Delta N_{IT}$) for both devices [13].

The overall ΔV_T time kinetics modeling is shown for mixed V_G/T during stress (Fig. 7a) and bias dependence of fixed time ΔV_T at the end of 1Ks stress at different temperatures (Fig. 7b). The modeling of ΔV_T recovery at various measurement conditions, i.e., the recovery after different stress conditions ($V_{G\text{-}STR}$ and T) at recovery bias ($V_{G\text{-}REC}$) of 0 V (Fig. 8a), the $V_{G\text{-}REC}$ dependence after longer (1Ks).

stress time (Fig. 8b), the stress time-dependent recovery behavior (Fig. 8c), and the $V_{G\text{-}REC}$ dependence after shorter stress time of 100 ms (Fig. 8d) is also achieved. It is appreciable that TCAD can mimic the re-stressing during recovery after a short stress time (100 ms). The three model subcomponents (Fig. 1), i.e., $\Delta V_{IT,}$ ΔV_{HT} and ΔV_{OT} are used to model the D1 device measured data (Figs. 6–8). The model framework shows good agreement with experimental data.

for the D2 device (Fig. 9a–f) showing DC stress-recovery bias variation, DC-AC-DC, AC-DC-AC, and pure AC gate pulses having variable pulse duty cycle (PDC). The ΔV_T model subcomponents for the D2 device measured data are ΔV_{IT} and ΔV_{HT} (Fig. 9a-f). The framework is extended to 3D FinFETs (Fig. 10a). The simulated trap profile and charge trapping are shown (Fig. 10b-e). Time kinetics of the generated traps and trapped charges in the FinFET show similar behavior as in 2D TCAD simulations for planar devices, indicating the 3D capability of the framework (Fig. 10f-g).

6. Conclusion

A fully physical TCAD framework to model NBTI is validated with measured data of differently processed MOSFETs by incorporating the RD model with the ABDWT model (as TTOM), the RDD model, and the ABDWT model for the interface traps, bulk traps, and charge trapping, respectively. TCAD framework validation in 3D with measured data for a FinFET and GAA-FET is in progress.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The authors are unable or have chosen not to specify which data has been used.

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