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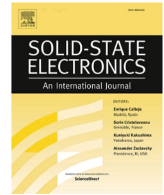

A dynamic current hysteresis model for IGZO-TFT

Yu Li [a], Xiaoqing Huang [a], Congwei Liao [a], Runsheng Wang [b], Shengdong Zhang [a], Lining Zhang [a,*], Ru Huang [b]

[a] *School of Electronic and Computer Engineering, Peking University, Shenzhen, China*
[b] *School of Integrated Circuits, Peking University, Beijing, China*

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ABSTRACT

This paper proposes a dynamic current hysteresis model for the Indium Gallium Zinc Oxide Thin Film Transistor (IGZO-TFT). Based on the Shockley-Read-Hall (SRH) theory, a kinetic equation that accurately describes the interface trap's capture/emission behaviour is presented, which can incorporate the effect of interface trap density, trap energy level and scan rate dependency. Further, the kinetic equation is solved using a sub-circuit approach, combined with a calibrated TFT static current model, to achieve an accurate simulation of the current hysteresis of IGZO-TFT. This model has been validated with numerical TCAD simulations and has been shown to precisely reflect the effect of trap energy level, trap density and scan rate on the current hysteresis characteristics.

1. Introduction

The progressive advancement of thin-film transistor technology, combined with rapid advances in materials and processes, has enabled the emergence of large-scale TFT circuits and integrated systems for applications ranging from biosensing to storage arrays, enhanced displays and matrix imaging. [1–3] However, a non-negligible number of interface traps are introduced during different device processing, including organic [4], polycrystalline silicon [5] and a-IGZO-TFT [6,7] and so on. The capture and emission events of the interface trap result in a degradation of the threshold voltage and carrier mobility, which leads to current hysteresis in the transfer characteristics of the transistor and subsequently has a significant impact on the performance of the TFT device at the circuit level. For example, this hysteresis can be used to alter the brightness of the current-driven device Organic Light-Emitting Diode [6]. Furthermore, if the hysteresis characteristics can be effectively controlled, combined with its low temperature process and simplified structure, TFT array could be a potential contender for 3D stacked NVMs [3].

There are few reported works on modelling dynamic current hysteresis for circuit simulation based on trap dynamics [8]. The design and performance evaluation of large-scale systems place high demands on a dynamic current hysteresis model that captures the effects of the physical properties of the interface trap and the scan rate of the gate voltage on the current characteristics of the TFT.

In this paper, a dynamic current hysteresis model based on trap dynamics is proposed and has been shown to accurately reflect the effect of trap energy level, trap density and scan rate on the current hysteresis characteristics.

2. Current hysteresis of IGZO-TFT

For acceptor-traps, "shallow" means that the energy level E_{tA} is close to the conduction band energy level E_C (i.e. $\Delta E_t = E_C - E_{tA}$ is relatively small), while E_{tA} is near the intrinsic Fermi level E_i for the deep traps. Fig. 1(a) is the 3D structure of the IGZO-TFT device used in this paper. The thickness of the a-IGZO layer is 0.04 um, with the density of conduction band states $N_c = 5.2 \times 10^{18} cm^{-3}$ and the density of valence band states $N_v = 5.0 \times 10^{20} cm^{-3}$ at the temperature of 300 K. The Heiman model and the trap-assisted tunneling are activated for the simulation of the interface traps. In numerical TCAD simulation, by introducing a certain amount of acceptor-traps ($\Delta E_t = 0.1 eV$, $N_{t,shallow} = 3 \times 10^{12} cm^{-2}$) at the IGZO/$SiO_2$ interface for a-IGZO-TFT device with W = 20um, L = 20um and $V_d = 1.1V$, the transfer characteristic curve shows a clockwise hysteresis current (as shown in Fig. 1(b)).

The physical origin of this clockwise hysteresis is that the electrons in the reservoir (i.e., gate and channel) are captured by the interface acceptor-traps during the forward scanning, resulting in the larger threshold voltage shift at the reverse scanning. The width of the current

* Corresponding author.
E-mail address: eelnzhang@pku.edu.cn (L. Zhang).

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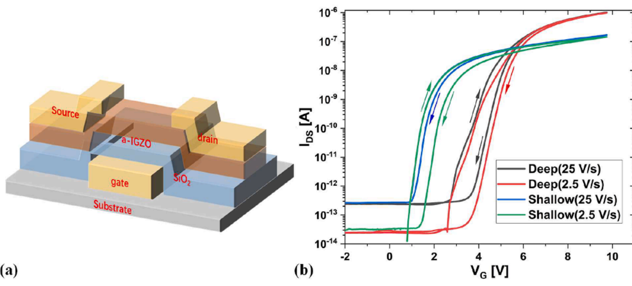

Fig. 1. (a) Schematic of IGZO-TFT 3D structure. (b) Dependence of hysteresis width on scan rate.

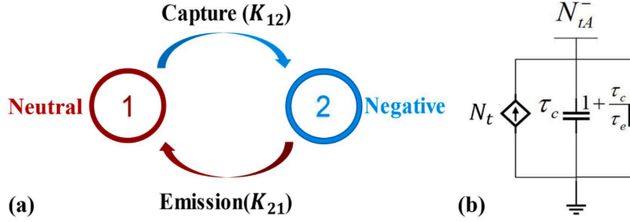

Fig. 2. (a) Capture and emission events of Acceptor-trap. (b) Equivalent sub-circuit of the trap kinetic equation.

hysteresis increases when the applied voltage scan rate is reduced, and the above phenomenon is consistent with that reported in [6].

3. Dynamic model description

SRH theory is often used to describe interface trap dynamics [9,10], this section discusses the implementation of trap theory in the trap dynamics simulation.

A. Trap Dynamics Based on SRH Theory

Fig. 2(a) illustrates the switching of trap state involving carriers in the channel, where the transition rate (probability per unit time) $K_{12/21}$ is related to the capture and emission coefficients[11]. The trap occupation probability $p_2(t)$ can be described in the form of Eq (1),

$$p_2(t+\Delta t) = K_{12}\bullet\Delta t\bullet p_1(t) + (1-K_{21}\bullet\Delta t)p_2(t) \tag{1}$$

Since $p_1(t) + p_2(t) = 1$, the corresponding differential form of (1) can be rearranged as Eq (2),

$$\frac{dp_2(t)}{dt} = K_{12}\bullet(1-p_2(t)) + K_{21}\bullet p_2(t). \tag{2}$$

According to the SRH theory, the transition rates are shown in Eq (3),

$$K_{12} = v_{th,n}\bullet\sigma_n\bullet n;\ \ K_{21} = v_{th,p}\bullet\sigma_p\bullet p \tag{3}$$

where $v_{th,n/p}$ denotes the carrier thermal velocity and $\sigma_{n/p}$ is the electron/hole capture cross-section.

B. *Sub-Circuit Approach*

To facilitate the use of the sub-circuit approach to calculate the number of occupied acceptor-traps N_{tA}^-, Eq (2) can be reformulated:

$$\frac{dN_{tA}^-(t)}{dt} = \frac{N_t - N_{tA}^-(t)}{\tau_c} - \frac{N_{tA}^-(t)}{\tau_e} \tag{4}$$

where N_t is the interface traps density with $N_{tA}^- = p_2(t)\bullet N_t$, and $\tau_{c/e}$ is the capture/emission time constant, expressed as Eqs. (5) and (6).

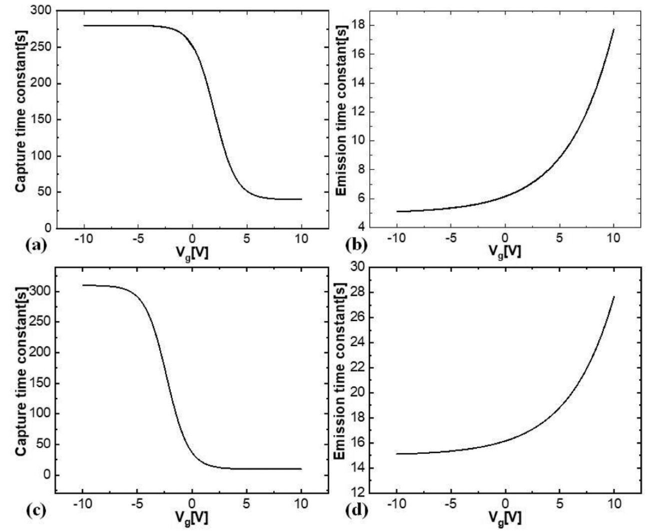

Fig. 3. Capture and Emission time constant curves of shallow and deep energy level traps.

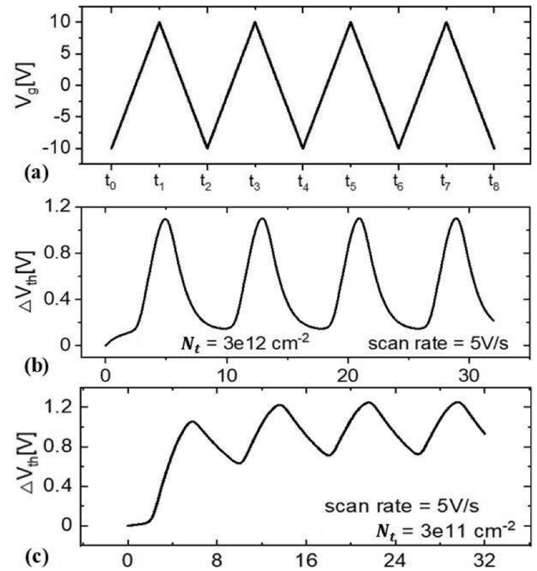

Fig. 4. (a) The scan voltage. Threshold voltage shift dynamic responding of (b) shallow traps with $N_{t,shallow} = 3\times 10^{12}cm^{-2}$. (c) deep traps with $N_{t,deep} = 3\times 10^{11}cm^{-2}$.

$$\tau_c = \frac{1}{K_{12}} = \tau_{c0}\bullet\exp\left(\frac{-V_g(t)}{n\bullet k\bullet T}\right) \tag{5}$$

$$\tau_e = \frac{1}{K_{21}} = \tau_{e0}\bullet\exp\left(\frac{V_g(t)}{n\bullet k\bullet T}\right) \tag{6}$$

The sub-circuit shown in Fig. 2(b) is built to solve the dynamic node voltage in SPICE simulator and the device threshold voltage is updated in the form of Eq. (7),

$$V_{th}(t) = V_{th0} + \Delta V_{th}(t) = V_{th0} + \frac{q\bullet N_{tA}^-(t)}{C_{ox}} \tag{7}$$

4. Simulations and results

Since the carrier capture cross-section is related to the trap energy level, the time constant is found to depend on the gate voltage V_g and the

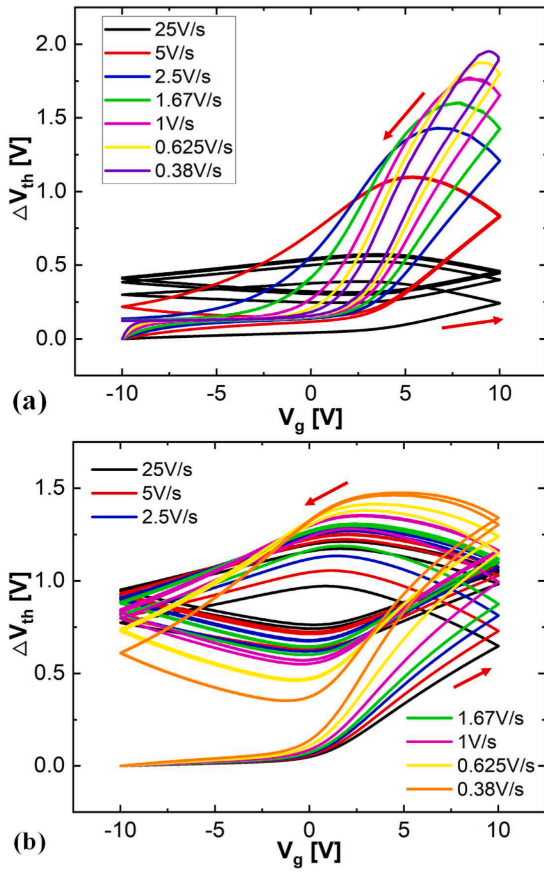

Fig. 5. ΔV_{th} versus Vg for different scan rates of (a) shallow energy level traps ($\Delta E_t = 0.1eV$), (b) deep energy level traps ($\Delta E_t = 0.6eV$).

defect energy level E_t with Eqs (3–5).

A. *Threshold Voltage Shift (ΔV_{th}) Simulation*

In order to improve convergence and fitting accuracy, the time constant expressions are rationalized as the Eqs. (8) and (9), while parameters are extracted for shallow and deep energy level traps respectively.

$$\tau_c = A_1 \bullet \tanh(B_1 \bullet V_G + C_1) + D_1 \tag{8}$$

$$\tau_e = A_2 \bullet \exp(B_2 \bullet V_G + C_2) + D_2 \tag{9}$$

Fig. 3 shows the dependence of the time constant on the gate voltage for the shallow ($\Delta E_t = 0.1\,eV$) and the deep ($\Delta E_t = 0.6\,eV$) traps. The capture probability becomes larger when the trap energy level is bent below the Fermi level, creating a step-down trend in the capture time constant curve.

During the simulation, the scan voltage is a triangular wave (Fig. 4 (a)), while the effect of trap energy level on the threshold voltage shift is shown in Fig. 4(b-c) with $N_t = 3 \times 10^{12} cm^{-2}$ and scan rate = 5 V/s, where the peak of the curve corresponds to the highest trap occupancy.

For shallow energy traps ($\Delta E_t = 0.1eV$), Fig. 5(a) reveals that as the scan rate decreases, the trap obtains sufficient time for capturing, resulting in the peak of the threshold voltage shift gradually increasing and shifting to the right. It is worth noting that Fig. 5(b) shows an overall upward shift in the threshold voltage shift curve for the deep traps, which is due to the earlier appearance of the step-down.

B. *IGZO-TFT Static Current Model.*

Current hysteresis can be modeled as a result of the dynamic response of the threshold voltage acting on a static current model. The credibility of the static current model is therefore a prerequisite for the accuracy of the dynamic hysteresis model, however, there is no standard model of static current for IGZO-TFT in the industry at present [12–14].

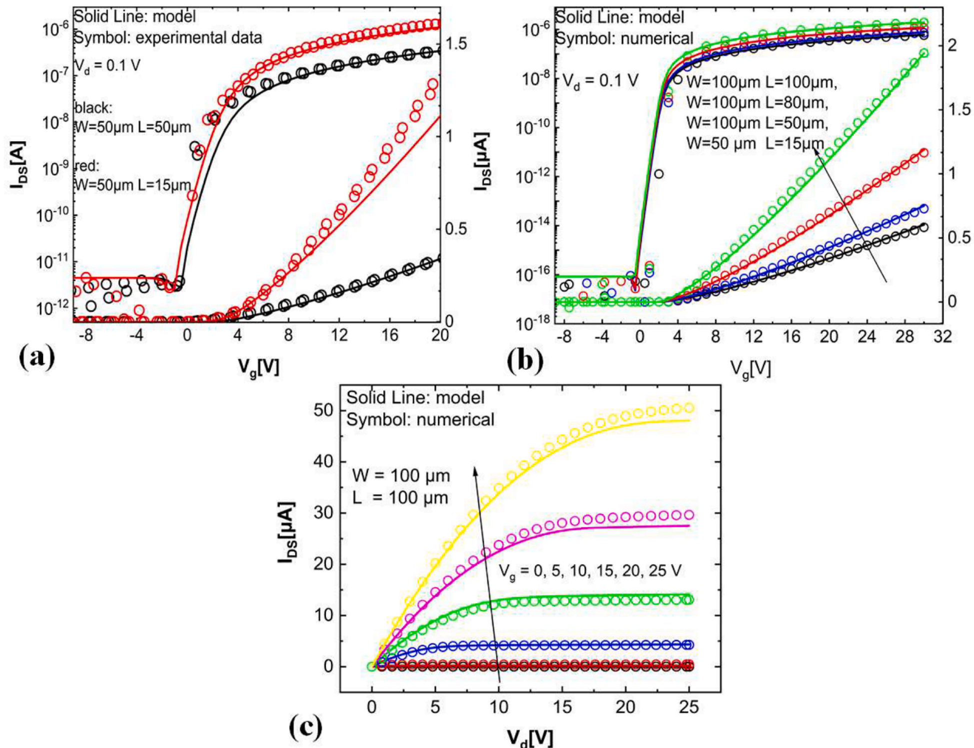

Fig. 6. Parameter extraction of the static current model with (a) experimental data, (b) Id-Vg curves and (c) Id-Vd curves.

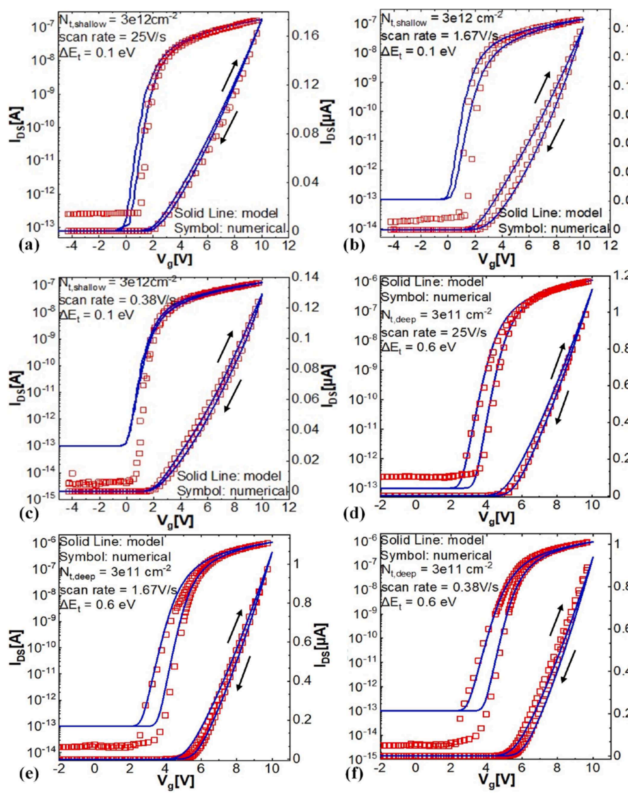

Fig. 7. Model validation of the hysteresis characteristics of Id-Vg curves for different scan rates for (a–c) shallow energy level traps ($\Delta E_t = 0.1eV$), (d-f) deep energy level traps ($\Delta E_t = 0.6eV$).

In consideration of compatibility with trap kinetic behaviors, the threshold voltage-based IGZO-TFT current model [15] is used in this paper. The parameters (mobility, threshold voltage, subthreshold slope and off-state current) of this model have been extracted using the experiment data and TCAD data. Fig. 6(a) shows the agreement of transfer characteristic between the model and experiments. Fig. 6(b-c) show the agreement between the current model and the TCAD simulation results.

C. *Current Hysteresis Simulation*

By applying the dynamic response of the threshold voltage shift to the calibrated Vth-based IGZO-TFT current model, the current hysteresis characteristics of the IGZO-TFT can be obtained. Fig. 7(a-c) show the hysteresis curves of the transfer characteristics for an IGZO-TFT with W = 20um, L = 20um, $N_{t,shallow} = 3 \times 10^{12} cm^{-2}$ and $V_d = 1.1V$ at different scan rates. It can be found that the shallow energy level traps do not significantly change the subthreshold slope of the device during the scan, but the hysteresis width tends to increase and then decrease with decreasing scan rate. Fig. 7(d–f) show the dynamic hysteresis with $N_{t,deep} = 3 \times 10^{11} cm^{-2}$ and reveal that the earlier appearance of the step-down causes the transfer characteristic curve to shift to the right as the scan rate decreases during forward scanning for deep traps. In addition, the change in subthreshold slop caused by the shallow trap compared to the deep trap is negligible as its energy level is further away from the Fermi energy level, making it more difficult for carriers to be captured by them.

The scan rate dependence of the hysteresis width is quantified by using a fixed current method. For the curves in Fig. 7 the difference of the gate voltage corresponding to the forward and backward sweep at Ids = 1nA is obtained as hysteresis width for our dynamic model and TCAD numerical results (Fig. 8), where the ramp time indicates the time

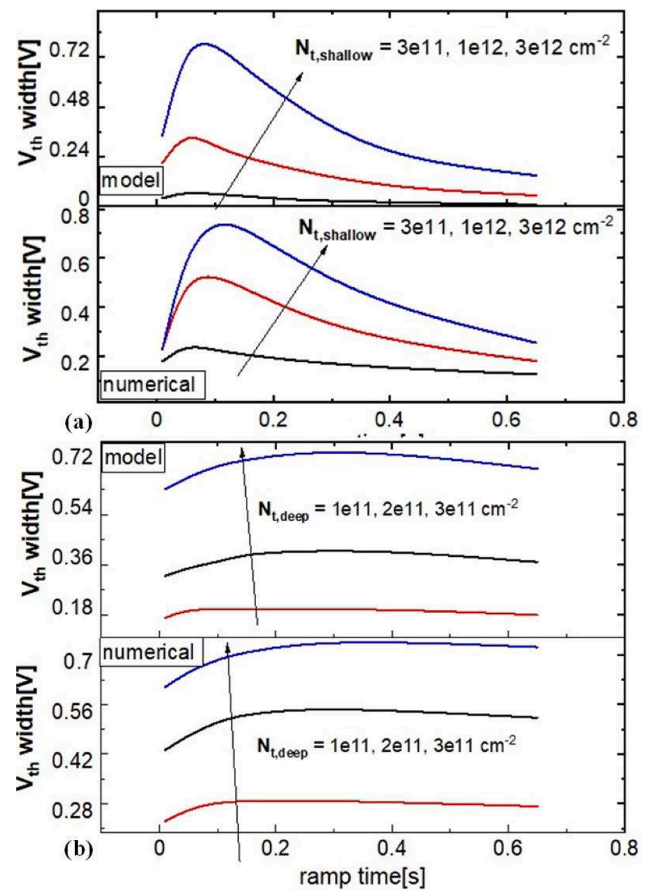

Fig. 8. Dependence of hysteresis width on scan rate at different interface trap densities for (a) shallow energy level traps, (b) deep energy level traps.

required to increase by 0.25 mV.

5. Conclusion

A dynamic current hysteresis model of IGZO-TFT is developed in this work. The trap dynamics described by the two-state trap model can be accurately solved by the sub-circuit method. Combined with the calibrated static current model, the dynamic model developed in this paper can well capture the effect of trap energy level and trap density on hysteresis width, while accurately reflecting the dependence of hysteresis width on scan rate. [13].

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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