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A comprehensive Pelgrom-based on-current variability model for FinFET, NWFET and NSFET☆

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ABSTRACT

We present a novel Pelgrom-based predictive (PBP) model to estimate the impact of variability on the on-current of different state-of-the-art semiconductor devices. In this work, we focus on two of the most problematic sources of variability, the metal grain granularity (MGG) and the line edge roughness (LER). This model allows us to make an accurate prediction of the on-current standard deviation σI_{on}, being the relative error of the predicted data lower than 8% in 92% of the studied cases. The PBP model entails an immense reduction in the computational cost since once it is calibrated for an architecture, the prediction of the impact of a variability on devices with any given dimension can be made without any further simulations. This model could be useful for predicting the effect of variability on future technology nodes.

1. Introduction

The scaling of semiconductor devices is essential for the progress of the electronic industry, but their small size requirements make them more vulnerable to different sources of variability. The metal grain granularity (MGG) and the line edge roughness (LER) are two of the variability sources that have the greatest impact on state-of-the-art transistor architectures [1]: FinFETs, nanowire (NW) FETs, and nanosheet (NS) FETs. Technology computer-aided design (TCAD) is commonly used in variability studies since, to obtain statistical significance, we require the analysis of a large number of samples. The computational cost of on-region variability studies can be prohibitive because either quantum-corrected (QC) Monte Carlo (MC), or full quantum simulations are necessary to properly capture non-equilibrium transport effects. For this reason, new strategies are needed to reduce the computational times of statistical studies [2,3].

In this work, we propose a novel Pelgrom-based predictive (PBP) model to estimate the on-current (I_{on}) variability due to MGG and LER, for three state-of-the-art architectures (FinFET, NWFET, and NSFET). The structure of this paper is as follows. Section 2 presents the assumptions, the calibration, and the accuracy of the model for MGG (Section 2.1), and LER (Section 2.2), together with the computational cost of the model (Section 2.3). Finally, the main conclusions of this work are presented in Section 3.

2. Pelgrom-based σI_{on} predictive model

Pelgrom's Law [4] states that the standard deviation of a figure of merit, I_{on} in this particular case, is proportional to the inverse square root of the effective gate area, defined as the product between the gate length (L) and the effective gate perimeter (W) [5,6]:

$$\sigma I_{on} = \frac{A_i}{\sqrt{LW}}, \tag{1}$$

where A_i is the on-current matching factor, determined by the contributions of all possible sources of transistor variations [7].

There are previous studies for multigate transistors that show that MGG and LER variabilities follow the Pelgrom's law [8,9]. Therefore, we have developed two models based on Pelgrom's Law, for these two sources of variability, applying them to the three architectures shown in Fig. 1: (a) NWFET, (b) FinFET, and (c) NSFET. To validate the PBP model we have used data published by different authors [10–13] combined with simulations that were specifically done for this study using QC MC methodology in VENDES [14] tool.

2.1. PBP model for MGG

The MGG variability is implemented in TCAD studies by generating random grain distribution in the gate using the Poisson–Voronoi

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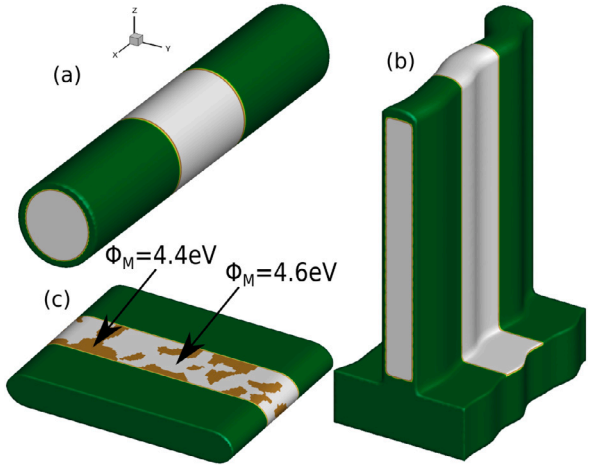

Fig. 1. Scheme of a (a) NWFET not affected by any variability source, (b) FinFET affected by LER variability, and (c) NSFET affected by TiN MGG with two gate work-functions (ϕ_M).

diagram methodology depending on the average grain size (GS) (see Fig. 1(c)), this methodology has been validated against experimental data in [15]. As all devices of this work have a TiN metal gate, the generated profiles have two metal grain orientations with work-functions of 4.4 eV, and 4.6 eV, and occurrence probabilities of 40%, and 60%, respectively. The GS is determined by the annealing temperature and deposition time of the metal gate deposition process [16]. To develop the PBP model for MGG variability, we assume that MGG is the sole contributor to transistor variations, and therefore $A_i = A_{mgg}$. Also, we assume that σI_{on} depends linearly on the GS as reported in [10,12], leading to the PBP model for MGG:

$$\sigma I_{on} = A_{mgg}\frac{1}{\sqrt{LW}} = \theta_{mgg}\frac{GS}{\sqrt{LW}} \tag{2}$$

We define the θ_{mgg} as the on-current mismatch for MGG, which is a technological parameter that states how the variability impacts a certain architecture, and once is determined, σI_{on} could be predicted for any device dimensions at any GS.

The PBP model plots for MGG are shown for the three architectures in Fig. 2(a)–(c). The minimum sample size used for each set of simulations is 300 in order to obtain statistical significance. The black line is the reference line that denotes the fitting of the model, where the error bars correspond to 10% of the relative error with respect to the simulated data, a tolerance that we consider acceptable. As can be seen, the majority of the predictions are inside the 10% margin. Table 1 presents the predicted (σI^P_{on}) and simulated (σI^S_{on}) on-current standard deviations together with the relative error (σ_r) between them, the GS, the θ_{mgg}, and dimensional information of the devices (LW). The estimations outside the 10% margin of error are highlighted in bold in the table, and are due to the saturation of the standard deviation in devices with small LW and large GS (i.e. NWFET L = 10 nm with GS = 7 nm and 10 nm), this phenomenon is described in [17].

2.2. PBP model for LER

LER variability is reproduced in TCAD studies using the Fourier transform of the Gaussian spectra [18] (see Fig. 1(b)), depending on two parameters: the root mean square height (Δ, depth of the roughness) and the correlation length (Λ, propagation of the roughness). In this case, the LER is the sole contributor to variability $A_i = A_{ler}$. Also, we assume that σI_{on} increases linearly with Δ (see [1,12]), depending on the square root of the product between the device width (w) and a function of Λ, which is empirically defined as:

$$f(\Lambda) = \Lambda \cdot \left[1 - e^{-\sqrt{\frac{L}{\Lambda}}}\right] \tag{3}$$

Table 1
Predicted (σI^P_{on}) vs. simulated (σI^S_{on}) on-current standard deviations, at different GS for each architecture. In the table, we also list the on-current mismatch θ_{mgg}, the gate effective gate area (LW), and the relative error σ_r.

	GS	σI^P_{on}	σI^S_{on}	θ_{mgg} = 120 nA/nm		Ref.
	[nm]	[A/m]	[A/m]	σ_r	L × W [nm²]	
NWFET	3	23.8	25.0	−4.8%	10.0 × 22.8	[12]
		11.5	12.5	−8.0%	22.0 × 44.9	[12]
	5	39.7	42.5	−6.6%	10.0 × 22.8	[12]
		19.1	19.0	+0.5%	10.0 × 35.2	[11]
		32.0	33.0	−5.3%	22.0 × 44.9	[12]
	7	55.6	47.7	**+16.6%**	10.0 × 22.8	[12]
		26.7	26.3	+1.5%	22.0 × 44.9	[12]
	10	79.5	67.7	**+17.4%**	10.0 × 22.8	[12]
		38.2	42.4	−9.9%	22.0 × 44.9	[12]
	GS	σI^P_{on}	σI^S_{on}	θ_{mgg} = 192 nA/nm		Ref.
	[nm]	[A/m]	[A/m]	σ_r	L × W [nm²]	
FinFET	3	14.9	15.0	−0.7%	25.0 × 60.0	[a]
		16.3	16.3	+0.0%	12.0 × 105.0	[a]
	5	52.7	58.6	−8.4%	10.7 × 30.0	[10]
		24.9	24.9	+0.0%	25.0 × 60.0	[a]
		27.1	27.1	+0.0%	12.0 × 105.0	[a]
	7	75.2	75.9	−0.9%	10.7 × 30.0	[10]
		34.8	36.4	−4.5%	25.0 × 60.0	[a]
		38.0	35.3	+7.6%	12.0 × 105.0	[a]
	10	107.4	105.9	+1.4%	10.7 × 30.0	[10]
		49.7	47.1	+5.5%	25.0 × 60.0	[a]
		54.2	53.3	+1.7%	12.0 × 105.0	[a]
	GS	σI^P_{on}	σI^S_{on}	θ_{mgg} = 191 nA/nm		Ref.
	[nm]	[A/m]	[A/m]	σ_r	L × W [nm²]	
NSFET	3	15.8	15.2	+3.9%	12.0 × 110.0	[13]
		10.5	11.4	−7.9%	18.0 × 165.3	[a]
	5	26.3	25.0	+5.2%	12.0 × 110.0	[13]
		17.5	16.5	+6.1%	18.0 × 165.3	[a]
	7	36.8	36.5	+1.0%	12.0 × 110.0	[13]
		24.5	24.8	−1.2%	18.0 × 165.3	[a]
	10	52.6	52.3	+0.7%	12.0 × 110.0	[13]
		35.0	32.8	+6.7%	18.0 × 165.3	[a]

[a]The simulations done for this work are referenced.

Thus, the PBP model for LER will be as follows:

$$\sigma I_{on} = A_{ler}\frac{1}{\sqrt{LW}} = \theta_{ler}\cdot\Delta\sqrt{\frac{f(\Lambda)\cdot w}{LW}}, \tag{4}$$

where θ_{ler} is the on-current mismatch for LER, a parameter that states the dependence of variability due to an architecture, and once is fixed, the estimation of σI_{on} could be done at any dimensions (L, W, w), Δ, or Λ.

The PBP model plots are shown in Fig. 3(a)–(b) for NWFET and FinFET due to LER-induced variability, respectively. Also, in Fig. 3(c) we show a comparison between the simulated and predicted σI_{on} due to LER variability, together with the shaded region where the deviations are lower than 10% from the expected value for the 22 devices studied. The NSFET is not studied for LER variability since, the impact on I_{on} is negligible for this architecture because the roughness due to the etching processes is on the non-critical dimension, this could be seen in [1]. We can see a good match between the predicted and the simulated data for different values of Δ, Λ, different dimensions, and architectures.

2.3. Computational cost

Once the model's accuracy has been tested, we present another advantage of the PBP model, the reduction of computational cost. In this section, we compare the computational cost of performing a

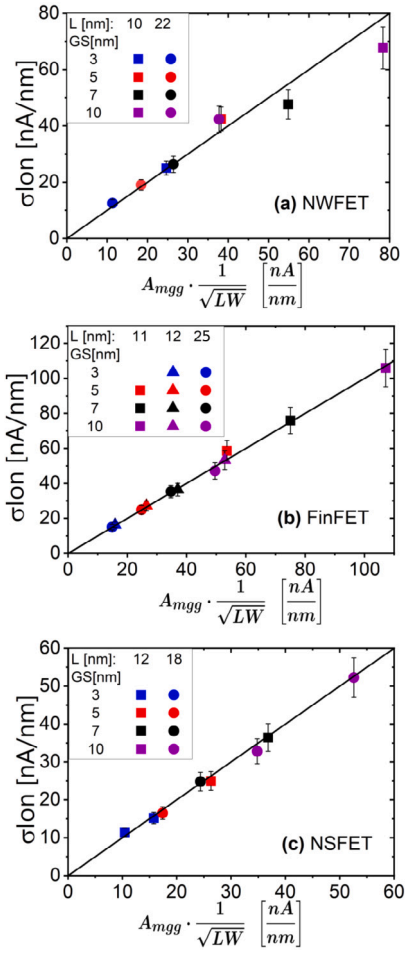

Fig. 2. Pelgrom-based predictive (PBP) plots for MGG variability for three state-of-the-art different architectures: (a) NWFET, (b) FinFET, and (c) NSFET. The gate length L of the devices, together with the GS are also shown.

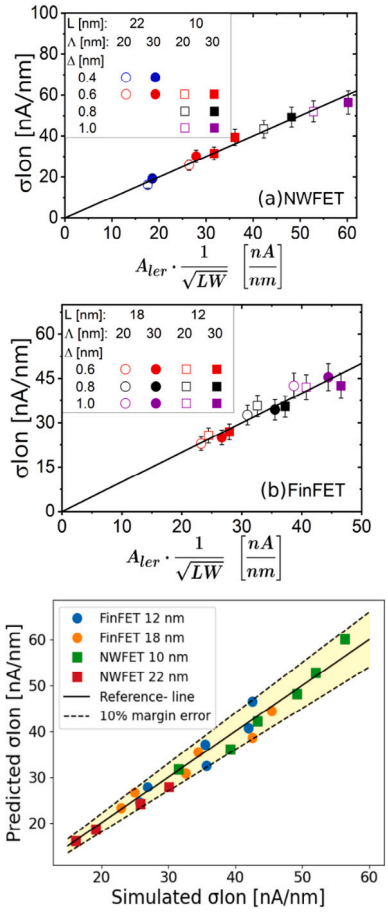

Fig. 3. PBP plots for LER variability impact on σI_{on} for two state-of-the-art different architectures: (a) NWFET, (b) FinFET. Also, in (c) is shown a comparison between data predicted with the PBP model and the simulated data due to LER. The gate length L of the devices, together with the variability parameters for LER (Δ and Λ), are also shown.

variability study through TCAD simulations versus the calibration and application of the PBP model.

To calibrate the model for MGG (LER), we only need the simulation of the sets (300 simulations per set) for an architecture at four different GS (Δ or Λ) values. The computational time for a single simulation of a 10 nm NWFET affected by MGG or LER variability with QC MC methodology using VENDES software on Intel$^{(R)}$ Core$^{(T_M)}$ i9-10 850 K CPU at 3.60 GHz with a memory DDR4 with 3200 MT/s is around 25 h. Fig. 4 shows a comparison of the computational time required for a QC MC TCAD study for several dimensional devices with a common architecture (NWFET) affected by MGG variability. Also, the calibration time for the PBP model is shown. Note that this time matches the computational cost of one TCAD simulation variability study. Once the PBP model is calibrated, the computational time on estimating the impact of variability on new devices does not increase. As can be seen, the reduction in computational time by using the PBP model is significant as the number of devices increases. Therefore, this model can help to predict the impact of future technology nodes with a reduced computational cost.

3. Conclusions

In conclusion, we have presented a new comprehensive on-current variability prediction model for MGG and LER based on Pelgrom's Law.

PBP model has been tested for three state-of-the-art architectures, with prediction errors lower than 8% in the 92% of the cases. The application of the PBP model implies a huge reduction of the computational

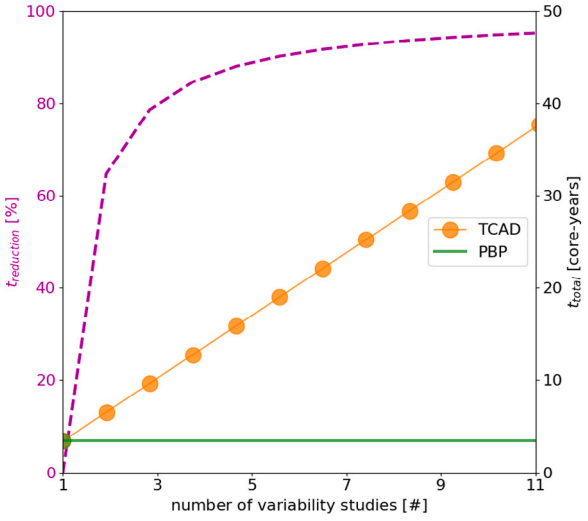

Fig. 4. Computational time in the estimation of the on-current standard deviation (σI_{on}) due to MGG versus the number of variability studies. The simulation time of QC MC TCAD is compared to that of the PBP model. Each TCAD point of the graph corresponds to a complete variability study (four GS values) for several devices. The reduction in computational cost derived from the application of the PBP model compared to TCAD is also shown.

time in comparison with QC MC TCAD variability studies. Also, the power of the model allows us to predict the impact of MGG and LER on any device for a calibrated architecture with no further simulations.

Hence, the PBP model is a simple, fast, and reliable strategy to estimate the impact on the transistor performance of a certain source of variability. This model could be useful to predict the impact of variability on future technology nodes.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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References

[1] Seoane N, Fernandez JG, Kalna K, Comesaña E, García-Loureiro A. IEEE Electron Dev Lett 2021;42(10):1416–9. http://dx.doi.org/10.1109/LED.2021.3109586.
[2] Carrillo-Nuñez H, Dimitrova N, Asenov A, Georgiev V. IEEE Electron Dev Lett 2019;40(9):1366–9. http://dx.doi.org/10.1109/LED.2019.2931839.
[3] Indalecio G, Seoane N, Kalna K, Garcia Loureiro A. IEEE Trans Electron Dev 2017;64:1–7. http://dx.doi.org/10.1109/TED.2017.2670060.
[4] Pelgrom M, Duinmaijer A, Welbers A. IEEE J Solid-State Circuits 1989;24(5):1433–9. http://dx.doi.org/10.1109/JSSC.1989.572629.
[5] Sheikholeslami A. IEEE Solid-State Circuits Mag 2015;7(1):8–9. http://dx.doi.org/10.1109/MSSC.2014.2369331.
[6] Lu N, Brown JS, Thoma R, Kotecha PM, Wachnik RA. IEEE IEDM 2014;35.3.1–4.. http://dx.doi.org/10.1109/IEDM.2014.7047174.
[7] Stolk P, Widdershoven F, Klaassen D. IEEE Trans Electron Dev 1998;45(9):1960–71. http://dx.doi.org/10.1109/16.711362.
[8] Nayak K, Agarwal S, Bajaj M, Oldiges PJ, Murali KVRM, Rao VR. IEEE Trans Electron Dev 2014;61(11):3892–5. http://dx.doi.org/10.1109/TED.2014.2351401.
[9] Sudarsanan A, Venkateswarlu S, Nayak K. IEEE Trans Electron Dev 2019;66(11):4646–52. http://dx.doi.org/10.1109/TED.2019.2941896.
[10] Seoane N, Indalecio G, Aldegunde M, Nagy D, Elmessary MA, García-Loureiro AJ, Kalna K. IEEE Trans Electron Dev 2016;63(3):1209–16. http://dx.doi.org/10.1109/TED.2016.2516921.
[11] Sung W-L, Yang Y-S, Li Y. IEEE J Electron Dev Soc 2021;9:151–9. http://dx.doi.org/10.1109/JEDS.2020.3046608.
[12] Nagy D, Indalecio G, GarcíA-Loureiro AJ, Elmessary MA, Kalna K, Seoane N. IEEE J Electron Dev Soc 2018;6:332–40. http://dx.doi.org/10.1109/JEDS.2018.2804383.
[13] Nagy D, Espiñeira G, Indalecio G, García-Loureiro AJ, Kalna K, Seoane N. IEEE Access 2020;8:53196–202. http://dx.doi.org/10.1109/ACCESS.2020.2980925.
[14] Seoane N, Nagy D, Indalecio G, Espiñeira G, Kalna K, García-Loureiro A. Materials 2019;12(15). http://dx.doi.org/10.3390/ma12152391.
[15] Indalecio G, García-Loureiro AJ, Seoane Iglesias N, Kalna K. IEEE Trans Electron Devices 2016;63(6):2625–8. http://dx.doi.org/10.1109/TED.2016.2556749.
[16] Dadgour H, Endo K, De V, Banerjee K. Ieee iedm. 2008, p. 1–4. http://dx.doi.org/10.1109/IEDM.2008.4796792.
[17] Fernandez JG, Seoane N, Comesaña E, Kalna K, García-Loureiro A. SISPAD 2021;201–5. http://dx.doi.org/10.1109/SISPAD54002.2021.9592600.
[18] Asenov A, Kaya S, Brown A. IEEE Trans Electron Dev 2003;50(5):1254–60.. http://dx.doi.org/10.1109/TED.2003.813457.