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28 nm FD-SOI MEOL parasitic capacitance segmentation using electrical testing and semiconductor process modeling

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ABSTRACT

This paper describes an extraction methodology for segmenting the different contributions to interconnect and contact driven parasitic capacitance present on a 28 nm Fully Depleted Silicon On Insulator technology. The segmentation was enabled by creating specific test structures that had been designed, processed, and electrically tested across full wafer mappings. A 3D semiconductor process model, including capacitance extraction, was subsequently built and calibrated using the statistical distribution of actual silicon data. Once fully calibrated (<3% mean deviation to actual data), the model was used to understand the sensitivity of parasitic capacitance to specific process/design parameters and to enable Design Technology Co-Optimization.

1. Introduction

As MOS transistor dimensions continue to decrease, parasitic capacitance introduced by source/drain contacts are increasing [1] and need to be accurately estimated during logic circuit design. Analytical [2–5], 2-D [6,7] or 3-D TCAD models [8] are generally used to estimate the fringe capacitances in MOSFET devices, and to understand their relationship with process parameters such as gate height or source/drain epitaxy thickness. However, in these models, assumptions are made to simplify the geometry of devices compared to the actual morphology on silicon. In this paper, we propose to quantify the parasitic capacitance between source/drain contacts and MOS transistors gates on a 28 nm FD-SOI MOSFET structure and will do so by using a geometrically accurate 3-D virtual process model and calibrating it against actual wafer measurements.

2. Experimental and simulation methodology

To extract the contribution of poly-to-contact capacitance in interconnect stack, we designed dedicated structures on a silicon wafer with various transistors geometries. In parallel, a 3-D process model is calibrated on silicon to fit the electrical measurements and provide insights on design/technology interactions.

2.1. Test structure details and electrical-test segmentation

Transistors designs were considered with two channel width (W) and length (L) geometries (W/L = 1/0.3 μm and W/L = 0.21/0.3 μm) along with three poly-to-contact (Po2Co) distances (0.037/0.074 and 0.111 μm). In all structures, the transistors are isolated from the bulk substrate to decorrelate the MOS contribution during parasitic extraction.

Each transistor design is finally duplicated in two de-embedded test structures configurations to extract the contribution of poly-to-contact parasitic capacitance:

- Configuration A, with poly on shallow trench isolation (STI) and source/drain contacts on STI;
- Configuration B, with poly on STI but without source/drain contacts.

Minimum, median and maximum capacitance values from the Gate to the Source/Drain were extracted from a silicon-based e-test performed on 98 dies on a wafer.

2.2. Virtual process model calibration

SEMulator3D® virtual semiconductor process models of each unit test structure were built to better understand the correlation between process parameter changes and the effect on various parasitic capacitances. Three different SEMulator3D® models were considered with

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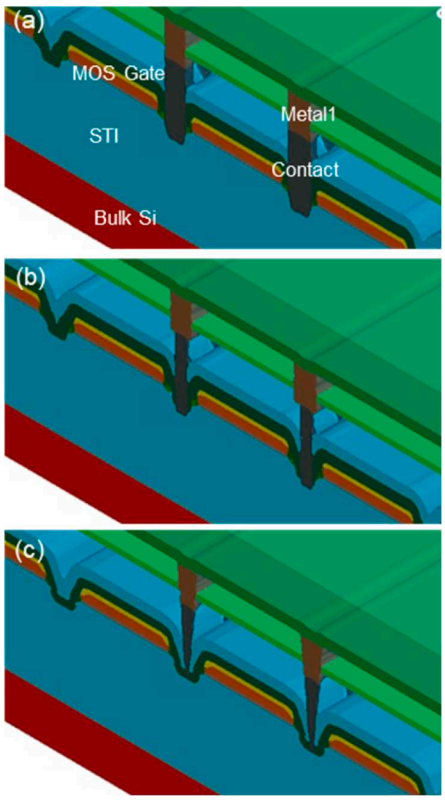

Fig. 1. Three types of process models: a) 3D extruded geometric model from the 2D layout, b) 3D extruded geometric model from the 2D layout with CD corrections, c) 3D silicon realistic. For clarity, some dielectric materials are hidden.

increasing turn-around time and level of accuracy with respect to silicon morphology, as depicted in Fig. 1.

The first model is based on a 3D stack extruded from a 2D layout (Fig. 1a). The second model is a 3D extruded model with Critical Dimension (CD) correction matching of the top CDs for the Via/Lines as measured inline from production lots (Fig. 1b). The final model shown on Fig. 1c describes a full flow calibrated to TEM cross-sections (XTEM). It includes realistic etch models/profiles, lithography corrections (CD) and emulation (corner rounding).

Assumptions have been made on contacts overetch in STI since this configuration is usually not encountered on standard devices (contacts being here electrically not connected to source/drain).

3. Results

3.1. Electrical measurements

The electrical measurements of the two de-embedded configurations are reported for each transistor design in Fig. 2. The contribution of the poly-to-contact capacitance as a portion of the total parasitic capacitance is noted C_{POCO} and is determined as

$$C_{POCO} = C_A - C_B$$

where A and B stands for the two de-embedding configurations described in Section 2.1, C_A corresponding to the total interconnect capacitance per device.

Figs. 2 and 3 illustrate that poly-to-contact capacitance varies between 2 aF and 10 aF per contact. 10–30 % of the total interconnect

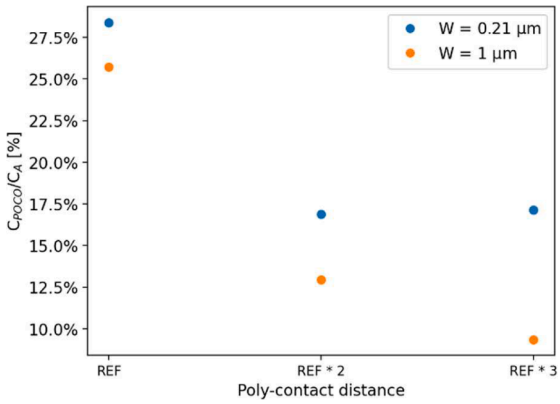

Fig. 3. Relative contribution of the poly-to-contact parasitic capacitance for W = 0.21 µm (blue) and W = 1 µm (orange). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

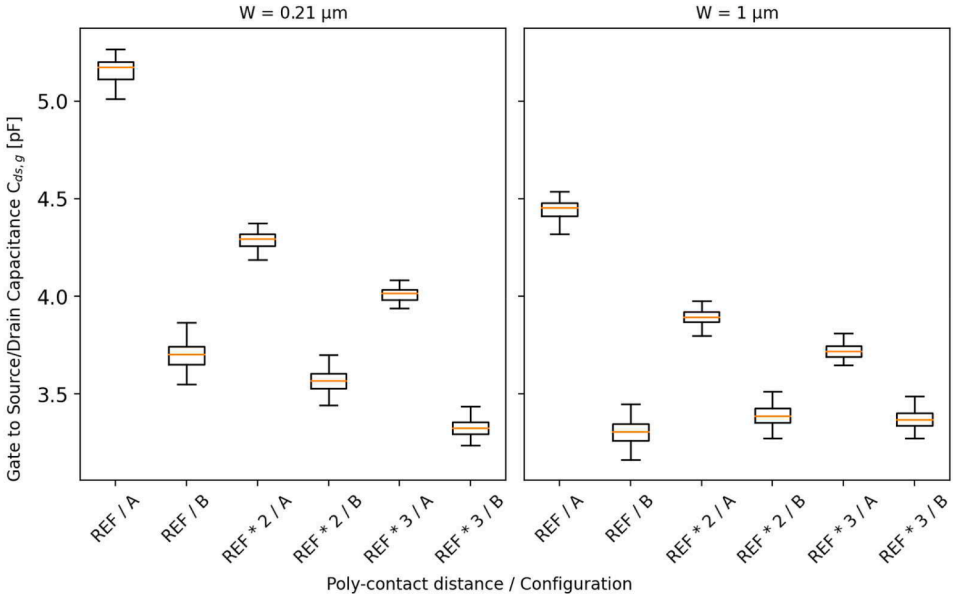

Fig. 2. Gate to Source/Drain Capacitance ($C_{ds,g}$) values extracted from de-embedded structures for W = 0.21 µm (left) and W = 1 µm (right).

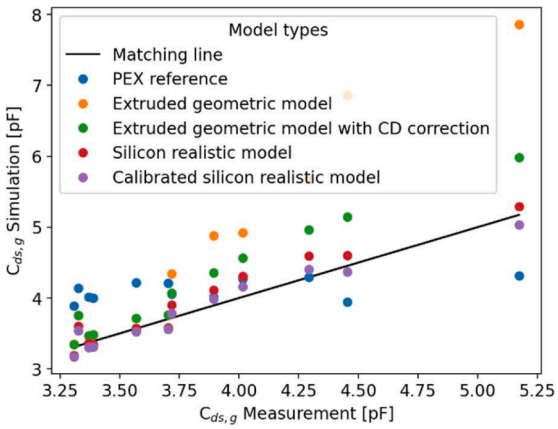

Fig. 4. Comparison between parasitic capacitances measured on 12 different devices and extraction from simulations for different models.

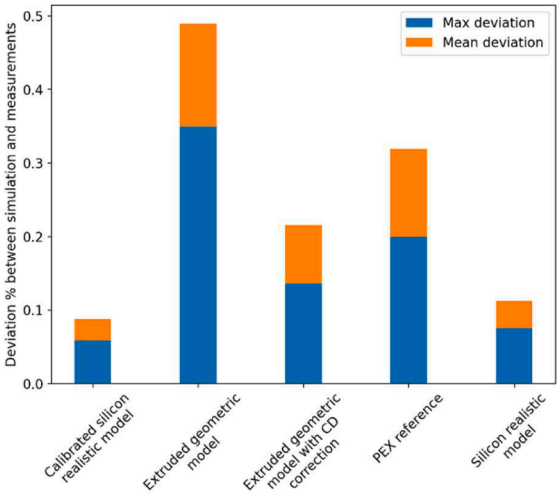

Fig. 5. Deviation percentage between simulation and Si data values.

capacitance is therefore attributed to the tungsten contacts, depending on the transistor design considered (see Fig. 3).

3.2. Model vs measured capacitances

For each of the structures simulated, parasitic capacitance between the gate and the source interconnects and the gate and the drain interconnects were extracted using SEMulator3D®. A standard parasitics extraction procedure (PEX) was used as a reference.

For each transistor design and each of the three model types detailed above, Fig. 4 reports the simulated Gate to Source/Drain parasitic capacitance compared to the normalized (across multiple transistors) mean Gate to Source/Drain Capacitance extracted from Si wafer measurements. The extruded TCAD geometric simulation model shows a similar mean deviation as PEX (12–14 %) when compared to silicon data (see Fig. 5). The more realistic SEMulator3D silicon 3D model shows a much better correlation with the actual silicon data, with the error difference not exceeding 7 %. This demonstrates the importance of properly matching the geometry of the silicon structure to the structure used in simulation, in order to accurately extract electrical (parasitic capacitance) data during simulation.

3.3. Model calibration and process sensitivity analysis

The silicon realistic 3D model was further improved by completing

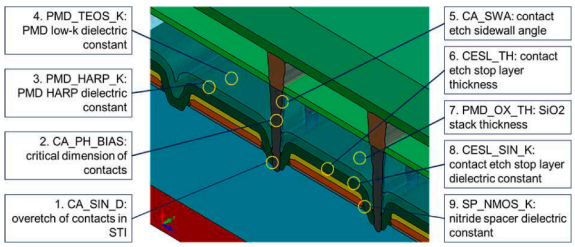

Fig. 6. Process parameters from the silicon realistic model that were used for further calibration.

an additional automatic model calibration step using silicon e-test data. A calibrated model ensures that the model will more accurately reflect the process behavior noticed in silicon.

Nine different process parameters were then selected for further analysis, as detailed in Fig. 6. They involve geometric parameters and dielectric constants of materials from the stack which are expected to affect the poly-to-contact capacitance values:

1 CA_SIN_D: overetch of contacts in STI resulting from the dry etch process;
2 CA_PH_BIAS: photolithography bias i.e. variation of the contacts CD;
3 PMD_HARP_K: dielectric constant of pre-metal dielectric (PMD) high aspect-ratio oxide after deposition and cure;
4 PMD_TEOS_K: dielectric constant of pre-metal dielectric TEOS oxide after deposition and cure;
5 CA_SWA: sidewall angle of contact hole after dry etch and tungsten filling process;
6 CESL_TH: thickness of conformal nitride contact etch stop layer;
7 PMD_OX_TH: total thickness of PMD oxide layers;
8 CESL_SIN_K: dielectric constant of conformal nitride contact etch stop layer;
9 SP_NMOS_K: dielectric constant of nitride used as MOS spacer material.

A large virtual Design Of Experiment (DOE) was executed by completing 200 virtual experiments on each of the 12 devices. In the experiment, parameter values were varied by generating and assigning Monte Carlo normal distribution values to each of the nine selected process parameters. For the CDs and thicknesses, the extreme values are taken from inline measurements performed on the tested wafer lot. For the rest of the parameters like dielectric constants or sidewall angles, the limits are set based on typical values obtained from offline characterizations.

Silicon wafer mean values for all 12 devices were collected and compared to the simulation data. A regression analysis was performed to calibrate the 9 process parameters and further optimize the correlation to Si data. Using the results shown in Fig. 4, a "Calibrated Silicon Realistic Model" was simulated and produced a deviation to silicon e-test data of only 2.9 % and 5.9 % (mean and maximum values, respectively). This deviation is lower than any of the other models. The statistical data obtained from the DOE (a total of 2400 virtual experiments) was subsequently used to determine the sensitivity of the calculated parasitic capacitance values to each of the selected process parameters.

Table 1
Process parameters and cross-term parameters ranked based upon their weight in affecting Gate to Source/Drain parasitic capacitance.

Parameter	P-Value	Weight
CESL_SIN_K	0.0128	−1.098
CA_SWA	<0.001	−0.3113
CESL_SIN_K× PMD_HARP_K	0.0025	0.167
CESL_SIN_K× PMD_TEOS_K	<0.001	0.1583
CA_PH_BIAS	<0.001	0.1155

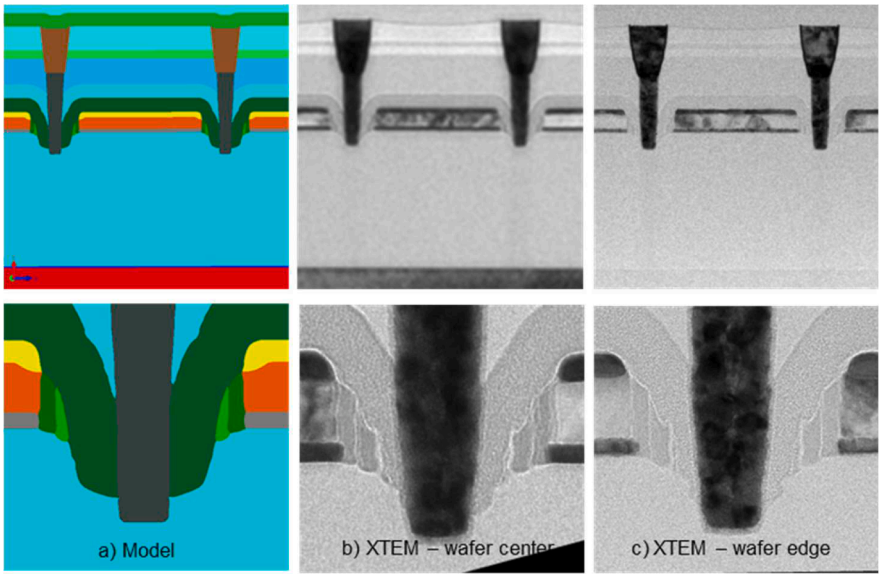

Fig. 7. Comparison of output of virtual fabrication model after automatic calibration (a) and the same structure cut in XTEM at the center (b) and edge (c) of the wafer.

Focusing on a real MOS structure (including interconnects, contacts and active components), Table 1 illustrates the weight, from highest to lowest, of the most significant process parameters and their cross-terms that affect the parasitic contribution of Gate to Source/Drain capacitance. P-values refer to the probability of their statistical significance occurring by chance i.e. the lower the p-Value, the higher the statistical significance of a given parameter. The table highlights the most important parameters that can be controlled or adjusted to reduce parasitics.

4. Discussion

P-values from Table 1 show that the statistical significance of these process parameters is high, confirming that poly-to-contact parasitic capacitance are strongly related to the geometry of the contact itself and the relative permittivity of the silicon nitride layer acting as a contact etch stop layer. Regarding this, it is important to verify that the output of the 3D model calibration is accurate and matches the actual topology on silicon samples.

XTEM performed on measured wafer are compared to the calibrated output virtual fabrication model in Fig. 7. The direct comparison of characterized and simulated devices confirms the assumptions made on contacts dimensions (especially on overetch distance in STI) which is furthermore validated by XTEM at the edge of the wafer. This result gives promising insights on the validity of this methodology and allows to extrapolate it to any complex interconnects topology.

5. Conclusions

Independent parasitic contributions of contacts and interconnects on Gate to Source/Drain capacitance were identified, using test structures specifically fabricated, tested and simulated for that purpose. The simulation results included a large statistical data set (2400 experiments). This data set was used to build the correlation between nine different process parameters and measured capacitance on various test structures (including a complete MOS structure). Six significant process parameters (including cross term factors) were identified as the most important parameters to control, in order to reduce and better control the fringe capacitance of MOSFETs. The simulation results were highly predictive (<3% mean deviation) when compared to actual wafer data, as long as accurate, well-calibrated structural geometries were used during the process model simulation and electrical analysis.

Declaration of Competing Interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Benjamin Vianne reports financial support was provided by STMicroelectronics.

Data availability

The data that has been used is confidential.

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