

RF performance improvement on 22FDX® platform and beyond

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Abstract—The paper describes manufacturing process and layout optimizations to improve RF performance of 22FDX® N/PFET devices, based on a comprehensive calibration of DC and RF figures of merit. Process and Device simulations of the individual and combined elements show f_t/f_{max} improvement up to about 1.13/1.1x (NFET) and about 1.32/1.24x (PFET) over standard devices mainly driven by mechanical stress and parasitic R/C elements.

Keywords—FDSOI, f_t , f_{max} , 22FDX®, TCAD, RF, mmWave

I. INTRODUCTION

The benefits of 22FDX® in terms of ultra low leakage and power applications as well as RF features have been extensively analyzed in several publications [1,2,3]. This paper is now focusing on the TCAD simulation of further manufacturing processes and layout options to enhance RF performance for mmWave devices. Section II discusses the calibration of DC and RF Figures-of-Merit (FoMs) for both NFET and PFET devices. The calibration procedure in mixed-mode includes intrinsic transistor behavior as well as parasitic RC components, extracted after a layout analysis. Section III of the paper analyzes RF performance elements such as poly-poly pitch, gate length, different raised Source/Drain options and additional PFET Middle-of-Line stressors in detail. Significant increase in f_t and f_{max} can be achieved by merging the single elements together.

II. PROCESS FLOW AND TCAD CALIBRATION

A. Process flow

The manufacturing processes relevant for the RF analysis of single devices consists of Front-End-of-Line until Metall, since de-embedding procedure removes Back-End-of-Line parasitic elements from the measurement data. 22FDX® FEOL features are Si/SiGe channel as well as in-situ doped Si/SiGe raised source/drain for N/PFET, a high-k metal gate process with tensile strained liner to improve NFET performance with minimal impact on PFET devices. Flip-well (Super Low V_{th}) architecture allows further forward back biasing and exceptional low noise behavior due to low channel doping [1,2].

B. TCAD calibration

Process and device simulations have been performed with SENTAURUS TCAD including quantum-drift-diffusion framework, thin layer mobility, mechanical stress modulation of mobility and band structure. By implementing relevant process steps and doing careful structural matching to inline and TEM data (Fig.1) a solid DC matching to

median values of the electrical test parameters can be achieved as shown in Fig.2 for NFET and Fig.3 for PFET devices. Parasitic resistances and capacitances from salicidation and contact process are included according to the layout of the measured devices and by considering additional measurements from specific test structures like contact chains.

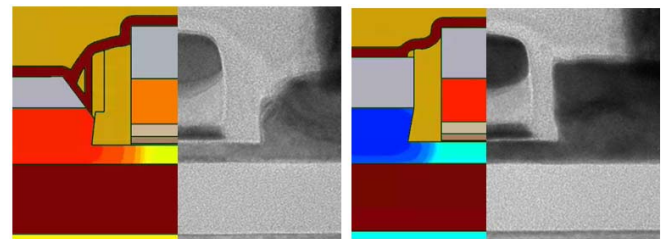


Fig. 1. TCAD and TEM cross section of a) NFET and b) PFET, along the channel

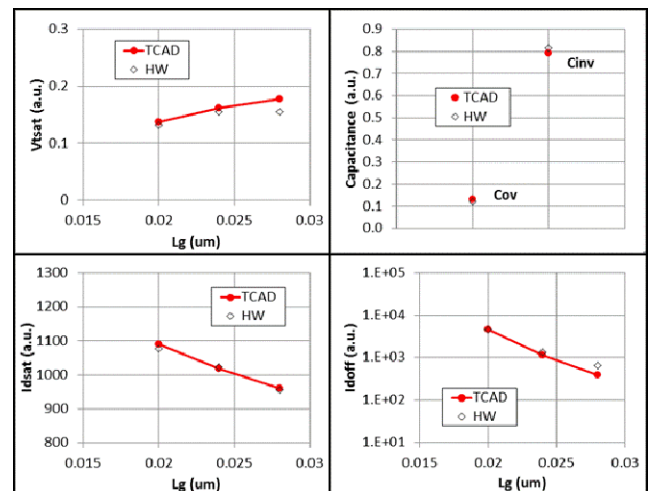


Fig. 2. NFET DC calibration across gate length (TCAD - line / HW - symbols)

Additionally, simulation time reduction could be achieved by simulating only one finger of the typical multi-finger RF devices by taking into account the active length effect on mechanical stress and the change in effective contact resistance

The resulting I_dV_g and G_mV_g characteristics in saturation ($V_d=V_g=0.8V$) of a typical device are shown in Fig.4 (NFET) and Fig.5 (PFET). These comparisons illustrate that TCAD simulations well reproduce the device

DC behavior in the sub-threshold regime, at low as well as in high inversion regimes, with a particular focus on the transconductance behavior over gate bias, which is an important parameter for the RF FoMs. In order to match f_t and f_{max} a careful analysis of the test structure (Fig.6) is essential to include the necessary parasitic components into the mixed mode simulation. Therefore additional separate 3D simulations have been performed to quantify the gate overhang and substrate capacitances as well as gate to contact and Metal capacitance (Fig.7). After taking into account all the above mentioned elements in a mixed-mode simulation, a good fit matching over gate bias as well as over drain current can be achieved as shown in Fig.8 (NFET) and Fig.9 (PFET).

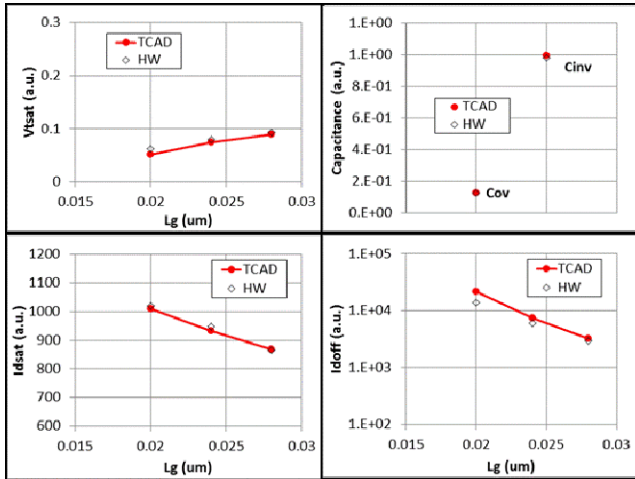


Fig. 3. PFET DC calibration across gate length (TCAD - line / HW - symbols)

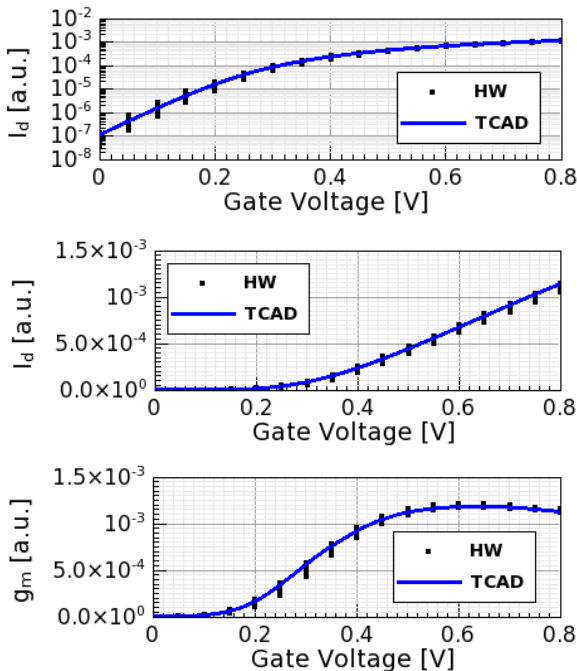


Fig. 4. Comparison of TCAD (line) against HW (symbols) in terms of I_dV_g and g_mV_g characteristics for a typical NFET device.

Having f_t calibrated, f_{max} is mainly impacted by gate resistance. Here the high-k metal gate first technology includes a couple of parallel and series resistances, namely the MetalGate-PolySilicon, PolySilicon-Salicide and

Salicide-Contact interfaces and the MetalGate, Polysilicon, Salicide and Contact itself. Putting all of them together with the parasitic capacitances in a network of lumped elements, f_{max} will follow f_t (Fig.8-NFET / Fig.9-PFET). The calculated gate resistance out of simulated S-Parameter matrix can be compared to the measured values for reference.

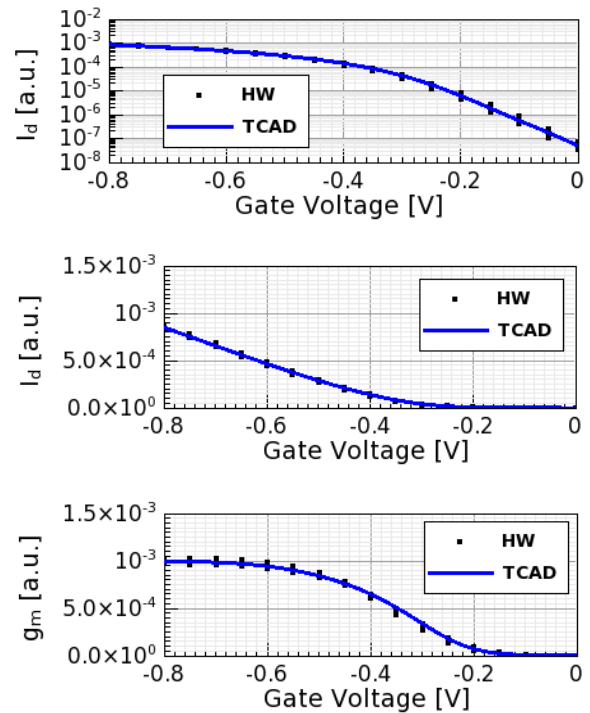


Fig. 5. Comparison of TCAD (line) against HW (symbols) in terms of I_dV_g and G_mV_g characteristics for a typical PFET device.

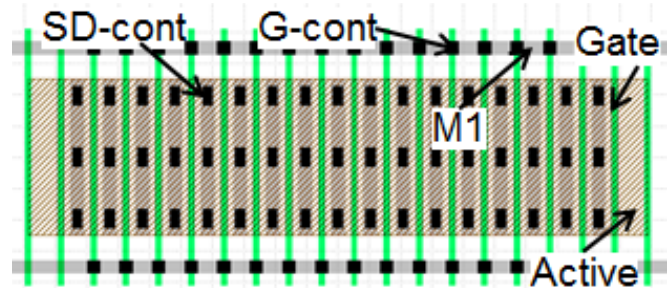


Fig. 6. Layout of RF single device test structure using Multi-Finger architecture and top/bottom gate contacts

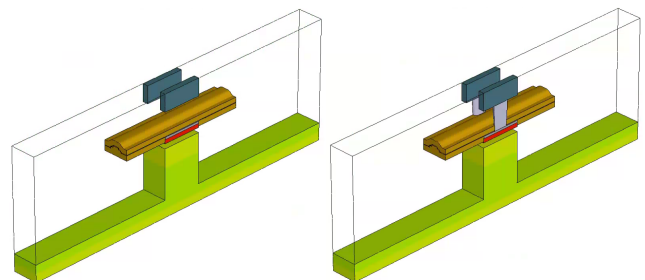


Fig. 7. 3D simulation structure to quantify parasitics of a) poly overhang to S/D/Substrate and b) poly to contact and Metal1 layer

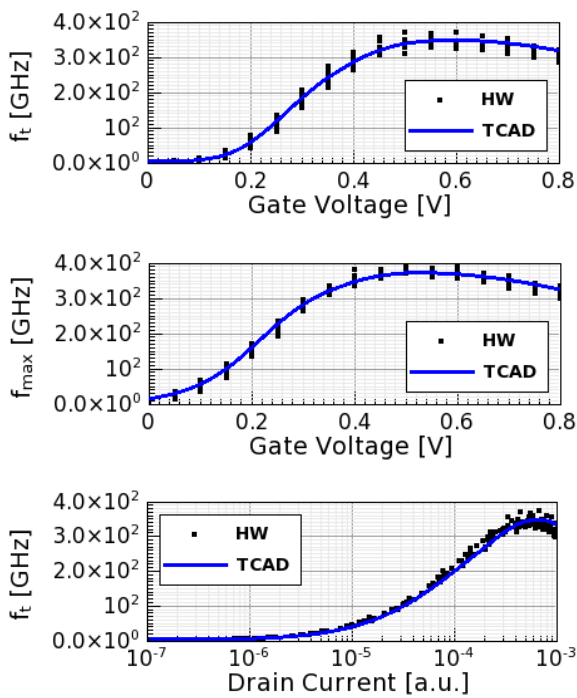


Fig. 8. f_t/f_{max} calibration for NFET (TCAD - solid line / HW - squares)

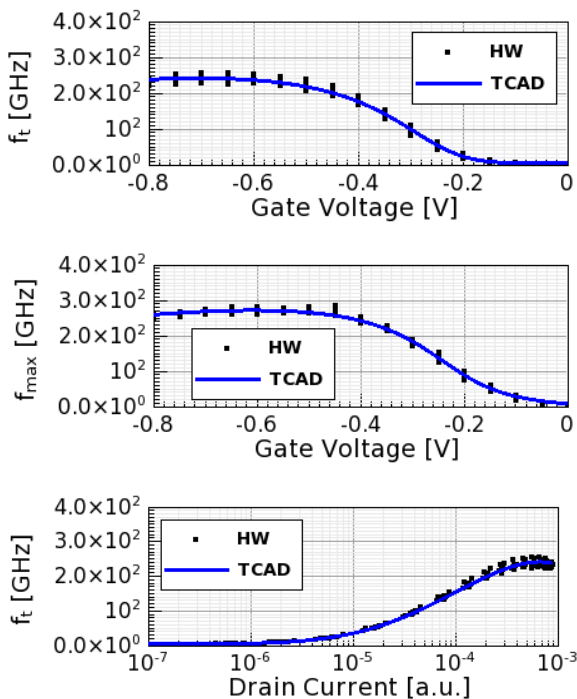


Fig. 9. f_t/f_{max} calibration for PFET (TCAD - solid line / HW - squares)

III. RF OPTIMIZATION KNOBS

A. Individual elements analysis

Improvement of the RF FoMs f_t and f_{max} can be done in two ways: by manufacturing process and by layout optimization. The considered elements in this study are summarized in Fig.10 and their independent relative impact on f_t , f_{max} , g_m are given in Fig.11 (NFET) and Fig.12 (PFET).

The process optimizations investigated here are 2 different raised S/D options and the introduction of a Middle-of-Line stressor element for PFET devices. With careful implementation, raised S/D modifications are mainly reducing the parasitic capacitance with only marginal impact on transconductance. The 2 raised S/D options consist of an epitaxy height reduction and the implementation of a partial facet epitaxy [4]. Adding the Middle-of-Line stressor element to the PFET device boosts uniaxial strain and improves g_m significantly, hence increases f_t and f_{max} .

An option combining manufacturing process and layout optimization is the gate length reduction. This is enabled by the intrinsic superior electrostatic control of FDSOI architecture. In addition, the increased Idoff leakage due to shorter L_{gate} is not detrimental for many RF applications. Thus, a lower effective inversion capacitance as well as higher transconductance as a consequence of shorter channel length is beneficial for RF FoMs g_m and f_t . Interestingly, f_{max} remains stable since the L_{gate} reduction brings about an R_{gate} increase, which eventually compensates the capacitance and transconductance benefits. Relaxation of poly-poly pitch is investigated as a layout driven performance element [5]. The improvement of the RF FoMs can be mainly attributed to mechanical strain increase due to larger volume of raised S/D SiGe for PFET devices. NFET devices show better mechanical stress transfer from the MoL stressor into the channel region due to the larger open area between the polysilicon fingers. In addition, the larger raised S/D area allows for double row contact placement and has longer Silicon-Salicide interface region, which reduces the source/drain parasitic resistance for N- and PFET simultaneously.

Single splits - #	Description	
	NFET	PFET
1	Standard Process/Layout	
2	epi option 1	
3	epi option 2	
4	Gate length reduction	
5	Poly-Poly pitch relaxation	
6	--	MoL stressor

Fig. 10. Split table of the individual elements for RF improvement

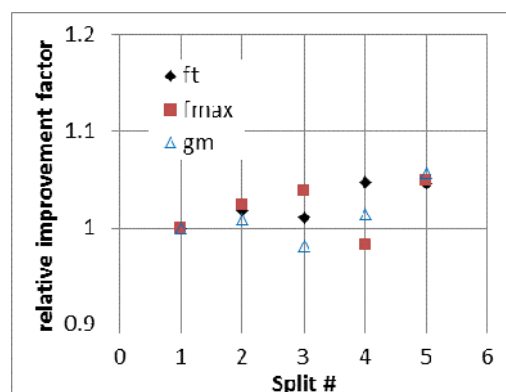


Fig. 11. Relative $f_t/f_{max}/g_m$ improvement for single elements (listed in Fig.10) for NFET device.

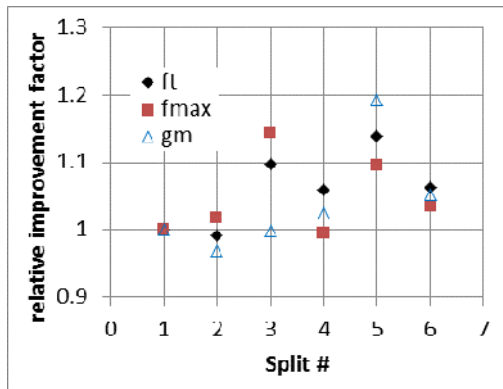


Fig. 12. Relative ft/fmax/gm improvement for single elements (listed in Fig.10) for PFET device

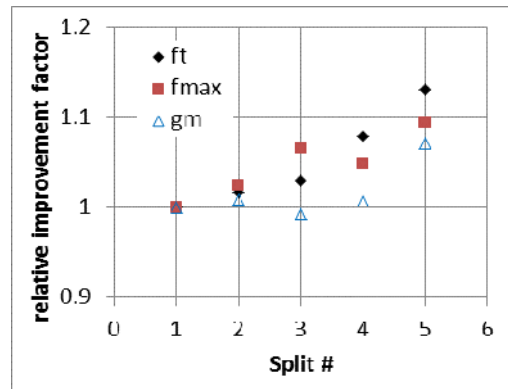


Fig. 15. Relative ft/fmax/gm improvement for NFET with the combined elements (shown in Fig.13)

B. Combined elements analysis

The step-by-step combination of the elements is described in Fig.13. The corresponding mid channel stress for NFET and PFET devices is shown in Fig. 14. Here epi option 1 acts slightly and the Poly-Poly pitch relaxation stronger on the NFET channel stress, which leads to a gm and hence also ft/fmax improvement (Fig. 15). PFET devices show similar behavior of increasing channel stress using MoL stressor and Poly-Poly pitch relaxation resulting in gm/ft/fmax improvement (Fig.16). In contrast, the gate length reduction is increasing gm and ft, but slightly reduces fmax due to higher gate resistance. As stated in III.A the epi options are mainly reducing parasitic capacitances with a minor impact on gm, but improvement of ft and fmax. Combining all elements a ft/fmax improvement of ~1.13/1.11 for NFET and ~1.32/1.24 for PFET can be achieved with respect to current process and standard layout.

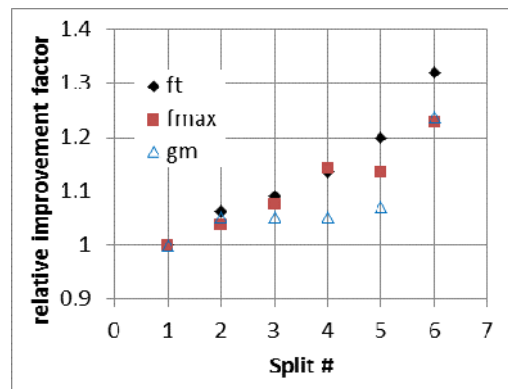


Fig. 16. Relative ft/fmax/gm improvement for PFET with the combined elements (shown in Fig.13).

Combined splits - #		Description
NFET	PFET	
1	1	Standard Process/Layout
	2	-- + MoL stressor
2	3	+ epi option 1
3	4	+ epi option 2
4	5	+ Gate length reduction
5	6	+ Poly-Poly pitch relaxation

Fig. 13. Split table of the combined elements for RF improvement

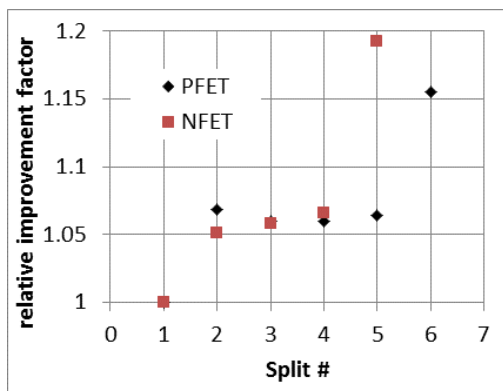


Fig. 14. Mechanical stress improvement factor of NFET and PFET device at mid channel position.

IV. CONCLUSION

The potential improvement of 22FDX® technology with regard to gm/ft/fmax could be shown by combining different process and layout elements in TCAD simulations. Based on careful process and device calibration the different individual elements have been investigated and a combination of those elements shows a ft/fmax improvement of ~1.13/1.11 for NFET and ~1.32/1.24 for PFET. Main drivers are channel mechanical stress and parasitic resistance/capacitance.

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