A Robust Simulation Method for Breakdown with Voltage Boundary Condition Utilizing Negative Time Constant Information

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***Abstract*—Dominant time constant analysis reveals that the semiconductor equations at hard breakdown turn into a positive feedback state where the convergence of steady state (DC) Newton iteration is substantially difficult even if continuation method is used. A robust simulation method for hard breakdown which detects the appearance of negative time constant during DC Newton iteration and then switches to transient (TR) simulation is proposed. The negative time constant value during the TR simulation is used for the time step restriction and the maximum time constant value is used for the determination of the final time of the TR simulation. By using the proposed method, a trace of the stable operation points in the snapback I-V trajectory corresponding to each DC bias can be obtained robustly with a simple voltage sweep at the voltage boundary.**

Keywords—hard breakdown, negative time constant, positive feedback, DC Newton iteration, continuation method, voltage boundary condition

I. Introduction

Breakdown voltage is a key design parameter for power devices, ESD protection devices and device isolations. Current capacity after the onset of breakdown is also important for ESD protection devices. To optimize the breakdown voltage, TCAD simulation is intensively used. Continuation method [1] which adopts a variable external resistance connected to a voltage boundary is usually used for the breakdown TCAD simulation because simple voltage sweep at the voltage boundary produces a convergence problem. Although the continuation method works well for variety of problems, the authors found that it sometimes suffers from the convergence problem if hard breakdown of PN junction is simulated. In this paper, the convergence problem is investigated and a robust simulation method for hard breakdown with voltage boundary condition utilizing negative time constant information is presented.

II. Problems with Conventional Breakdown Simulation Methods

The discretization scheme shown in Fig. 1 which assigns the carrier generation term by impact ionization to the downstream side of the carrier drift [2] is adopted. This scheme can avoid the instability due to the local self-feedback in a control volume under large electric field. The diode

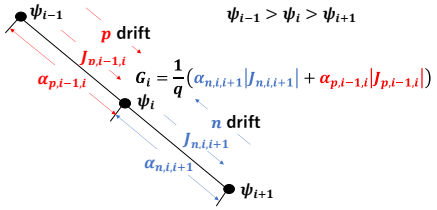

Fig. 1. Carrier generation term by impact ionization is assigned to the downstream side of the carrier drift.

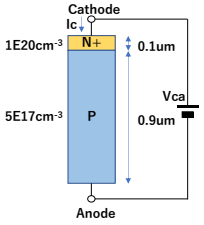

Fig. 2. Diode structure used for hard breakdown simulation.

structure used for hard breakdown simulation is shown in Fig. 2. Ic-Vca characteristics obtained by using conventional voltage sweep is shown in Fig. 3 (a). At Vca = 9.2 V, Newton iteration did not converge as shown by the blue line in Fig. 3 (b), where *dx_max* is the maximum variation of the variables at each Newton iteration. Fig. 4 shows the variation of the electrostatic potentials, the electron densities and the hole densities during the first 10 Newton iterations at Vca = 9.2 V. As shown by the thick red arrow, the carrier densities continue to decrease. This is due to the damper implemented in the program which suppresses the appearance of negative carrier density. In other words, the Newton method tries to solve the equations by introducing negative carrier density, which is an extraneous root. The grey line in Fig. 3 (b) shows the convergence behavior when another linear-search damper which tries to minimize the equation residual is used. In this case, the solution is rarely improved, which means the solution has been trapped in a local minimum. For sufficiently smooth and homeomorphic problems, even if they are highly nonlinear, Newton iteration converges if the variation of the variables is suppressed by a proper damper. [3] However, the hard breakdown simulation does not seem to be the case. To analyze the situation, 4 largest magnitude time constants of the

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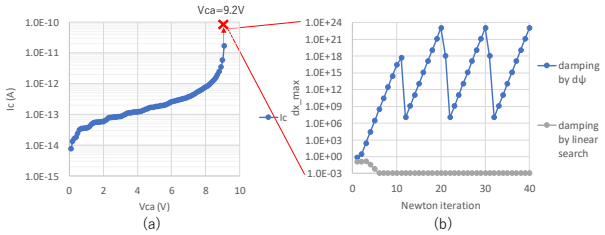

Fig. 3. (a) Ic-Vca characteristics obtained by using conventional DC voltage sweep. (b) Convergence behaavior at the non-converged bias point Vca = 9.2 V.

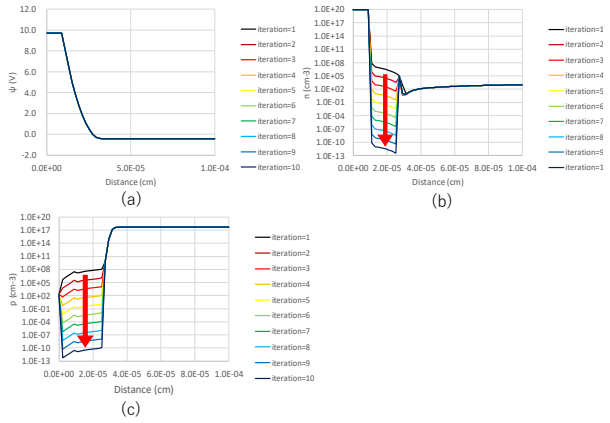

Fig. 4. Variation of (a) ψ, (b) n, and (c) p during first 10 Newton iterations at Vca = 9.2 V

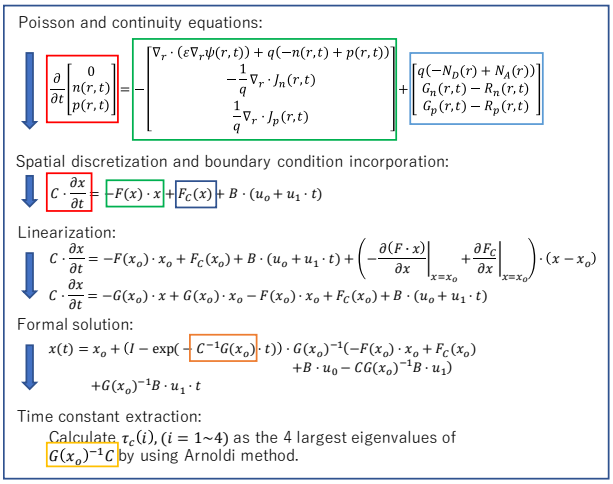

Fig. 5. Concept of time constant extraction of semiconductor device state equation.

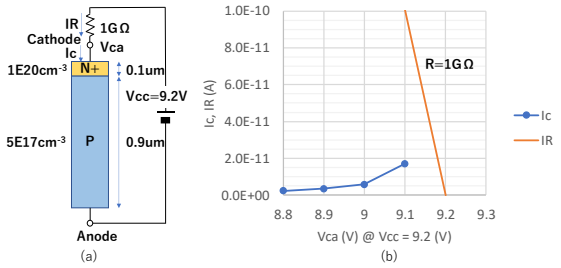

Fig. 7. (a) Diode + external resistance structure to mimic continuation method for DC breakdown simulation. (b) Diode characteristics before breakdown and 1GΩ external resistance load line.

diode structure at each Newton iteration are extracted by applying Arnoldi method to the exponential decay factor in the formal solution of the device state equation shown in Fig. 5. [4][5] Fig. 6 shows the variation of the time constants during the Newton iterations in the hard breakdown simulation. The filled squares are the time constants when the Newton iteration converges and the open circles are the negative time constants appeared during the Newton iterations. At Vca = 9.2 V, negative time constants appear at almost all iterations, which means the system is in a positive feedback state from a view point of transfer function (i.e. positive poles). This is due to the negative differential resistance induced by the increasing carrier densities by impact ionization.

To improve the convergence, 1 GΩ external resistance is connected to the cathode to mimic the continuation method as shown in Fig. 7. By adding high resistance, it is expected that the negative differential resistance would be compensated and the system would become stable. However, the convergence behaviors are quite similar to the ones in Figs. 3 and 4. Fig. 8 shows the variation of the time constants. Although the largest time constants become positive, negative time constants still remain at Vca = 9.2 V. Therefore, adding external resistance can limit the voltage variation of the cathode terminal but it cannot turn the positive feedback system into a stable one.

III. Proposed Breakdoen Simulation Method

Since the negative time constants do not disappear by connecting the external resistance, the positive feedback loop seems to be closed within the high field impact ionization region as shown in Fig. 9, where $-\tau_c > 0$ is the positive feedback loop time constant. By using TR simulation with the time step width $\Delta t < |\tau_c|$, the feedback is suppressed and stable trace of the time development is expected. Suppose that the positive feedback system with a state variable x is described by the following equation.

$$\frac{dx}{dt} = -\frac{x}{\tau_c} \tag{1}$$

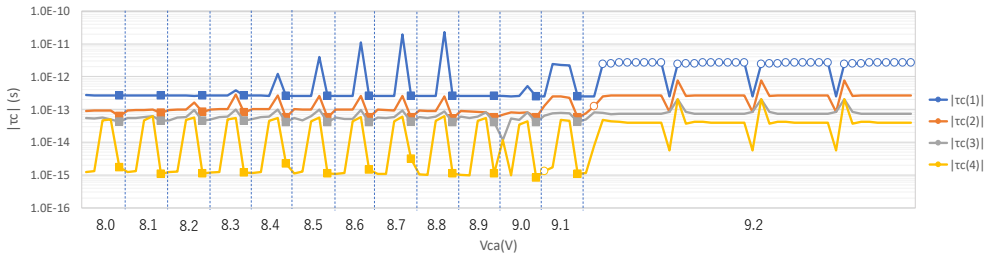

Fig. 6. Variation of time constants during Newton iteration in hard breakdown simulation.

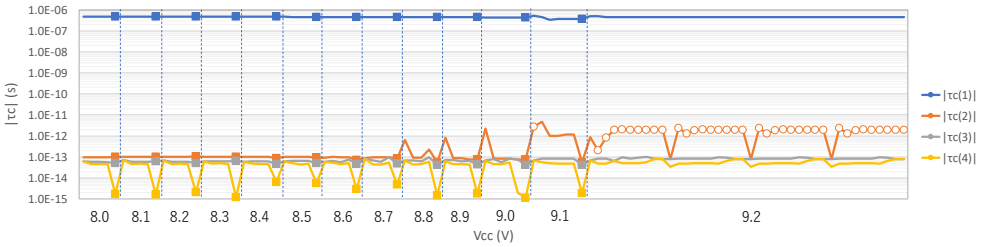

Fig. 8. Variation of the time constants during Newton iteration in DC breakdown simulation of diode + external resistance.

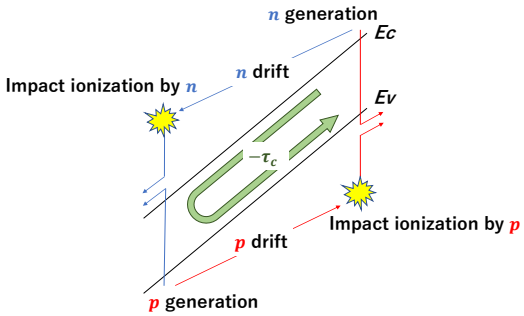

Fig. 9. Positive feedback loop closed within the high field impact ionization region. Here, $-\tau_c$ is the positive feedback loop time constant.

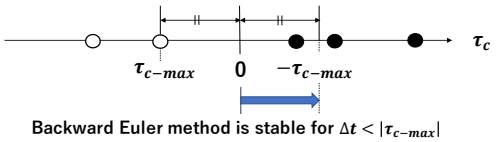

Fig. 10. Backward Euler method becomes conditionally stable if both positive (filled circle) and negative (open circle) time constants coexist.

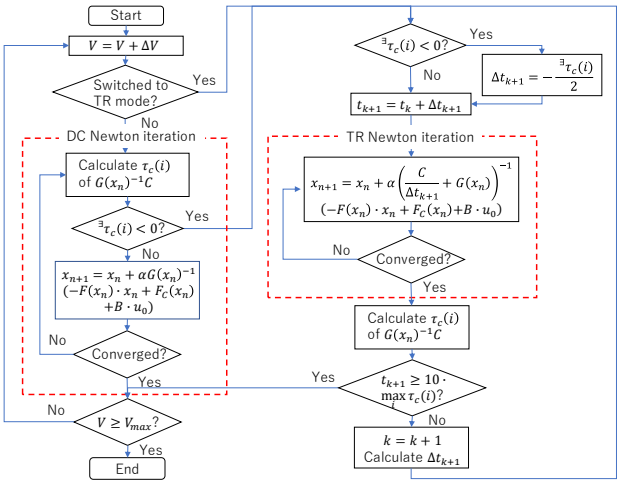

Fig. 11. Proposed breakdown simulation flow switching from DC to TR anaysis upon detecting a negative time constant.

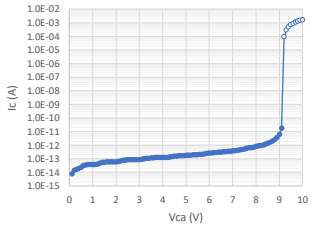

Fig. 12. Ic-Vca characteristics calculated by the proposed simulation method.

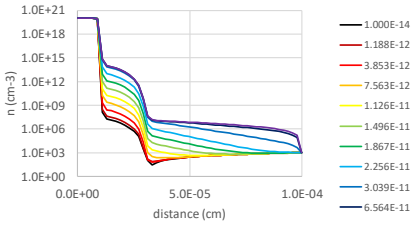

Fig. 13. Variation of electron concentration during TR simulation at Vca = 9.2 V.

By using Backward Euler method, (1) can be discretized as follows.

$$\frac{x_{k+1} - x_k}{\Delta t_{k+1}} = -\frac{x_{k+1}}{\tau_c} \tag{2}$$

where k is a time step number. By rearranging (2), the following relation is obtained.

$$x_{k+1} = \frac{\tau_c}{\Delta t_{k+1} + \tau_c} x_k \tag{3}$$

As $\tau_c < 0$ in this case, $\Delta t_{k+1} > |\tau_c|$ produces unphysical oscillatory solution with sign change. Therefore, $\Delta t_{k+1} < |\tau_{c-max}|$ where τ_{c-max} is the maximum negative time constant must be kept in Backward Euler method as shown in Fig. 10.

Since TR simulation is costly for TCAD, an algorithm shown in Fig. 11 is proposed. The algorithm switches DC simulation to TR simulation when negative time constant is detected during the DC Newton iteration. Fig. 12 shows Ic-

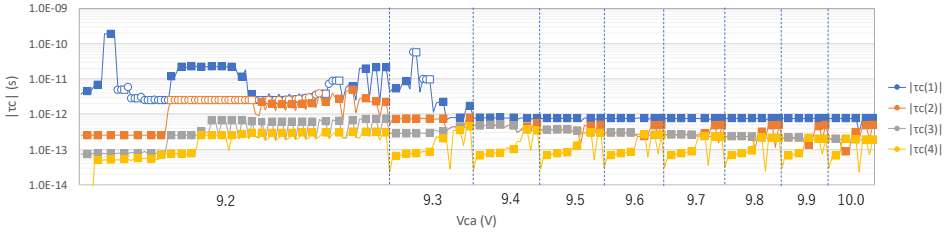

Fig. 14. Variation of the time constants at each time step during TR simulation for Vca = 9.2 – 10 V.

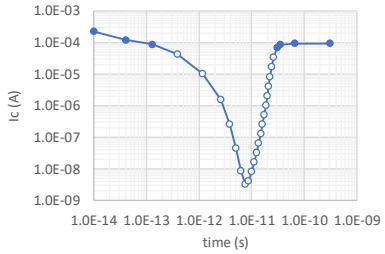

Fig. 15. Ic-t characteristic during TR simulation at Vca = 9.2 V.

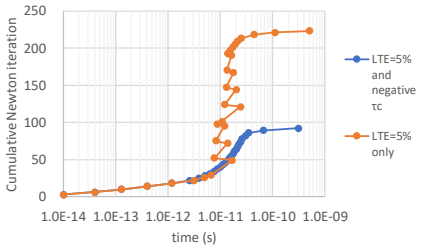

Fig. 16. Cumulative Newton iteration with / without time step limitation by negative time constant.

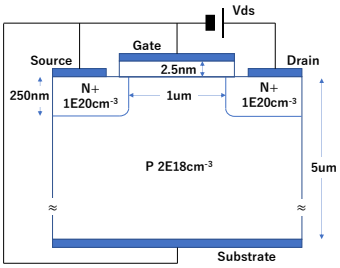

Fig. 17. GG-NMOS structure used for hard breakdown simulation.

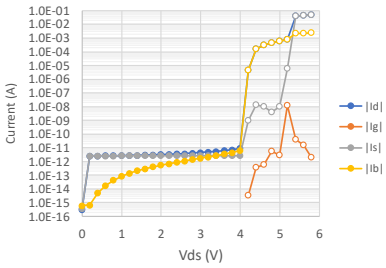

Fig. 18. Breakdown characteristics of GG-NMOS calculated by the proposed simulation method.

Vca characteristic calculated by using the algorithm. The open circles correspond to the solution by the TR simulation. Fig. 13 shows the variation of the electron density during the TR simulation at Vca = 9.2 V, where the electron density gradually increases as opposed to Fig. 4 (b). Variation of the time constants at each time step during the TR simulation for Vca = 9.2 V – 10 V is shown in Fig. 14, where the filled squares mean the positive cones and the open squares mean the negative ones. There are a lot of negative time constants at Vcs = 9.2 V and a few at Vca = 9.3 V. Since there is no negative time constant after Vca = 9.4 V, convergence may be obtained by using the conventional dampers in DC simulation. This stabilization comes from the increased Shockley-Red-Hall recombination. Ic-t characteristics during the TR simulation at Vca = 9.2 V is shown in Fig. 15, where the open circles stand for the time steps with negative time constants. The final time of the TR simulation is determined as 10 times of the largest magnitude time constant. Fig. 16 shows the cumulative Newton iteration when only Local Truncation Error (LTE) = 5 % is applied to the time step control (orange) [4][5] and when the time step width is limited to the half of the negative time constant magnitude in addition to LTE = 5 % (blue). In the case of LTE = 5 % only, a lot of retries occur due to non-convergence since the carrier density generated by impact ionization is still too small to affect the LTE. Therefore, it is very important to limit the time steps by taking the negative time constant information into account. The most CPU-time consuming part in TCAD is LU-factorization of Jacobian matrix. Since the time constant calculation in Arnoldi method in Fig. 5 uses the same Jacobian $G(x_n)$ as that of Newton iteration in Fig. 11, CPU-time overhead is small for the negative time constant detection in the DC simulation. On the other hand, in the TR simulation, as the Jacobian is $C/\Delta t_{k+1} + G(x_n)$, an extra LU-factorization is required for the time constant calculation. This cost is almost equivalent to one more extra Newton iteration at each time step [5] as shown in Fig. 11.

Fig. 17 shows a Grounded Gate (GG) NMOS structure which mimics an ESD protection device. The breakdown simulation results are shown in Fig. 18, where the filled circles are with the original DC simulation and open circles are with the switched TR simulation. Hard breakdown of the drain-substrate junction occurs at Vds = 4.2 V and the second abrupt drain current increase due to parasitic bipolar effect occurs at Vds = 5.4 V. Since the simulation is performed with voltage boundary condition, no snapback I-V curve is obtained here. However, without using the continuation method, a trace of the stable operating points in the snapback I-V trajectory corresponding to each DC bias can be obtained robustly with a simple voltage sweep at the voltage boundary.

IV. Conclusion

A robust simulation method for hard breakdown is proposed. It detects the appearance of negative time constant during DC Newton iteration and then switches to TR simulation. The negative time constant value during the TR simulation is used for the time step restriction and the maximum time constant value is used for the determination of the final time of the TR simulation. By using the proposed method, a trace of the stable operating points in the snapback I-V trajectory corresponding to each DC bias can be obtained robustly with a simple voltage sweep at the voltage boundary.

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