Relationship between capacitance and conductance in MOS capacitors

E. Caruso*, J. Lin*, S. Monaghan*, K. Cherkaoui*, L. Floyd*, F. Gity*, P. Palestri¥, D. Esseni¥, L. Selmi#, P. K. Hurley*

*Tyndall National Institute, University College Cork, Cork, Ireland
¥ DPIA, University of Udine, Via delle Scienze 206, 33100, Udine, Italy
DIEF, University of Modena and Reggio Emilia, Via P. Vivarelli 10/1, 41125, Modena, Italy

***Abstract*—In this work, we describe how the frequency dependence of conductance (G) and capacitance (C) of a generic MOS capacitor results in peaks of the functions G/ω and -ωdC/dω. By means of TCAD simulations, we show that G/ω and -ωdC/dω peak at the same value and at the same frequency for every bias point from accumulation to inversion. We illustrate how the properties of the peaks change with the semiconductor doping (N_D), oxide capacitance (C_{OX}), minority carrier lifetime (τ_g), interface defect parameters (N_{IT}, σ) and majority carrier dielectric relaxation time (τ_r). Finally, we demonstrate how these insights on G/ω and -ωdC/dω can be used to extract C_{OX}, N_D and τ_g from InGaAs MOSCAP measurements**

Keywords—Characterization, extraction technique, MOS, multi-frequency, C-V, G-V, minority carrier lifetime, oxide capacitance, doping

I. INTRODUCTION

Measuring and analyzing the impedance of the metal-oxide-semiconductor (MOS) system has played a central role in the development of MOS structures in electronic, photovoltaic and photocatalytic devices. The impedance/ admittance modulus (Z, Y) and phase angle (θ) of the MOS capacitor are typically measured over the frequency range from 20 Hz to 1 MHz, and resolved into capacitive (C) and conductive (G) elements. The behavior of C and G as a function of gate voltage, temperature and frequency are used to investigate and quantify physical parameters and defects of the MOS system [1].

It was recently shown using experimental results, simulations and mathematical analysis, that for any MOS capacitor in inversion, functions of the capacitance (-ωdC/dω) and conductance (G/ω) are related at all angular frequencies (ω=2πf) and that the two functions both exhibit a maximum value at the transition frequency (f_m). In addition, the values of G/ω and -ωdC/dω are equal at f_m [2].

The objective of this work is to extend on [2], to show that the functions G/ω and -ωdC/dω are related in all bias regions of the MOS C-V response and that this holds for ideal MOS systems and for non-ideal MOS structures with interface traps.

II. THE G/ω AND - ω dC/dω RELATIONSHIP: VALIDATION

To demonstrate the relationship between the C and G parameters, we consider the case of an InGaAs MOS capacitor (53% In). It is important to emphasize that the relationship is expected to hold for all MOS structures. InGaAs was selected as an example MOS system for the following reasons: (a) based on the energy gap (E_g=0.74 eV) and typical τ_g values, InGaAs MOS capacitors can exhibit an inversion response at room temperature [3], (b) MOS systems based on wider band gap semiconductors, (e.g., Si, GaN), and typical values t_g, exhibit peak frequency values (f_m) in inversion which are typically below 1 mHz, making difficult the measurements, (c) the C and G functions also have coincident peaks in the GHz regime, of relevance to RF and mm wave applications, where In(Ga)As devices are often employed [4].

Figure 1(a) and 1(b) report the multi-frequency C-V and G-V responses (1 kHz to 1 MHz) of an $In_{0.53}Ga_{0.47}As$ MOS capacitor simulated with Sentaurus device simulator [5], including Fermi-Dirac statistics, multi-valley band structure with non-parabolic corrections and Shockley–Read–Hall (SRH) generation/recombination. Figure 2 plots G/ω and -ωdC/dω in inversion (V_G=-3V) from 10^2 to 10^{14} Hz. The plot confirms that the two functions feature the same value at f = 2285 Hz, as described in [2], where the peak frequency is determined by the SRH time τ_g. The plot also shows that the two functions exhibit a second peak value at f = 8.53 THz. Figure 3 plots the magnitude of the peak values of G/ω and -ωdC/dω as the gate bias is varied. The plot demonstrates how the relationship holds at all bias points in the ideal CV/GV response.

Figure 4 shows how the two peak frequencies vary with the gate voltage. The high frequency peak is always present and relates to the majority carrier dielectric relation time, which is discussed later. The peak due to the supply of minority carriers to the inversion layer goes to zero, as expected, when the MOS structure moves from strong inversion to depletion. This is a general relationship and holds for any MOS system.

We next consider if the G/ω and -ωdC/dω relationships still hold for the non-ideal case, namely in the presence of interface states. Figure 5 illustrates an example for a Gaussian D_{IT} profile, described by the equation $D_{IT}(E) = N_{IT}\exp\left(-(E-E_{IT})^2/\left(2S_{IT}{}^2\right)\right)$. The traps are donor type, as proposed in previous publications [e.g., [6]]. This profile is introduced into the ideal InGaAs MOS structure considered in Figs. 1. The D_{IT} introduces a frequency dependent distortion into the CV and GV response, as reported in other publications [e.g., [6]]. Plotting the G/ω and -ωdC/dω peak values versus gate voltage (Figure 6(a)) and the frequency of the peak value versus bias (Figure 6(b)), indicates that the relationship still holds for interface states. The high frequency peaks (> 10^{12} Hz) are not influenced by interface states, as expected, and are removed for clarity.

The physical meaning of the peak values of G/ω and -ωdC/dω is illustrated in Figures. 7 to 10. Figure 7 shows that the peak frequency in inversion is directly related to $1/\tau_g$. At high values of the minority carrier lifetime, f_m eventually saturates, when the inversion layer carrier supply rate from minority carrier density in quasi neutral region (n_i^2/N_D) exceeds the SRH generation rate. In depletion region, where interface traps dominates the response, the peak value of G/ω linearly depends on N_{IT} (the peak value of D_{IT}) for G/ω<C_{OX}/2 (see Figure 8), and this is a well known result from the conductance method approach [1][7]. The peak frequency shows a linear dependence on the capture cross section (Figure 9). In accumulation, the high frequency peak is set by the majority carrier dielectric relaxation time (Figure 10)

978-1-7281-0940-4/19/$31.00 ©2019 IEEE

$\tau_r=\varepsilon_0 \cdot \varepsilon_r \cdot \rho$, with ε_0, ε_r and ρ being the free space permittivity and the semiconductor relative permittivity and resistivity [8].

The measured/simulated admittance is resolved in the equivalent circuit shown in Figure 11(c). This circuit representation in addition to the equivalent circuit topology of the device under test (Fig 11(b)) set the relationship between G/ω and $-\omega dC/d\omega$. By first writing C and G in terms of C_{OX}, G_S, C_S, and then by calculating the corresponding maximum/minimum, it is also possible to obtain analytic expressions for the peak value and position of the G/ω and $-\omega dC/d\omega$ functions:

$$f_m = \frac{G_S}{2\pi(C_S+C_{OX})} \quad (1.a)$$

$$\left(\frac{G}{\omega}\right)_{max} = \left(-\omega \frac{dC}{d\omega}\right)_{max} = \frac{C_{OX}^2}{2(C_S+C_{OX})} \quad (1.b)$$

where G_S and C_S are the conductance and capacitance of the semiconductor respectively. It is worth noting that at every bias point the semiconductor impedance can be modeled using a capacitor and a conductance, also in the presence of interface traps. The only assumption made in the topology reported in Figure 11(b) is that the oxide is free of traps. In fact, in the presence of border traps an R-C distributed network should be added in the circuit, as reported in [9].

III. The G/ ω and -ω dC/ dω relationship: application

By performing a direct comparison between G/ω and $-\omega dC/d\omega$ from simulations and experimental results, MOS parameters can be extracted. An example is shown in Figure 11(a) based on experimental multi-frequency C-V and G-V measured from 1 kHz to 1 MHz for a $Ni/Al_2O_3/n\text{-}In_{0.53}Ga_{0.47}As/InP$ structure [10]. The only region that can be analyzed is inversion, where the frequency peak of G/ω and $-\omega dC/d\omega$ is within the measured frequency range (Figure 4).
For non-silicon based MOS systems, defects in the oxide (border traps) can have a significant impact on the MOS/MOSFET characteristics [11][12]. However, in strong inversion the behavior of C and G is mainly given by the minority carriers response, so it is reasonable to neglect the effect of the border traps and to use the topology shown in Figure 11(b) also in this case.
Using C_{OX}=0.098 F/m^2, τ_g= 80 ps and N_D=4.6·10^{17} cm^{-3} we obtain an excellent agreement between simulations and experiments (Fig 11(a)). The extracted parameters are consistent with other extraction techniques [10]. In particular, N_D agrees with the mean value of the doping concentration extracted by ECV, while C_{OX} is compatible with the oxide thickness measured by TEM images (6 nm) and assuming a Al_2O_3 dielectric constant of 6.6, which is consistent with other experiments [13].

IV. Conclusions

Simulations have shown that the G/ω and $-\omega dC/d\omega$ versus frequency plots exhibit marked peaks. The value and the frequency of the peaks can be interpreted with the circuit elements of Figure 11(b) and thus eventually in terms of C_{OX}, N_D, τ_g, τ_r , D_{IT} and σ. In strong inversion, where the effect of border traps can be neglected for this analysis, it is possible to do a direct comparison of the G/ω and $-\omega dC/d\omega$ functions between experimental and simulated results (without traps). The triplet (C_{OX}, N_D, τ_g) that minimizes the error between these functions identifies the extracted quantities. This technique is completely general and applicable to any MOS capacitor system, the information that can be extracted from the experiments depends however on the frequency range that canbe practically explored.

Acknowledgment

The research leading to these results has received funding from the European Commission H2020 INSIGHT project No 688784 and Science Foundation Ireland (15/IA/3131).

References

[1] E. H. Nicollian and John R. Brews*, MOS Physics and Technology,* Wiley, 2002

[2] S. Monaghan, É. O'Connor, R. Rios, F. Ferdousi, L. Floyd, E. Ryan, K. Cherkaoui, I. M. Povey, K. J. Kuhn and P. K. Hurley, "Capacitance and Conductance for an MOS System in Inversion, with Oxide Capacitance and Minority Carrier Lifetime Extractions," in IEEE Transactions on Electron Devices, vol. 61, no. 12, pp. 4176-4185, 2014.

[3] É. O'Connor, K. Cherkaoui, S. Monaghan, B. Sheehan, I. M. Poey and P. K. Hurley "Inversion in the $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor system: Impact of the $In_{0.53}Ga_{0.47}As$ doping concentration", Applied Physics Letters, vol. 110, no. 3, 032902, 2017

[4] O. Kilpi, J. Svensson and L. Wernersson, "Sub-100-nm gate-length scaling of vertical InAs/InGaAs nanowire MOSFETs on Si," Conf. Proc IEDM, pp. 17.3.1-17.3.4, 2017

[5] *Sentaurus Device Manual L-2016.03-SP2*, Synopsys Inc., 2016

[6] G. Brammertz, A. Alian, D. H. Lin, M. Meuris, M. Caymax and W. -. Wang, "A Combined Interface and Border Trap Model for High-Mobility Substrate Metal–Oxide–Semiconductor Devices Applied to $In_{0.53}Ga_{0.47}As$ and InP Capacitors," in IEEE Transactions on Electron Devices, vol. 58, no. 11, pp. 3890-3897, 2011.

[7] K. Martens, G. Brammertz, B. De Jaeger,D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, "On the Correct Extraction of Interface Trap Density of MOS Devices With High-Mobility Semiconductor Substrates," in IEEE Transactions on Electron Devices, vol. 55, no. 2, pp. 547-556, Feb. 2008

[8] T. Ohmi, M. Tsubota, T. Tsuneto, "Relaxation of Brinkman-Smith Mode in Superfluid 3He–B between Parallel Plates." Japanese Journal of Applied Physics vol. 26, no. S3-1, p. 169, 1987

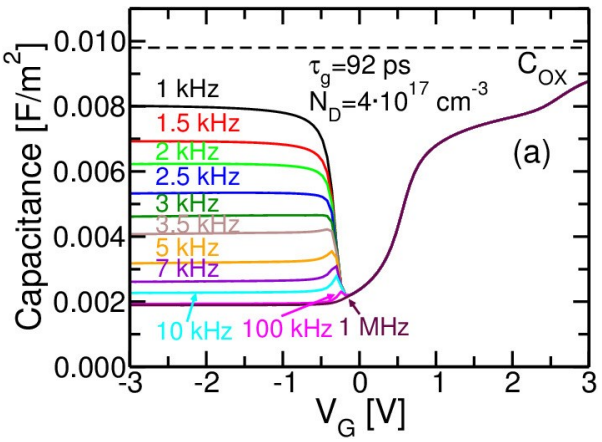
[9] Y. Yuan, B. Yu, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell and Y. Taur, "A Distributed Bulk-Oxide Trap Model for Al_2O_3 InGaAs MOS Devices," in IEEE Transactions on Electron Devices, vol. 59, no. 8, pp. 2100-2106, 2012.

[10] E. Caruso, J. Lin, K. F. Burke, K. Cherkaoui, D. Esseni, F. Gity, S. Monaghan, P. Palestri, P. Hurley and L. Selmi, "Profiling border-traps by TCAD analysis of multifrequency CV-curves in Al_2O_3/InGaAs stacks," Conf. Proc. EUROSOI-ULIS, pp. 1-4, 2018

[11] J. Lin, Y. Y. Gomeniuk, S. Monaghan, I. M. Povey, K. Cherkaoui, E. O'Connor and P. K. Hurley, "An investigation of capacitance-voltage hysteresis in metal/high-k/ $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors", Journal of Applied Physics, vol. 114, no 14, p. 144105, 2013

[12] S. Johansson, M. Berg, K. Persson and E. Lind, "A High-Frequency Transconductance Method for Characterization of High-κ Border Traps in III-V MOSFETs," in IEEE Transactions on Electron Devices, vol. 60, no. 2, pp. 776-781, 2013

[13] R. Y. Khosa, E. B Thorsteinsson, M. Winters, N. Rorsman, R. Karhu, J. Hassan, and E. Ö. Sveinbjörnsson, "Electrical characterization of amorphous Al2O3 dielectric films on n-type 4H-SiC". AIP Advances, vol. 8, no. 2,p. 025304, 2018



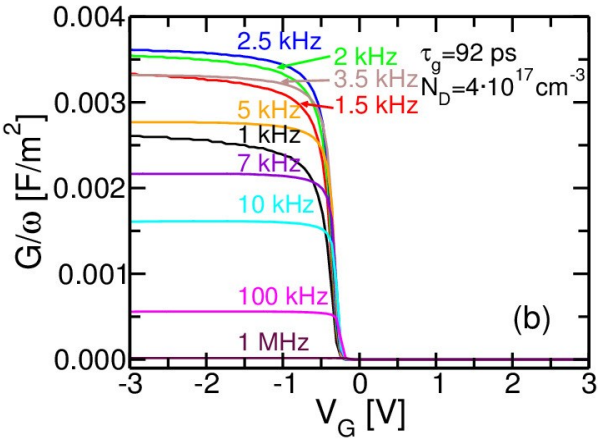


Figure 1. Simulated multi-frequency C-V (a) and G/ω -V (b) at 300 K w/o including traps. Simulations use N_D=4·10^{17} cm^{-3}, C_{OX}=0.0098 F/m^2 and τ_g= 92 ps.

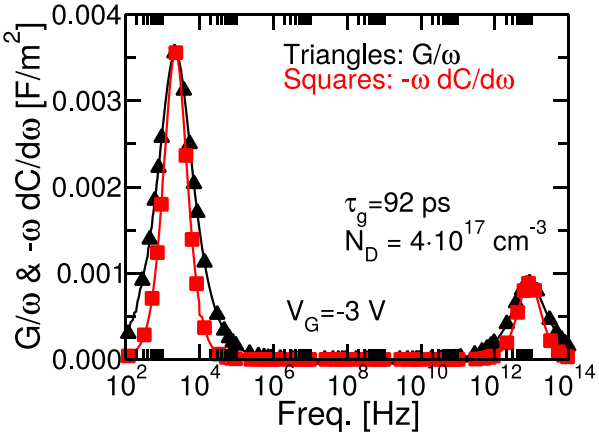


Figure 2. Simulated curves of G/ω (triangles) and -ω·dC/dω (squares) extracted from the MOS structure in Figure 1 and plotted as a function of frequency in inversion (V_G=-3 V).

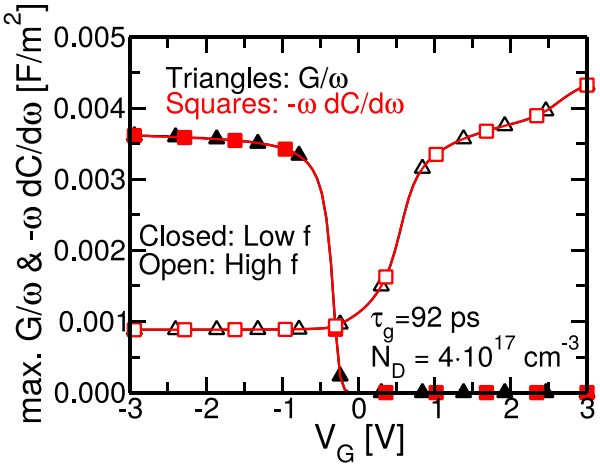


Figure 3. Peak value of G/ω (triangles) and -ω·dC/dω (squares) as a function of V_G for the simulations in Figure1

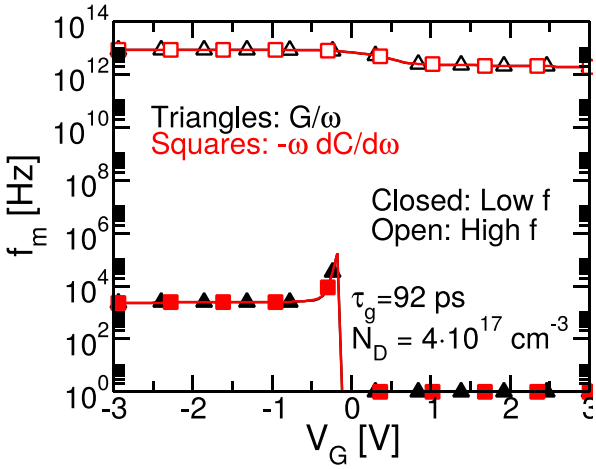


Figure 4. Frequency position of the peak value of G/ω (triangles) and -ω·dC/dω (squares) as a function of V_G for the simulations in Figure1.

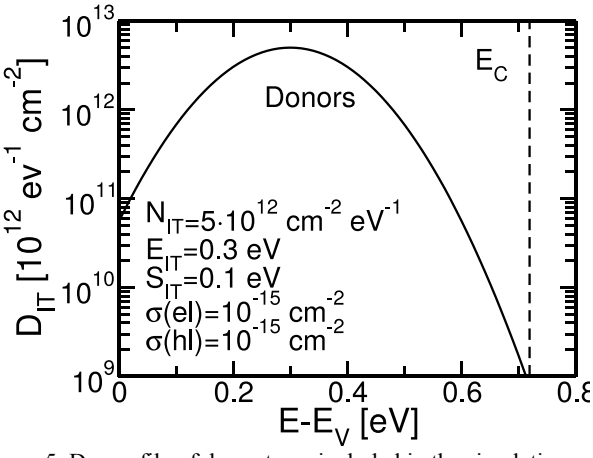


Figure 5. D_{IT} profile of donor traps included in the simulations of Figure 6. The energy is referred to the valence band of InGaAs. The figure reports also the parameter used for the Gaussian distribution and the values of the capture cross section for electron and holes.

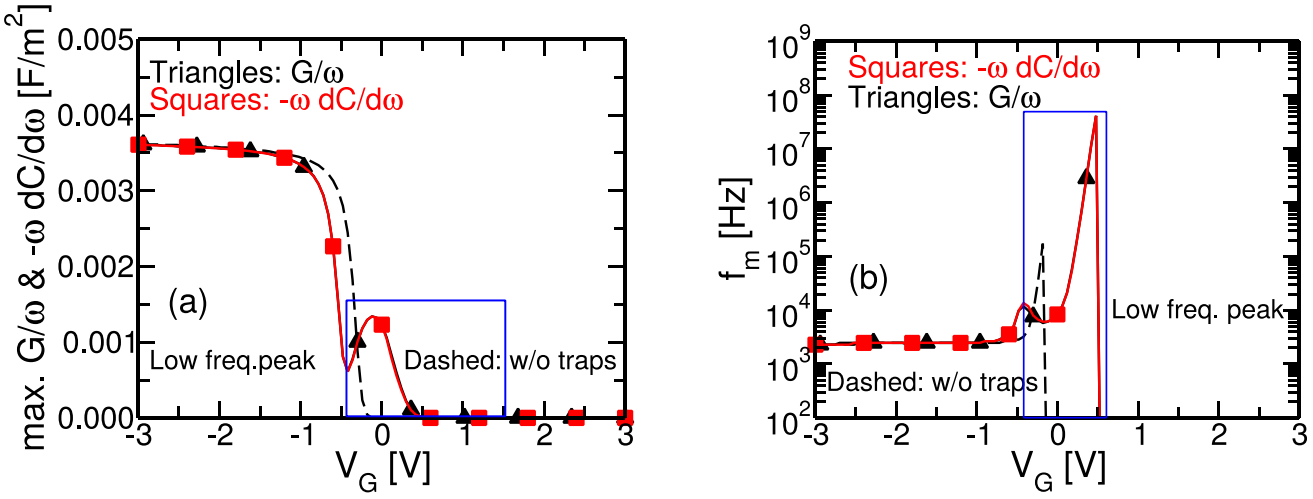


Figure 6. Simulations of the MOS structure in Figs. 1 including the Gaussian D_{IT} profile shown in Figure 5. The peak value of G/ω and -ω·dC/dω versus V_G is shown in (a) and its frequency position in (b). The dashed lines are the simulations results without traps and the blue box highlights the region where the D_{IT} affects the properties of the peaks. The high frequency peaks (> 10^{12} Hz) are not impacted by D_{IT}, as expected, and are removed for clarity.

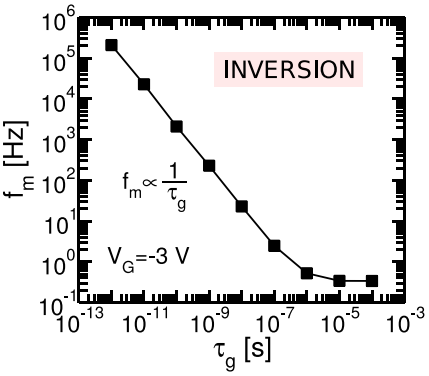


Figure. 7. Simulated f_m as a function of the minority carrier life time extracted from the MOS structure in Figure 1.

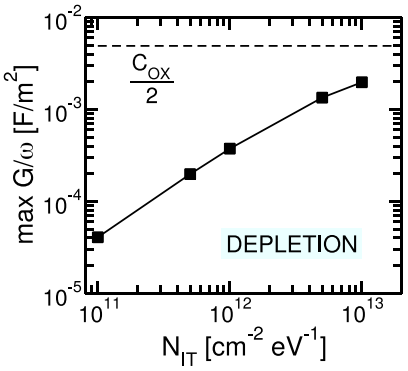


Figure. 8. Simulated maximum value of G/ω as a function of N_{IT} for the MOS structure in Figure 6. All the other parameter of D_{IT} are the ones reported in Figure 5. For high values of N_{IT}, the function tends to $C_{OX}/2$, which is shown with the dashed line.

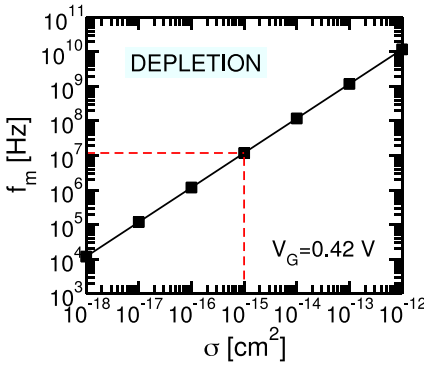


Figure 9. Simulated f_m associated to traps response of the D_{IT} in Figure 5 as a function of the capture cross section. Note that for $\sigma=1\cdot10^{-15}$ cm^2, f_m is ~ 10 MHz, which is outside the typical measurement range (up to 1 MHz).

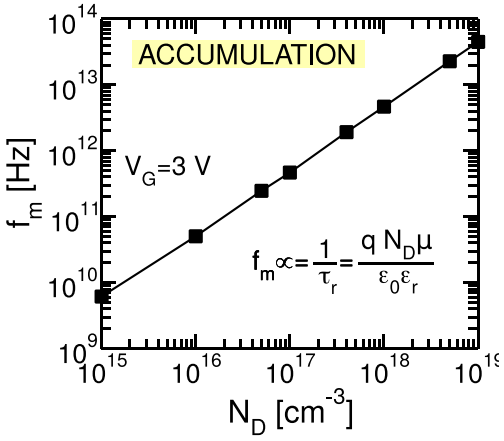


Figure 10. Simulated f_m of the majority carriers as a function of N_D from the MOS structure in Figure 1 (relevant for *mm* wave devices).

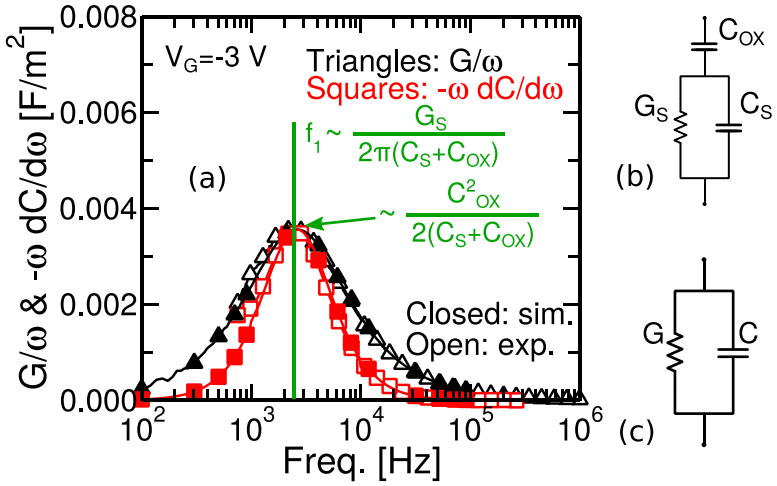


Figure. 11. (a) Simulated (closed) and experimental (open) curves at V_G= -3 V of G/ω (triangles) and -ω·dC/dω (squares) plotted as a function of frequency. (b) Equivalent electrical circuit of a MOS structure interpreted using a parallel G-C circuit (c).