Progress in dislocation stress field model and its appications

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***Abstract*— TCAD prediction of the stress field generated by dislocation is crucial for the optimization of stressors for next generation logic devices. In this paper, we present a new hybrid approach for dislocation stress field calculation and its application to strained Si devices. New methodology combines an analytic stress field model for dislocation cores and consecutive FEM stress solving to get mechanical equilibrium. It was applied to the design optimization of dislocation stress memorization technique (D-SMT), its local layout effect (LLE) modeling, and the relaxation of lattice mismatch strain at Si/SiGe interface which degrades eSiGe stress. All the simulation results were verified with experimental results.**

Keywords—dislocation, stress memorization technique, SMT, strained silicon, stress engineering, Peierls-Nabarro model

I. INTRODUCTION

Strained Si technology itself is a rather old topic in the history of semiconductor technology, which traces back to the early studies of deformation potential [1] and piezo-resistivity [2]. However, it caught the attention of semiconductor industry after the first commercialization of strained Si device by Intel in 2002. Since then, many stressors have been proposed and introduced in logic technology; tensile contact etch stopper layer (CESL) for NMOS and embedded SiGe (eSiGe) for PMOS in 90nm node, poly-Si stress memorization technique (SMT) for NMOS in 65nm node, tensile trench contact (TTC) for NMOS and sigma eSiGe for PMOS in 45nm, dislocation SMT (D-SMT) for NMOS in 32nm. Even in the era of FinFET beyond 22nm, stressors like eSiGe & stress-relaxed buffer (SRB) are still playing an important role as a performance booster. All these stressors can be categorized into 6 types depending on its deformation mechanism, which are listed in Table.1. All the stressors except high dimensional defect can be solved numerically in conventional TCAD framework only if we apply proper initial stress, mechanical properties & boundary condition. However, high dimensional defects like dislocation (1D defect), stacking fault/twin boundary (2D defect), and grain boundary (3D defect), are still difficult to simulate in conventional TCAD framework due to its phenomenological complexity.

Table 1 Categorization of stressors

Deformation mechanism		Examples
Elastic	Residual film stress	CESL
	Lattice mismatch stress	SiGe/SiC
	Thermal inclusion stress	TTC, TSV
Inelastic	Volume change by shrinkage / phase change	Oxide, Silicide
	Plastic deformation (yield)	SMT
	High dimensional defect	D-SMT, SRB

In Poly-Si/SiON (PSiON) gate first process used until 45~32nm planar transistor, SMT was a major stressor for NMOS, whose main effect comes from the plastic strain memorized within poly Si gate. However, in HK/MG gate last process introduced beyond 45~32nm, PSiON gate stack is replaced by HK/MG stack, which means the plastic strain memorized within Poly-Si gate disappears. To overcome this limitation, a new SMT process is proposed [3], which forms high dimensional defects within S/D region, what we call dislocation SMT (D-SMT). It deploys the mechanical stress exerted by the stacking fault generated during solid phase epitaxial regrowth (SPER) in SMT annealing step as shown in Fig.1.

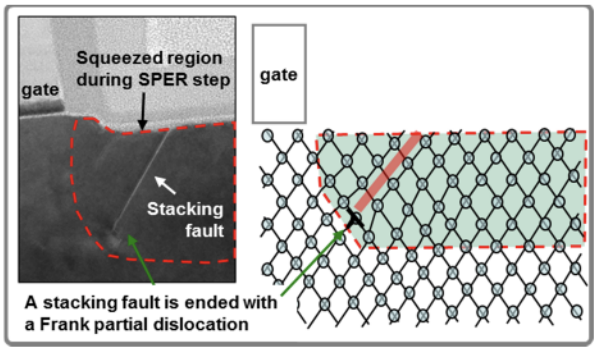


Fig. 1 A schematic illustration of the stacking fault generated during SPER.

Many researchers reported their experimental and modeling results [4] [5] describing the generation mechanism of stacking faults during SPER in SMT process. To estimate the channel stress enhancement by D-SMT, we should calculate the misfit strain exerted by a stacking fault, which means the conventional plastic strain model [6] is no more valid. To calculate the misfit strain exerted by a stacking fault rigorously, we needs a sophisticated ab-initio calculation [7] requiring very high computing power. However, the problem becomes extremely simply, if we assume the misfit strain of a stacking fault mostly comes from the partial dislocations forming the boundary of stacking fault. In fact, the strain field of stacking fault itself is negligible compared to that of surrounding partial dislocations. The equilibrium between the strain energy by surrounding partial dislocations and the stacking fault energy determines the area of stacking fault. So the simplest but effective way to estimate the stress field by stacking fault is to calculate the stress field from its surrounding partial dislocations. Dislocation also plays an important role in stress relaxation at the interface where lattice mismatch stress is applied. There are many types of relaxation by dislocations working in strained Si technology; misfit dislocations in Si/SiGe interface, threading dislocations in stress relaxed buffer (SRB). So many researchers analyzed

978-1-7281-0940-4/19/$31.00 © 2019 IEEE

dislocation problems in inhomogeneous media and the behavior of dislocations near material interface boundary.

Up to now, three different approaches have been made to calculate the stress field generated by dislocation core. The first is based on analytic approach represented by venerable Peierls–Nabarro model [8][9] inspired by Eshelby's inclusion problems [10]. The second is based on slab insertion type finite element method (FEM) [11], which requires very careful mesh handling at dislocation core to avoid the numerical instability at the singularity point. The third is a direct atomistic simulation, which is considerably more accurate but computationally expensive [12] [13]. Since the first application of analytic approach based on P-N model to the logic gate last devices [14], the flaw of analytic approach compared to FEM approach is pointed out by some group [15] ; i.e. the interaction between dislocation and material interfaces & free surface. A new approach remedying the drawback of conventional analytic approach is proposed in this paper.

II. Simulation Methodology

To overcome the shortcomings of conventional analytic approach when the dislocation is located at near free surface or hetero-interfaces, we solved mechanical equilibrium with appropriate boundary conditions after setting displacement field based on analytic dislocation field model. The overall calculation flow is as shown in Fig.2.

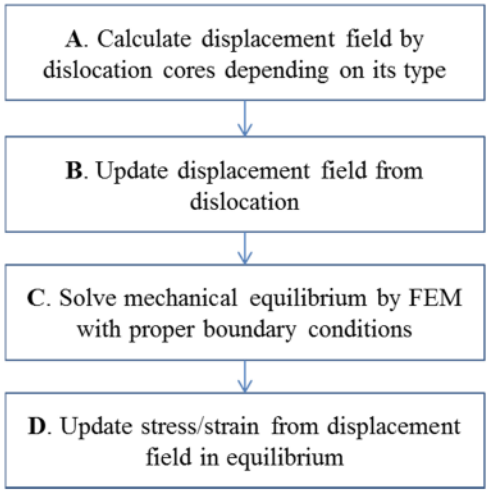


Fig. 2 Schematics chart of simulation flow

A. Calculate displacement vector $\{u^{disl}\}$ by a dislocation core depending on dislocation type;

(For edge dislocation)

$$u_1 = \frac{-b}{2\pi}\left[\tan^{-1}\left(\frac{x_2}{x_1}\right)+\frac{1}{2(1-\nu)}\frac{x_1x_2}{(x_1^2+x_2^2)}\right] \quad (1)$$

$$u_2 = \frac{b}{8\pi(1-\nu)}\left[(1-2\nu)\ln(x_1^2+x_2^2)+\frac{(x_1^2-x_2^2)}{(x_1^2+x_2^2)}\right]$$

$$u_3 = 0$$

(For screw dislocation)

$$u_1 = u_2 = 0$$

$$u_3 = \frac{b}{2\pi}\tan^{-1}(x_2/x_1) \quad (2)$$

Where ν is Poisson ratio and ***b*** is Burgers vector, which depends on dislocation types as below;

Dislocation Types	Burgers Vector
Perfect dislocation	$a_0/2$ [110]
Shockley partial	$a_0/6$ [112]
Frank partial	$a_0/3$ [111]

B. Update displacement field from multiple dislocations;

$$\{u\} = \{u^0\}+\Sigma\{u^{disl}\} \quad (3)$$

where $\{u^0\}$ is a displacement field vector from previous step by other stress sources like residual film stress, lattice match stress, thermal stress, and so on.

C. Solve FEM to get mechanical equilibrium;

Solve FEM to get displacement field $\{u\}$ in mechanical equilibrium with appropriate boundary conditions for hetro-interfaces within simulation domain

$$\boldsymbol{K}\{u\}=\{F\} \quad (4)$$

where ***K*** is a stiffness matrix, $\{F\}$ is a load vector.

D. Update strain and stress field

Update strain and stress field from the updated displacement field after equilibrium solving

$$\{\varepsilon\}=\boldsymbol{B}\{u\}\,,\ \{\sigma\}=\boldsymbol{E}\{\varepsilon\} \quad (5)$$

where ***B*** is a matrix differential operator, ***E*** is elasticity matrix.

III. Application Results and Discussion

New dislocation field model is implemented into our in-house process simulator and tested for various cases to show an improvement over conventional analytic / FEM approaches. And also, all the simulation results were verified with experimental results.

A. An improvement over coventional analytic approach

In conventional analytic approach, the stress field from analytic formulation, what we call P-N model, is just mapped on the whole node point of Si region as shown in Fig.3.

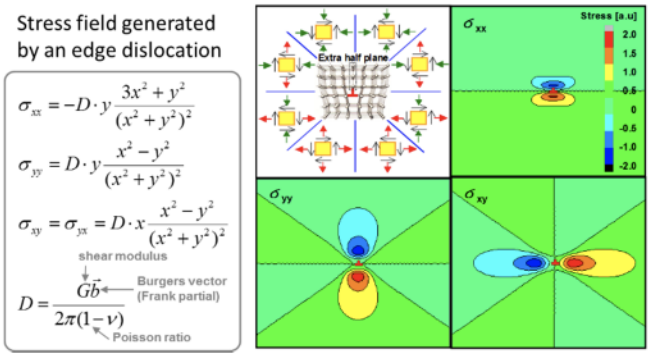


Fig. 3 Dislocation stress field mapping technique used in conventional analytic approach

This causes two drawbacks; Firstly, it cannot consider the stress relaxation at the surface or at the interface with softer material, which is the main drawback of analytic approach

compared to FEM approach. Secondly, it is hard to combine with other consecutive stressors solving mechanical equilibrium with FEM, which has to manage historic displacement information for stress history calculation.

An increase of ~0.2% strain in the channel is observed when we remove the poly-Si gate in gate last process, which was successfully reproduced by new approach as shown in Fig.4. The stress contours by hybrid approach match well the corresponding FEM cases when the dislocation core comes close to the surfaces, which is verifying the new hybrid approach.

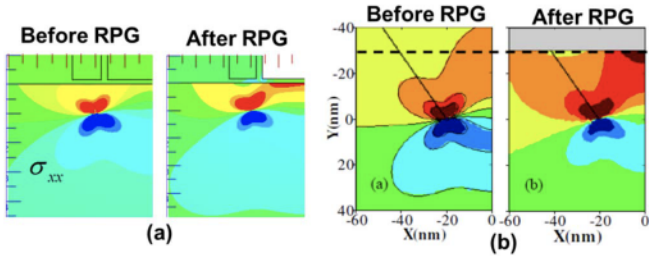
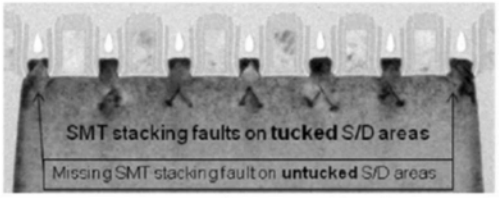


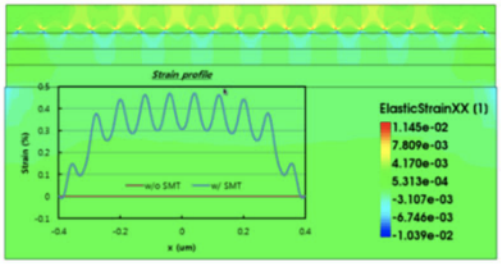
Fig. 4 Free surface effect in D-SMT for NMOS when dummy poly-Si gate is removed with (a) new hybrid approach and (b) a slab-insertion FEM approach [15].

B. An improvement over coventional FEM approach

Conventional FEM approach, whose concept is to remove an atom plane from perfect crystal lattice and to map displacement vector across the missing atom plane (slab), has several drawbacks; Firstly, it is a matter of cause that you have to get over the numerical instability at the singularity point of dislocation core through mesh refinement. Secondly, it requires extra geometry handling because you have to define the slab region (extra half plane) manually. The difficulty increases exponentially when you try to consider the nested dislocation stress field from multiple dislocation cores to estimate the impact of length of diffusion (LOD) or contacted poly pitch (CPP). Finally, it is hard to apply to mixed dislocations whose slab insertion shape is not a simple cuboid but complexly curved one.



(a) TEM image of SMT stacking faults

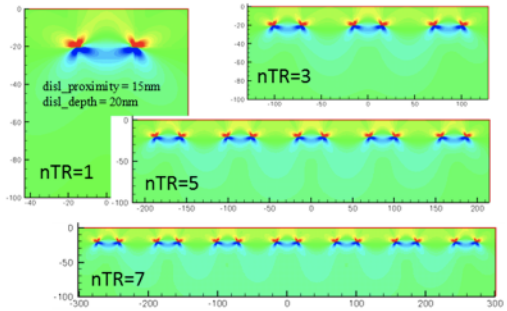


(b) Strain profile across active region

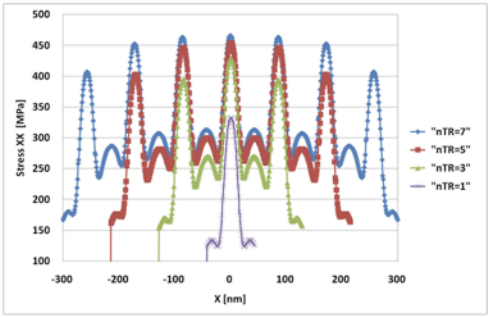
Fig. 5 (a) TEM image of stacking faults in LOD TEG [16] (b) Strain profile simulated by new hybrid approach

With new hybrid dislocation field approach, the LOD effect generated by the hetero-interface between rigid Si and soft STI oxide is successfully reproduced as shown in Fig.5.

And also, the channel stress increase by nested dislocation field with increasing transistor number and smaller contacted poly pitch (CPP) are successfully simulated as shown in Fig.6 and Fig.7. Different from other stressors likes embedded SiGe and CESL, the beneficial effect of D-SMT does not decrease with CPP scaling but rather increases according to our analysis.

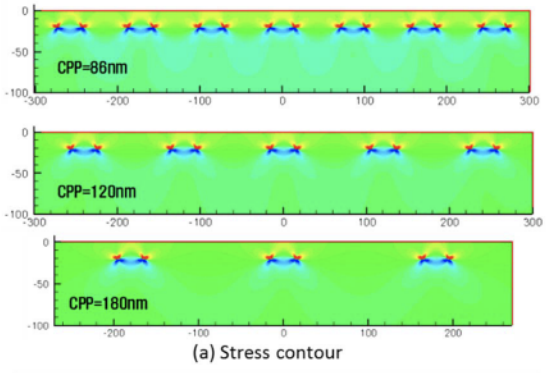


(a) Stress contour

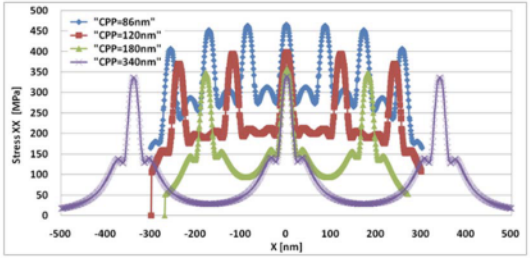


(b) Stress profile at the surface

Fig. 6 Effect of nested dislocation field (a) 2D stress contour (b) stress profile at the channel surface.



(a) Stress contour



(d) Stress profile at the surface

Fig. 7 The effect of CPP (a) 2D stress contour (b) stress profile at the channel surface.

C. *Accuracy check with experimental measurement*

The accuracy of new hybrid approach is confirmed by comparing to experimental strain measurement result with scanning transmission electron microscopy-geometrical phase analysis (STEM-GPA) & scanning moiré fringe (SMF) pattern [17] shown in Fig.8.

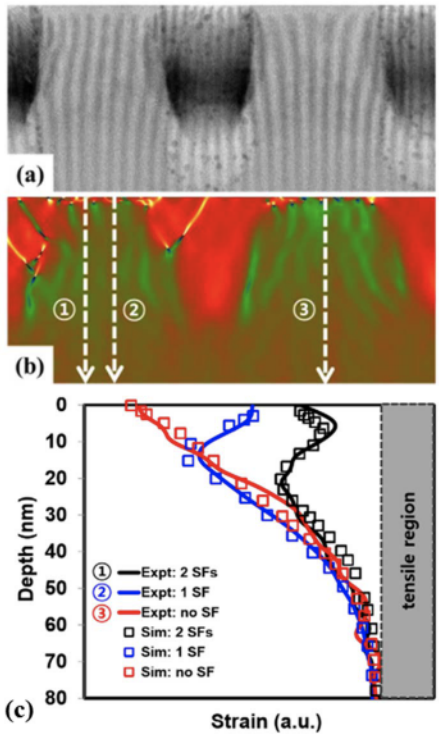


Fig. 8 Strain comparisons with experiments. (a) SMF image (b) Strain map obtained by STEM-GPA. (c) Simulation vs. experimental strain profile

With new approach, it is possible to find the optimal position & number of stacking faults for D-SMT to maximize NMOS performance. And also, you can quantitatively model the degradation of compressive strain in the channel, which causes DC saturation in state-of-the-art PMOS, when [Ge] gradient in the layered structure of eSiGe is too steep.

IV. Conclusion

TCAD prediction of the stress field generated by dislocations is crucial for the optimization of D-SMT for NMOS, its length of diffusion (LOD) dependency on local layout effect (LLE) model, and the degradation of lattice mismatch strain at the Si/SiGe interface. A new approach for dislocation field model, the combination of analytic dislocation field model and succeeding FEM solving to get mechanical equilibrium, is developed and successfully applied to state-of-the-art strained Si devices. New approach works well with multiple dislocations and arbitrary boundary shape so we could model the nested dislocation stress field effect fast with high accuracy. Moreover, it showed good match with experimental STEM-GPA/SMF strain measurements.

References

[1] J. Bardeen and W. Shockley, "Deformation Potentials and Mobilities in non-polar crystals", Phys. Rev. 80, 72 (1950)
[2] C. S. Smith, "Piezoresistance effect in germanium and silicon", Phys. Rev. 94, p.42 (1954)
[3] A. Wei et al., "Multiple Stress Memorization In Advanced SOI CMOS Technologies", IEEE VLSI, p.216 (2007)
[4] N. G. Rudawski et al., "Effect of uniaxial stress on solid phase epitaxy in patterned Si wafers", APL 89, p.082107 (2006)
[5] S. Morarka et al., "Modeling of two-dimensional solid-phase epitaxial regrowth using level set methods", JAP 105, 053701 (2009)
[6] X. Wang et al., "Progress in modeling of SMT "stress memorization technique" and prediction of stress enhancement by a novel PMOS SMT process", SISPAD, p.117 (2008)
[7] H. V. Swygenhoven et al., "Stacking fault energies and slip in nanocrystalline metals", Nature Material 3, p.399 (2004)
[8] Peierls RE. "The size of a dislocation." Proceedings of the Physical Society; 52:34 –37 (1940)
[9] Nabarro FRN. "Dislocation in Solids." North-Holland: Amsterdam (1979)
[10] J. D. Eshelby, "The determination of the elastic field of an ellipsoidal inclusion, and related problems", Proceedings of the Royal Society, London, Series A, 241, 376–396. (1957)
[11] K. Sasaki, et al., "Stress analysis in continuous media with an edge dislocation by finite element dislocation model", Int. J. Numer. Meth. Engng; 54:671–683 (2002)
[12] Wei Cai, "Atomistic and Mesoscale Modeling of Dislocation Mobility", Ph.D Thesis, MIT (2001)
[13] P.M. Derlet et al., "Atomistic simulations of dislocations in confined volumes", MRS Bulletin, vol 34, Mar. (2009)
[14] K-Y. Lim et al., "Novel stress-memorization-technology (smt) for high electron mobility enhancement of gate last high-k/metal gate `devices," IEDM Tech. Dig., 229-232 (2010)
[15] C. E. Weber et. al. "Modeling of NMOS Performance Gains from Edge Dislocation Stress", IEDM (2011)
[16] F. Sato et al., "Process and Local Layout Effect interaction on a high performance planar 20nm CMOS", VLSI (2013)
[17] Jeong-Guk Min et al., "The Impact of Dislocation on Bulk -Si Fin FET Technologies: Physical Modeling of Strain Relaxation and Enhancement by Dislocation", Nanotech. Materials and Devices (2018)