Precise Transient Mechanism of Steep Subthreshold Slope PN-Body-Tied SOI-FET and Proposal of a New Structure for Reducing Leakage Current upon Turn-off

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Abstract—In this study, the precise transient mechanism of the super-steep subthreshold slope PN-body-tied (PNBT) silicon on insulator field-effect transistor (SOI-FET) is clarified by using technology computer-aided design. We found out that the operation mechanism differs between the turn-on and turn-off. Additionally, a new PNBT SOI-FET structure with a second gate for the high-speed operation is proposed and we showed that the new structure can reduce the leakage current upon the turn-off.

Keywords—body tied, feedback, floating body, steep subthreshold slope

I. INTRODUCTION

Ultralow power devices for the Internet of Things and artificial intelligence systems are needed to achieve a nextgeneration society such as Industry 4.0 [1] and Society 5.0 [2]. We proposed PN-body-tied (PNBT) silicon on insulator fieldeffect transistors (SOI-FETs), which have a super-steep subthreshold slope (SS) (<1 mV/dec) with a low drain voltage $(V_d = 0.1 \text{ V})$ [3][4]. A PNBT SOI-FET has the possibility to be applied to ultralow power consumption LSIs, sensors, and neuromorphic chips. We report the DC and transient characteristics of the PNBT SOI-FET; however, an understanding of the operation principle is insufficient, and the device shows a long time leakage current upon a turn-off [5][6]. In this study, we clarify the precise transient mechanism on a PNBT SOI-FET using technology computeraided design and propose a new structure PNBT SOI-FET with a second gate to reduce the leakage current.

II. DEVICE STRUCTURE AND SIMULATION CONDITION

Fig. 1 shows the structure of the PNBT SOI-FET. The actual device was fabricated using a LAPIS Semiconductor $0.2 \mu m$ SOI CMOS process, and device simulations were

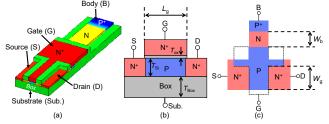


Fig. 1. Device structure of PNBT SOI-FET: (a) bird's eye view, (b) front view, and (c) top view.

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applied using HyENEXSS [7]. The device has a 50-nm thick SOI (T_{Si}), a 200-nm box (T_{Box}), a 4.4-nm thick gate oxide (T_{ox}) (in the simulation, $T_{ox} = 5$ nm), a 0.2-µm gate length (L_g), a 1-µm gate width (W_g), and a 1.2-µm base width (W_b). In the simulation, we used the Shockley–Read–Hall (SRH) recombination, auger recombination, and band-to-band tunneling model. The carrier lifetime parameters in the SRH model were modified (default lifetime × 0.02) to fit the measurement results [8].

III. RESULTS AND DISCUSSIONS

Fig. 2 shows the measured [5] and simulated [6] DC and transient (turn-on) characteristics of the PNBT SOI-FET. The PNBT SOI-FETs have a super-steep SS and turn-on delay time in both measurements and simulations. However, the turn-on delay time decreases when the gate voltage V_g slightly increases, as shown in Fig. 3. Therefore, the turn-on delay time is expected to not be a critical issue for a high-speed operation.

In order to clarify the more precise mechanism of transient effect, we focused on the time dependence of the potential (conduction band energy) shift of the body terminal direction to clarify the precise transient mechanism. The

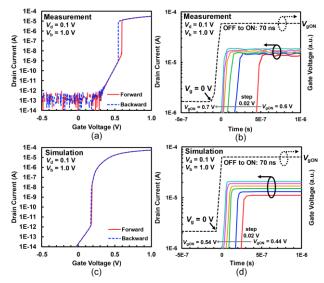


Fig. 2. DC and transient (turn-on) characteristics of PNBT SOI-FET: (a) measured I_d-V_g , (b) measured transient characteristics, (c) simulated I_d-V_g , and (d) simulated transient characteristics.

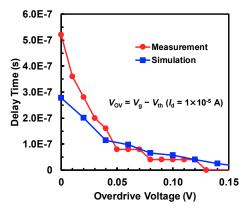


Fig. 3. Overdrive voltage dependence on turn-on delay time.

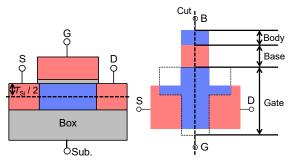


Fig. 4. Cutting direction used to extract potential.

cutting direction used to extract the potential is shown in Fig. 4. Fig. 5 shows the time-shift of the potential upon the turnon. The potential varies as the time proceeds; however, the potential in the gate region and that in the base region behave as different modes of change. Fig. 6 shows the time dependence on the potential in the gate and the base region extracted from Fig. 5. In the base region, the potential gradually decreases (the energy increases). In contrast, the potential in the gate region remains constant and then abruptly varies at (3) in Figs. 5 and 6. We consider the transient mechanism as follows. First, electrons flow from the source to the body just after a turn-on. The electrons modulate the potential in the base region. Second, holes are provided from the body and flow toward the base region. However, the holes recombine in the base region. Therefore, this phenomenon requires a certain amount of time, and the potential gradually modulates. Finally, the holes reach the gate region and modulate the potential of the gate region. This induces a strong

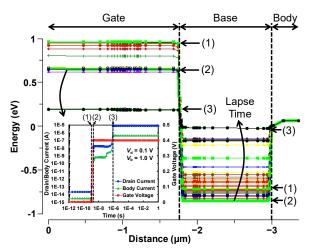


Fig. 5. Time-shift of potential (conduction band energy) upon a turn-on.

positive feedback, and thus the potentials jump to (3) in Figs. 5 and 6. Therefore, Large I_d abrupt flow as shown in Fig. 5. This behavior is similar to that of other devices using a feedback mechanism, such as Z²-FET [9].

Fig. 7 shows the measured [5] and simulated [6] transient characteristics upon a turn-off. The leakage current is

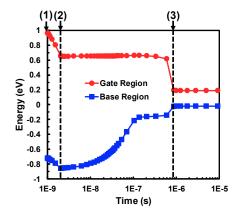


Fig. 6. Time dependence on potential in gate and base region extracted from Fig. 5.

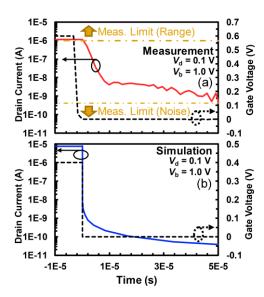


Fig. 7. Transient (turn-off) characteristics of PNBT SOI-FET: (a) measurement and (b) simulation results.

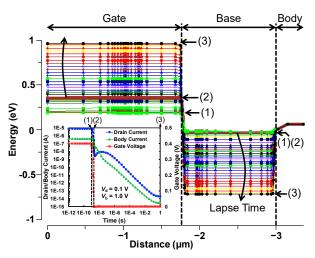


Fig. 8. Time-shift of potential upon a turn-off.

sustained for a few seconds. This is a significant issue of PNBT SOI-FET. Figs. 8 and 9 show the details of the time dependence on the potential shift in the gate and base region upon a turn-off. The potentials of both the gate region and the base region gradually vary as contrasted with the turn-on. For the turn-off, the accumulation carriers in both the gate region and the base region are ejected through a recombination, which unfortunately is a slow operation.

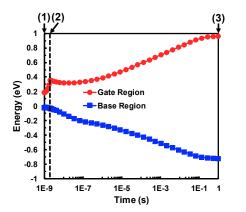


Fig. 9. Time dependence on potential in gate and base region extracted from Fig. 8.

To reduce the leakage current upon a turn-off, we propose a new structure, PNBT SOI-FET with a second gate, as shown in Fig. 10. The objective of the new PNBT SOI-FET structure is to control carrier injection and ejection by using the second gate. The second gate width set to be 1.2 μ m and the width between the first gate and second gate is 50 nm. Fig. 11 shows the simulated DC characteristics of the new PNBT SOI-FET structure. The device also has steep SS characteristics. Additionally, the body current I_b is smaller than I_d as shown in

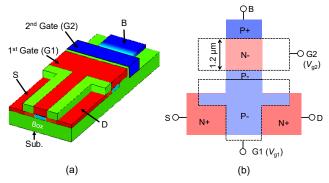


Fig. 10. New PNBT SOI-FET structure with second gate: (a) bird's eye view and (b) top view.

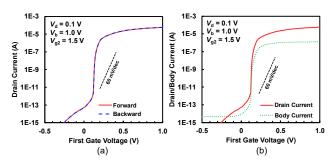


Fig. 11. Simulated DC characteristics of new PNBT SOI-FET structure with second gate. (a) Double sweep I_d-V_g characteristics and (b) I_d and I_b-V_g characteristics.

Fig. 11(b). Therefore, it is possible that the power consumption of the body lower than the power consumption of the drain. 12 shows the simulated transient (turn-off) characteristics of the new PNBT SOI-FET. When the first gate voltage V_{g1} only turns off, the leakage current flow is the same as in Fig. 8. However, for V_{g1} , body voltage V_{b} , and the V_{g2} turn off under the same timing, the leakage current decreases faster than the conventional PNBT SOI-FET. This phenomenon does not occur when V_{g1} and V_b turn off under the same timing (V_{g2} does not turn off). Switching the second gate means that the operation mode changes from PNBT mode to a common body-tied mode. Therefore, the turn-off delay decreases because the accumulation carriers smoothly eject to the body terminal.

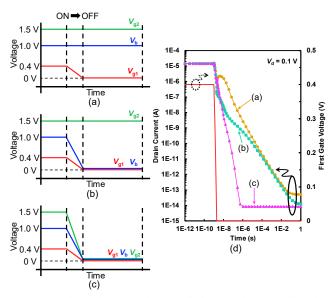


Fig. 12. Waveform of (a) V_{g1} only turn-off, (b) V_{g1} and V_b turn-off, and (c) V_{g1} , V_{b} , and V_{g2} turn-off. (d) Simulated transient (turn-off) characteristics of new PNBT SOI-FET structure with second gate.

IV. CONCLUSIONS

We clarified the precise transient mechanism of the PNBT SOI-FET and proposed a new PNBT SOI-FET structure with a second gate. We found for the first time that the operation mechanism of the PNBT SOI-FET differs between the turnon and turn-off from the time dependence of the potential shift. Additionally, the leakage current on the turn-off can be decreased by $V_{\rm b}$ and $V_{\rm g2}$ control on the new PNBT SOI-FET structure. The new PNBT SOI-FET structure has the possibility of a high-speed operation.

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