Modeling of crystal impurities in III-V ultra-thin body field-effect transistors within the empirical tight-binding framework

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***Abstract*— In this paper, we present a novel technique to model crystal impurities in III-V semiconductors at the material level, within the empirical $sp^3d^5s^*$ tight-binding (TB) framework. Regular semiconductor atoms are replaced by so-called "impurity atoms" whose TB parameters are adjusted to create single trap states characterized by a flat E-k dispersion. With the help of two dimensionless parameters, the energy level of a trap state can be continuously adjusted from deep inside the band gap to well inside the conduction band. To increase trap volume and model more complex defect structures, two or more impurity atoms can be clustered together. Coupled to a Poisson-Schrödinger device simulator, the model accounts for both electrostatic screening caused by free charge carrier trapping and trap-assisted tunneling. In particular, the impact of trap energy and volume on the coherent drive and leakage currents of an ultra-scaled double-gate $In_{0.53}Ga_{0.47}As$ MOSFET is investigated. It has been found that conduction band traps substantially lower the device ON-current, while source-to-drain tunneling assisted by band gap traps significantly increases the subthreshold slope.**

Keywords—III-V; InGaAs; impurity; trap; tight-binding; $sp^3d^5s^*$; atomistic modeling;

I. Introduction

Due to their high electron mobilities and injection velocities, III-V compounds have gained widespread attention as potential replacements for strained-Si n-MOSFETs at not-yet fabricated technology nodes [1]. Although very promising III-V MOSFETs have been recently reported [2][3], high densities of interface traps (D_{it}) at the III-V/high-k interface remain one of the main performance limitations of this technology [4][5]. Traps can induce threshold voltage variability, loss of electrostatic control in either the ON- or OFF-state, mobility degradation, and/or trap-assisted tunneling (TAT).

To predict and confirm III-Vs competitiveness at future ultra-scaled technology nodes, quantum-mechanical device simulations coupled with an accurate model for traps is required. In modeling frameworks based on the Boltzmann Transport Equation, distinct trap models must be used to simultaneously account for electrostatic effects [6] and TAT [7]. Such approaches are usually implemented as pre- and/or post-processing steps in the self-consistent "electrostatics-transport" loop. While it is possible to use similar models in quantum transport solvers [8], an atomistic framework such as empirical tight-binding (TB) [9] offers the possibility to account for crystal impurities and their trapping properties directly as local material perturbations. As a consequence, all trap-related effects are captured in the self-consistent loop without the need for pre- or post- processing steps. Additionally, the discrete nature of traps as 0D localized states is properly taken into account, which is critical in ultra-scaled devices. Indeed, trap models based on average densities of interface traps (D_{it}) [6] obtained from measurements on long channel MOS capacitors [4] [5] do not include effects caused by the random locations of single traps in channels containing less than 10000 atoms.

The paper is organized as follows: In Section II, a TB model for impurities following the previously outlined idea is presented and illustrated with electronic structure and flat-band transmission probability calculations. In Section III, the model is coupled with a Poisson-Schrödinger device simulator to investigate various trap-induced effects in the ultra-scaled $In_{0.53}Ga_{0.47}As$ ultra-thin body MOSFET presented in Fig. 1. Section IV summarizes the main results of this work and briefly discusses other application areas.

II. Method

In the nearest-neighbor $sp^3d^5s^*$ tight-binding formalism, each atom is represented by a basis set of ten orbitals (Löwdin orbitals) interacting with their immediate neighbors, four in the case of zincblende crystals [9]. Traps can be modeled at the material level by replacing regular semiconductor atoms with fictitious impurity atoms characterized by a different set of TB parameters adjusted to obtain the desired trap characteristics. Starting from the default TB parameters of the semiconductor atom, the impurity orbital eigenenergies and hopping parameters (i.e. Slater-Koster interatomic matrix elements) with its nearest-neighbors (NN) are multiplied, or "scaled" by two empirical, dimensionless parameters α_{eig} and β_{hop}:

$$E_{\rho\,tr} = \alpha_{eig}\, E_{\rho\,SC}, \tag{1}$$

$$V_{\rho\gamma\text{-}\xi\,tr\text{-}NN} = \beta_{hop}\, V_{\rho\gamma\text{-}\xi\,SC}, \tag{2}$$

where α_{eig} scales the on-site trap energy $E_{\rho\,tr}$ of orbital ρ (s, p, d, or s*) from the value $E_{\rho\,SC}$ of the original semiconductor atom it replaces. Identically, β_{hop} scales the hopping (off- diagonal)

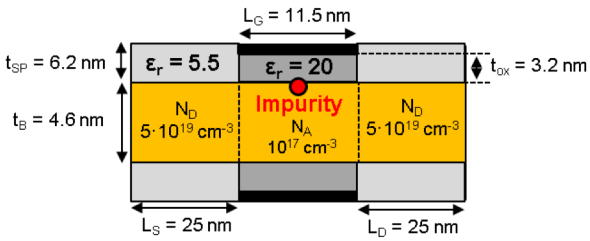

Fig 1: Investigated $In_{0.53}Ga_{0.47}As$ double-gate ultra-thin-body transistor structure in the presence of an impurity in the center of the channel at the semiconductor/oxide interface.

parameter $V_{\rho\gamma\text{-}\xi\ tr\text{-}NN}$ between the impurity orbital ρ and the NN's orbital γ for bond type ξ (σ, π, or δ) from its original value $V_{\rho\gamma\text{-}\xi\ SC}$. When introducing an impurity with properly chosen α_{eig} and β_{hop} into a semiconductor supercell, a single additional band characterized by a flat dispersion appears in the corresponding band structure. This feature is demonstrated in Fig. 2 for a 4.6 nm-thick $In_{0.53}Ga_{0.47}As$ quantum well where the impurity is placed at the edge of the well, i.e. the semiconductor/oxide interface. This behavior clearly indicates that the electronic state induced by the impurity is localized in space. Hence, it can act as a free carrier trap. By continuously varying α_{eig} and β_{hop}, the trap state energy can be freely adjusted from deep inside the band gap (deep trap) to well inside the conduction band (CB trap) (Fig. 3). The possibility of modeling CB traps is critical for III-V-based gate stacks, which are known to present significant trap densities inside the conduction band [4][10]. Deep traps exhibit a perfectly flat dispersion (Fig. 2a), which translates into a Dirac-like local-density-of-states (LDOS) at the trap state energy. CB traps on the other hand show a slight non-zero E-k dispersion because the induced trap state mixes and interacts with the conduction band states in its vicinity (Fig. 2b). For trap energy levels in the semiconductor band gap, an almost linear relationship between E_{tr} and α_{eig} is observed. As soon as E_{tr} approaches and enters the conduction band, this behavior is no longer valid and E_{tr} saturates with respect to α_{eig}. As seen in Eq. (2), increasing β_{hop} strengthens the coupling between the impurity and regular semiconductor atoms, i.e. it increases the interatomic matrix elements. Consequently, a stronger bending of the surrounding bands in case of a CB trap is observed (Fig. 4b). The larger β_{hop}, the lower the slope between E_{tr} and α_{eig}, and the stronger the saturation of E_{tr} with respect to α_{eig} as the trap energy enters the conduction band.

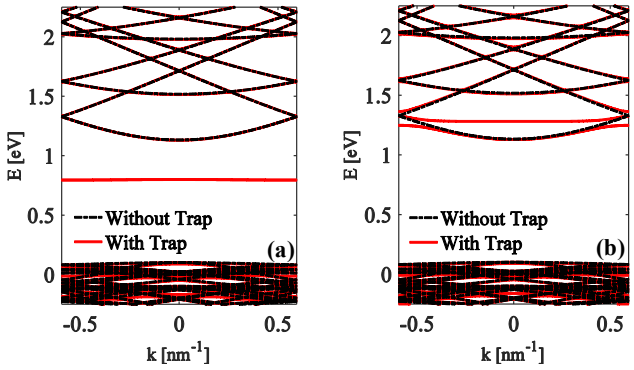

Fig. 2: (a) In-plane band structure of a 4.6 nm thick $In_{0.53}Ga_{0.47}As$ quantum well corresponding to the channel of the device in Fig. 1 with (red) and without (dotted black) a deep interface trap. (b) Same as (a), but for the case of a CB trap. The supercell volume is 5.28×4.6×0.586 nm^3, which corresponds to an interface trap density of 3.2×10^{13} cm^{-2}.

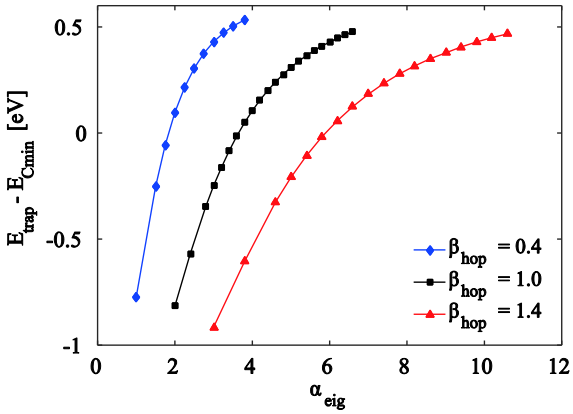

Fig. 3: Trap energy with respect to the conduction band edge as a function of α_{eig} for three different β_{hop} for a 4.6 nm thick $In_{0.53}Ga_{0.47}As$ quantum well.

Because the chosen TB model is limited to nearest-neighbor connections, the interaction range of the added trap state is constrained to the volume of a single atom, irrespective of the value of β_{hop}. This limitation can be overcome by clustering two or more impurity atoms together to form an ¨impurity isle¨. The resulting trap state becomes spatially more extended, which can be leveraged to represent more realistic crystal imperfections. A two-atom impurity, for example, has a stronger E-k dispersion than a single-atom impurity, even if the latter is parameterized with a large β_{hop} (Fig. 4b and 4c). For a CB trap, the effects of β_{hop} and impurity volume on electron transport can be visualized by computing the flat-band electron transmission probability in the channel of the device presented in Fig. 1. As can be seen on Fig. 5, increasing β_{hop} for a single-atom impurity has a marginal effect on the energy window in which the transmission is blocked (trapping window). However, when increasing the trap volume, a significantly larger trapping window is observed. Increasing the trap volume also leads to a lower peak LDOS. This can be understood by the fact that the strong E-k dispersion of two-atom impurities necessarily leads to less states exhibiting a perfectly flat dispersion, as compared to the single-atom case. Nonetheless, the electron transmission at the peak trap LDOS situated at 1.27 eV in Fig. 5 is completely blocked. This is due to the presence of one impurity per out-of-plane unit cell thickness t_{uc} = 0.586 nm, corresponding to a high trap density of 1.5×10^{13} cm^{-2} for the investigated channel length of 11.5 nm.

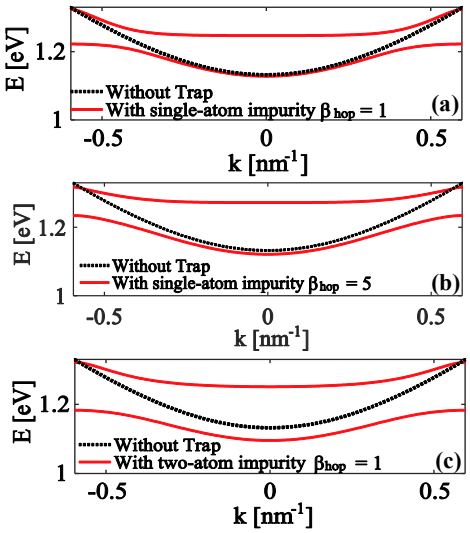

Fig. 4: (a-c) Lowest conduction bands around the trap state energy for three different types of CB traps at the same energy level.

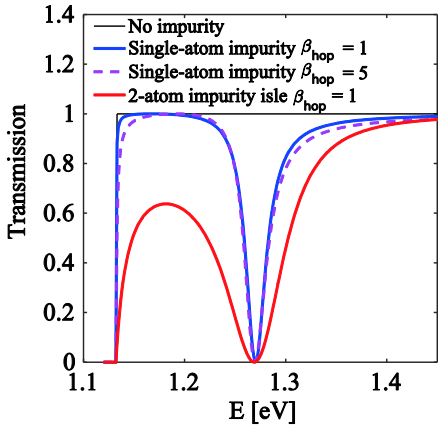

Fig. 5: Transmission probability at flat-band conditions in the channel of the device in Fig. 1 without and with different types of CB traps at 0.138 eV above the conduction band edge.

To simulate lower trap densities, the out-of-plane simulation domain must be extended while keeping a single impurity, thus drastically increasing the computational burden.

III. Results

The model is now coupled with the Schrödinger-Poisson solver presented in [9] to simulate the coherent I_{DS}-V_{GS} transfer characteristics of the ultra-scaled double-gate $In_{0.53}Ga_{0.47}As$ MOSFET depicted in Fig. 1. Four different types of impurities are considered at the semiconductor-oxide interface. Their features are summarized in Table 1. As in the previous section, the out-of-plane periodic device thickness is set to t_{uc}=0.586 nm. The choice of the CB trap energy $E_{tr} - E_{CBmin} = 0.1$ eV has been made in accordance with the experimental findings of [4] and [10], where the conduction band D_{it} starts to exceed 10^{13} cm^{-2}/eV at around 0.1 eV above E_{CBmin}. The specific value of the deep trap energy levels has been arbitrarily chosen and mainly serves as an indication of what effects traps in the band gap might have on this device. It should be noted that determining the exact trap energy levels with respect to band edges is challenging because the strong confinement of electrons in the investigated structure causes substantial energy shifts of the band edges as compared to bulk. This effect has not been studied here.

Impurity type	$E_{tr} - E_{Cmin}$ [eV]
Single-atom CB trap	0.1
Two-atom CB trap	0.1
Single-atom deep trap 1	-0.07
Single-atom deep trap 2	-0.23

Table 1: Energy levels E_{tr} of the four different impurity types considered here with respect to the CB edge of the device in Fig. 1.

In case of a CB trap, free carriers injected from the source/drain reservoir at energies close to the impurity level cannot propagate towards the other side of the device because they are trapped by the impurity. This can be seen in Fig. 6a, where the LDOS of carriers injected from the source contact at the trap energy level peaks at the trap location before decaying to zero in the second half of the device. This creates a hole in the spectral current at the trap energy and a lowering of the ON-current (Fig. 6b). As the gate voltage rises, the number of trapped carriers at the semiconductor/oxide interface increases (Fig. 7a). This gradual charging of the trap weakens the electrostatic control over the potential barrier (Fig. 7b) and further deteriorates the drain current (Fig. 8a). Here, the electrostatic screening is directly caused by the mechanism of free electron trapping. While the ON-current reduction induced by a single-atom CB trap is modest (10 %), the performance deterioration caused by a two-atom CB impurity becomes significant (55 %). This finding is consistent with the previously mentioned fact that a two-atom impurity induces a substantially larger trapping window than one made of a single-atom, while still blocking the electron transmission at the LDOS peak (Fig. 5). As a result, the larger impurity affects the device current immediately after the threshold, whereas the effect of the single-atom impurity is limited to high gate voltages (> 0.5V).

In case of deep traps, a significant subthreshold slope (SS) deterioration is observed. While screening induced by the charging of the trap partly contributes to this effect, the main cause of this phenomenon is source-to-drain trap-assisted tunneling. In effect, it can be seen in Fig. 6d that a large contribution to the OFF-current (≈ 30%) comes from the tunneling component at the same energy as the trap-induced LDOS peak. The shallow trap 1 at 0.07 eV below CB_{min} affects the device characteristics until the thermionic component becomes dominant (ON-state). The effects of trap 2 situated 0.23 eV below E_{CBmin} on the I_{DS}-V_{GS} characteristics vanish as soon as the trap energy level falls below the source E_{CBmin}.

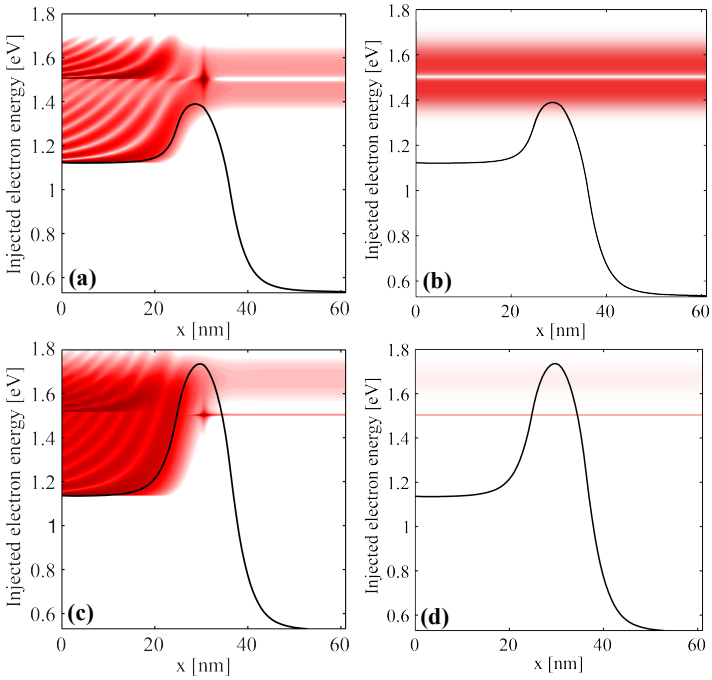

Fig. 6: (a) Source-injected local-density-of-states (LDOS, logarithmic color scale) multiplied by the source Fermi distribution in the ON-state superimposed with the average conduction band profile along the transport direction in case of a single atom CB trap. Red/white color corresponds to high/low values of the LDOS, respectively. The color scale has been adjusted to highlight the influence of the trap state. (b) Corresponding spectral current in the ON-state. Red/white color indicates high/low values of spectral current, respectively. (c) and (d) Same as (a) and (b), but for the deep trap 2 in the OFF-state.

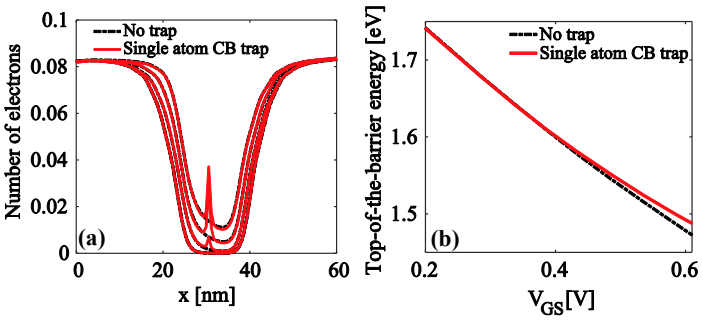

Fig. 7: (a) Number of electrons along the transport direction for increasing gate biases in the device presented in Fig. 1. (b) Top-of-the-barrier energy with respect to the gate voltage.

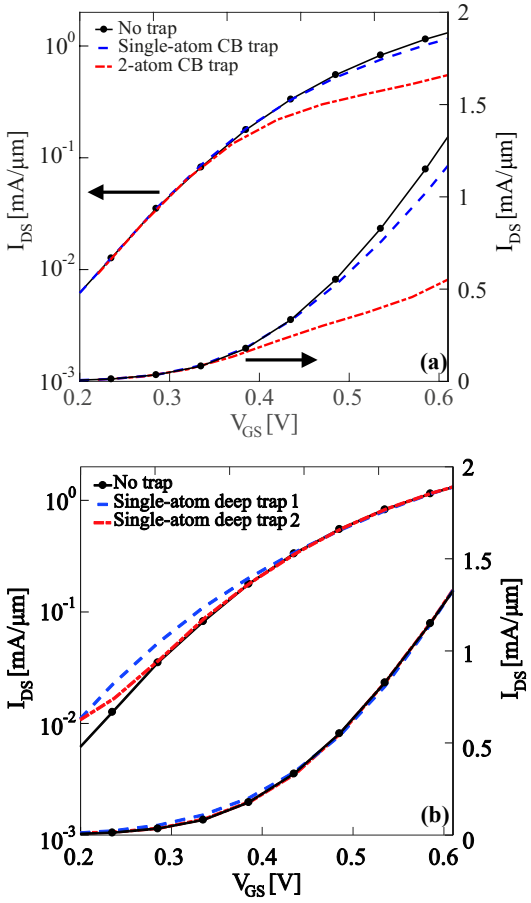

Fig. 8: (a) I_{DS}-V_{GS} characteristics at a drain-to-source bias V_{DS}=V_{DD}=0.61 V for a device without traps and with two types of CB traps. (b) Same as (a), but for two types of deep traps. The OFF-current of the device without traps has been set to 100 nA/μm.

Whereas source-to-drain trap-assisted tunneling is not a sensitive issue in longer channel devices, it exacerbates the already strong tunneling leakage in ultra-short III-V channels and requires careful considerations.

IV. Conclusion

We have demonstrated that in the empirical tight-binding formalism, crystal impurities can be accurately modeled by replacing regular semiconductor atoms with fictitious impurity atoms with a different, well parameterized set of TB parameters. Self-consistent device simulations of an ultra-scaled double-gate $In_{0.53}Ga_{0.47}As$ MOSFET have revealed that the model accounts for both electrostatic screening caused by the trapping of free charge carriers and trap-assisted tunneling. In the investigated device, conduction band traps can significantly lower the ON-current. Band gap traps on the other hand have been found to induce trap-assisted source-to-drain tunneling leading to an increase of the leakage current. The latter effect represents an additional performance limitation factor in devices with a channel length below 15 nm. When calibrated with first-principles data, the model is expected to provide quantitative predictions of trap-induced performance losses in ultra-scaled logic switches. The same approach could also be applied to other materials such as Si, Ge, or SiGe. Furthermore, it can be used to investigate trap-assisted band-to-band tunneling in tunnel-FETs.

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