2D-TCAD Simulation on Retention Time of Z2FET for DRAM Application

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Introduction

Traditional memory devices are facing more challenges due to continuous down-scaling. 6T-SRAM suffers from variability [1-2] and reliability [3-4] issues, which introduce cell stability problems. DRAM cells with one transistor, one capacitor (1T1C) struggle to maintain refresh time [5-6]. Efforts have been made to find new memory solutions, such as one transistor (1T) solutions [7-9]. Floating body based memory structures are among the potential candidates, but impact ionization or band-to-band tunnelling (B2BT) limits their refresh time [10]. A recently proposed zero impact ionization and zero subthreshold swing device named Z2FET [9, 11-12] has been demonstrated and is a promising candidate for 1T DRAM memory cell due to technology advantages such as CMOS technology compatibility, novel capacitor-less structure and sharp switching characteristics. In the Z2FET memory operation, refresh frequency is determined by data retention time. Previous research [11-12] is lacking systematic simulation analysis and understanding on the underlying mechanisms**. In this paper, we propose a new simulation methodology to accurately extract retention time in Z2FET devices and understand its dependency on applied biases, temperatures and relevant physical mechanisms.** Since the stored '1' state in Z2FET is an equilibrium state [9, 11-12] and there is no need to refresh, we will concentrate on state '0' retention. Two types of '0' retention time: HOLD '0' and READ '0' retention time will be discussed separately.

Z2FET Device Operation

The Z2FET structure (Fig. 1) is formed by p-i-n structure on SOI substrate, with partial front gate (FG) and back gate (BG) regions controlling electron and hole potential barriers. The fabrication process is compatible with STMicroelectronics 28 nm FDSOI technology [13]. For memory operation, the FG is biased with a positive voltage while BG is negatively biased, so complementary potential barriers are established in the gated and ungated regions. The complementary potentials prevent/allow (i.e. 0/1 state) carriers flowing between anode and cathode, depending on amount of electrons stored under the FG.

All necessary memory operation simulations such as program '0' (P0), hold '0' (H0), read '0' (R0), program '1' (P1), hold '1' (H1), and read '1' (R1) are illustrated in Fig. 2a. To examine the memory window, a higher anode voltage (VA) is required to switch the device on for state '0'. Lower VA is needed (Fig. 2b) when '1' is written, since the lowered potential barrier. The gap between two VAs is regarded as memory window (Fig. 2b). The experimentally calibrated Z2FET simulation deck (Fig. 3) was implemented using Synopsys Sentaurus TCAD suite [14].

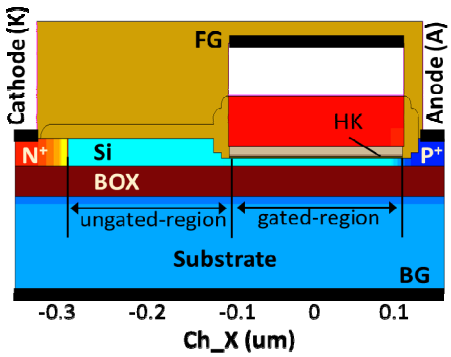


Fig. 1 Z2FET cross section structure used for simulation. Lengths of both ungated and gated regions are 200 nm.

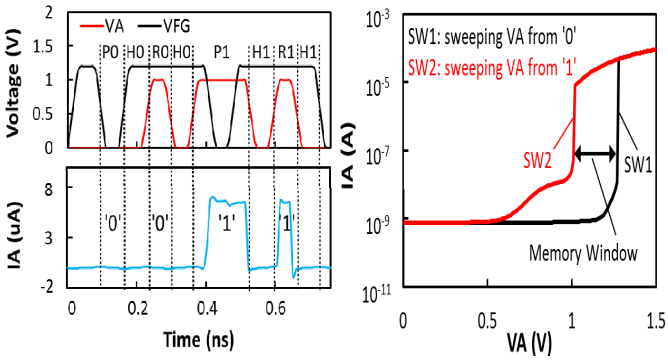


Fig. 2 Demonstration of memory operation that Z2FET works as a DRAM device. (a) Dynamic operation including P0, H0, R0, P1, H1, R1. (b) Memory window exists between data '0' and '1'.

Extraction of Retention Time

The straightforward way of measuring the Z2FET H0 retention time, is to regularly apply a pulsed VA and to monitor its current (Fig. 4 a & b). The time when the output (IA) becomes '1' is then taken to be H0 retention time. This however cannot provide the intrinsic H0 retention time as the applied pulsed-VA accelerates the collapse of stored data and contaminates retention time. Consequently, the extracted retention time is underestimated by several orders of magnitude, compared with the method presented in this

paper (Fig. 4 c, d & e). Using H0 retention as an example, our extraction procedure can be described as follows: 1) Ensure data '0' is stored. 2) Bias to H0 condition and monitor the potential (ψ) of Si channel under the FG. 3) The time holding 0 till the potential collapses is defined as the H0 retention time. Potential collapse under the FG is the basic evidence of data '0' loss, and will be used hereafter to extract retention time for both H0 and R0 operation.

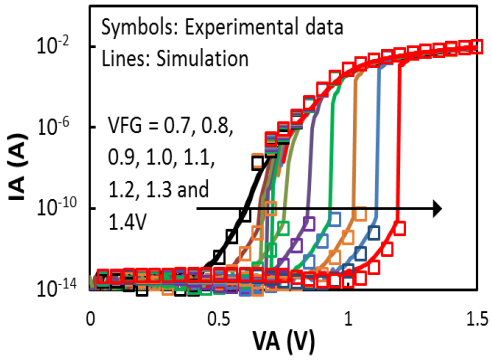
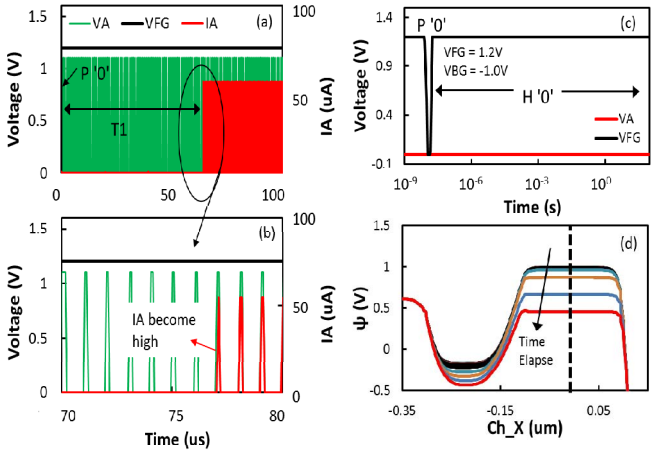


Fig. 3 Calibration of TCAD simulation deck. Simulation results match well with experimental data for various VFG voltages.

HOLD '0' Retention Time

Disruption of a '0' state can be caused by either (1) carrier generation and (2) leakage current induced positive feedback. In a hold condition, VA=VK=0, and no external current flows in the device and the retention degradation is most likely from carrier generation. Fig. 5 shows the evolution from non-equilibrated '0' to equilibrated state '1'. Energy levels of both conduction and valence band increase in the gated-region, and electron density rises. While the hole concentration in the ungated-region remains almost constant. Therefore, the collapse of the data '0' state is due to electron generation and accumulation under the FG. H0-Retention time is VBG and VFG bias independent (Fig. 6).



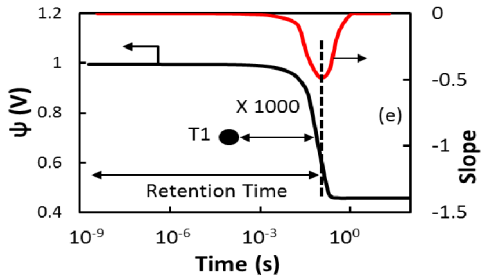


Fig. 4 (a) & (b) Waveform of pulsed method to obtain retention time (H0) T1 when IA becomes high. (c) Waveform to obtain retention time (H0) in this work. (d) Potential along channel X-direction. (e) Time dependent potential at center of Si in gated-region. Retention time extracted in (a) is underestimated by a factor of 1000.

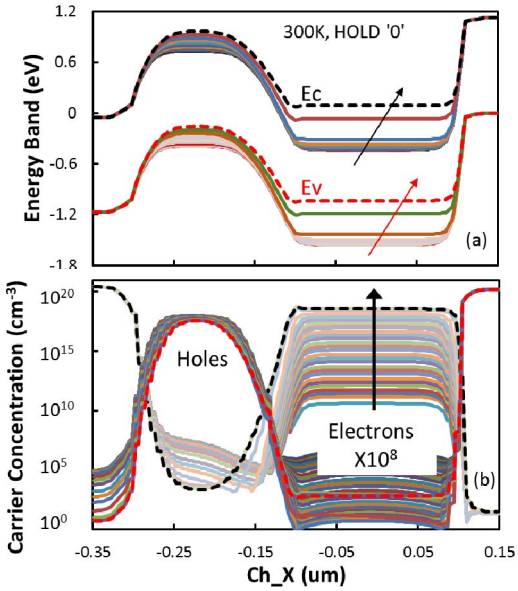


Fig. 5 Evolution of (a) energy band and (b) carriers' concentration distribution during H0 (Fig. 4c). Electrons in gated-region increase by a factor of 10^8, while holes in ungated-region change little. Dashed lines are equilibrium state.

READ '0' Retention Time

The pulsed-VA illustrated in Fig. 4b is actually a read operation. To understand how this pulsed-VA contaminates '0'-Retention time, data retention under a read condition must be investigated. In contrast to H0-Retention, Fig. 7 shows that R0-Retention time has a strong dependency on both VBG and VFG. It benefits from lower |VBG| and higher VFG. With a particular VFG value, the R0-Retention can become extremely long (>1000s in this simulation). All these phenomena obviously indicate the mechanisms of data '0' collapse under hold and read condition are different. To verify this, Fig. 8 shows the energy band and carrier concentration distribution along Si channel. It is observed that the energy level starts to collapse from the ungated-region (Fig. 8b), where the corresponding hole concentration

increases dramatically instead of electron concentration increase in the gated-region (Fig. 5b).

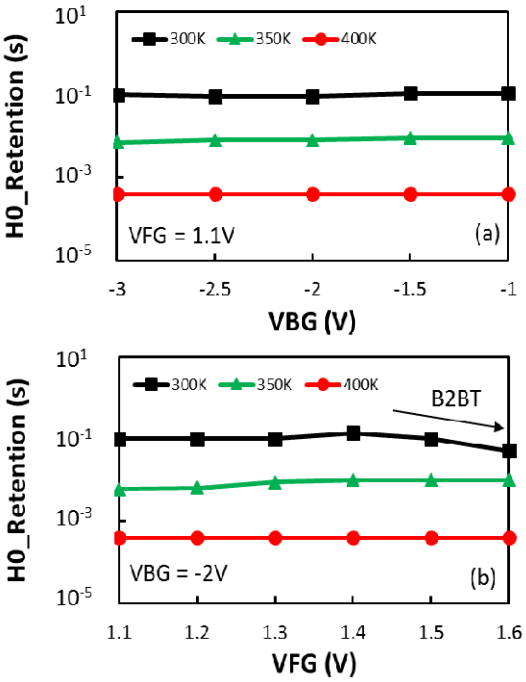


Fig. 6 Extracted retention time under HOLD condition (VA=0V). (a) dependency on back gate bias VBG, and (b) dependency on front gate bias VFG for different temperatures. HOLD '0' retention time is independent on both VBG and VFG.

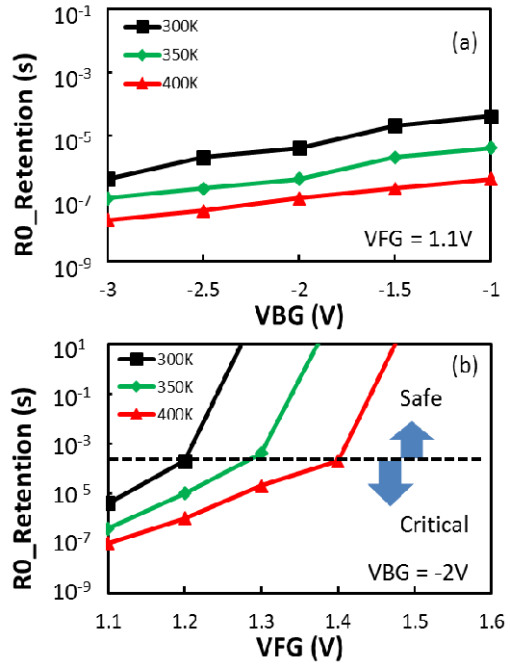


Fig. 7 Extracted retention time under READ condition (VA=1V). (a) dependency on back gate bias, and (b) front gate bias for different temperatures. Retention time above dashed line is extremely long (>1000s), but below is relatively shorter than H0_Retention in Fig. 6.

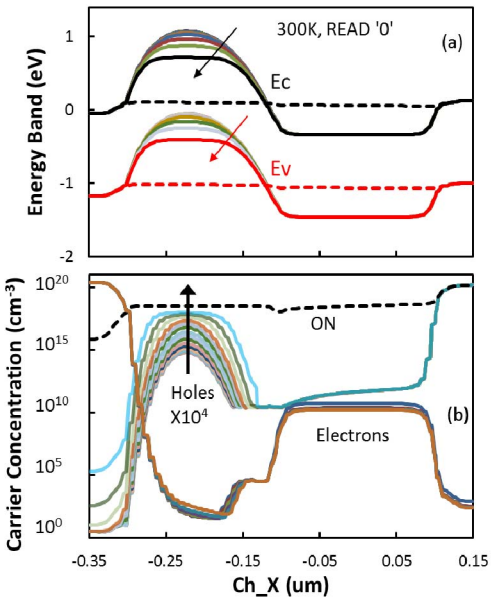


Fig. 8 Evolution of (a) energy band and (b) carriers' concentration distribution during R0 with VFG=1.1V, VBG=-1V. Electrons in gated-region change little, while holes in ungated-region increase by a factor of 10^4. Dashed lines are equilibrium state (ON).

Retention Degradation Mechanism

H0-Retention is controlled by the accumulation of electrons under the FG (Fig. 5). Insensitivity to VFG suggests that it is closely linked to Shockley-READ-Hall (SRH) generation (Fig. 9a) rather than leakage between FG and anode. The slight drop of H0-Retention at higher VFG at 300K (Fig. 6b) is attributed to enhanced Band to Band Tunnelling (B2BT) under a higher field. Generation processes happen mainly in the anode/gated-region junction (Inset of Fig. 9b). Generated electrons collapse the potential barrier to allow hole injection from anode to the ungated-region. At higher temperatures the SRH generation rate increases significantly (Fig. 9a), consequently reducing the retention time (Fig. 6 a & b). Enhancement of the electric field at the front gate does not increase SRH generation rate, so H0-Retention time is almost independent on VFG and VBG (Fig. 6).

For READ 0 operation, hole injection from the anode (Fig. 9b) is enhanced due to the applied positive VA. Holes flow into ungated-region to reduce the potential barrier and trigger positive feed-back. For this reason, a short retention time was obtained by the pulsed-VA method in Fig. 4a. The injection current is controlled by potential barrier established under FG. Higher VFG increases FG potential and reduces or even stops hole injection from anode. Meanwhile SRH generation in the R0 operation becomes insignificant (Insert of Fig. 9b) probably caused by the change of non-equilibrium condition. Therefore, both barriers in gated/ungated region remain unchanged resulting in an extremely long retention time (Fig. 7b). Higher |VBG|

weakens the control of VFG and has a negative impact on the barrier, reducing the retention time (Fig. 7a). At higher temperatures, carriers in the anode can gain more energy and are more likely to cross the barrier and be injected into the ungated-region (Fig. 7 & 9b). The two different retention degradation mechanisms are summarized in Fig. 10.

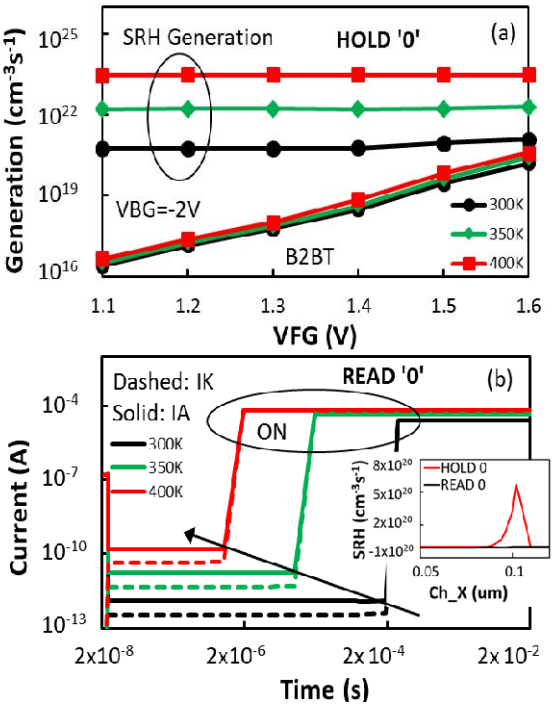


Fig. 9 (a) SRH and B2BT generation under H0 condition. SRH>B2BT even at 300K. (b) Current of anode and cathode under R0 condition. IA-IK before 'ON' is induced by hole injection into ungated-region. Insert is SRH generation rate comparison between H0 and R0.

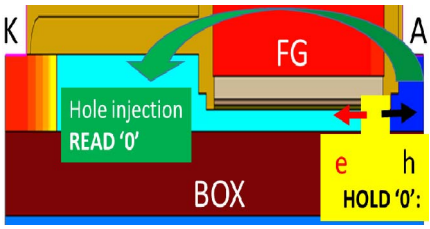


Fig. 10 Illustration of data '0' retention degradation mechanism under HOLD and READ conditions.

Conclusion

Retention time in emerging Z2FET DRAM device has been systematically investigated in this paper. An effective method to characterize retention time is proposed. It has been found that the degradation of HOLD 0 retention originates from gated-region where electrons accumulate. The degradation of READ 0 retention is caused by hole injection into ungated-region. The different degradation mechanisms have different dependency on VFG and VBG. Although retention time under read condition is more critical, careful choose of VFG and VBG can significantly reduce the injection and improve read retention time. We have demonstrated by 2D TCAD simulation that Z2FET is a promising device as candidate of DRAM cells in IoT applications.

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