Z²-FET DC hysteresis: deep understanding and preliminary model

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***Abstract*— Z²-FET, a partially gated diode, was explored for ESD application due to its sharp switching behavior [1,2]. 1T-DRAM application of Z²-FET has recently been evidenced [3,4] leading to an even stronger interest for this device. However, a deep explanation of physical phenomena involved in Z²-FET operation has not been proposed yet. In this paper, we pro-vide a detailed description of the Z²-FET DC behavior based on TCAD simulations and propose corresponding analytical modeling.**

Keywords: Z²-FET, 1T-DRAM, DC operation, TCAD, compact model.

I. INTRODUCTION

Z²-FET (Zero Impact Ionization and Zero Subthreshold Slope FET), has first been introduced as an ESD device because of its sharp switch [1,2]. Its behavior looks like a thyristor but does not involve impact ionization for triggering. More recently, Z²-FET for 1T-DRAM application has been experimentally evidenced [3,4] leading to an even stronger interest for this device. Moreover, its fabrication is fully compatible with standard 28FDSOI technology [4] and does not need any additional process step. To go further and determine if Z²-FET could bring any benefit at application level, a compact model is needed to enable circuit design studies. However, a full explanation of physical phenomena involved in Z²-FET operation and compact model usable in SPICE simulator are still missing. A recent work proposed a comprehensive Z²-FET model describing its complete DC behavior [5]. While predictive of the I-V characteristics, its multiple implicit equations are not compact and can't be used for circuit simulation. In this paper, after describing our Z²-FET TCAD simulation methodology, we propose a detailed explanation of the DC behavior of Z²-FET based on TCAD simulations and we finally propose a full analytical model of Z²-FET DC operation, validated by our TCAD simulations.

II. Z²-FET TCAD SIMULATION METHODOLOGY

Z²-FET device is a partially gated PIN diode on SOI (Fig. 1). It was experimentally demonstrated that Z²-FET DC operation presents sharp switching leading to a DC hysteresis [2]. This original behavior is due to field-induced doping through top and back gates polarization which turns the device into a virtual PNPN structure.

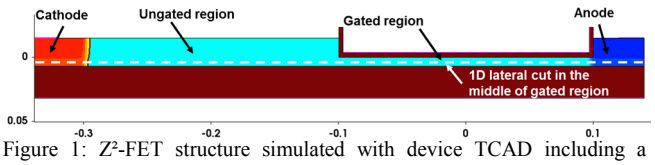


Figure 1: Z²-FET structure simulated with device TCAD including a representation of the 1D cut from cathode to anode used to analyse DC behavior.

We first set up a TCAD [6] methodology to evidence Z²-FET DC sharp switching and hysteresis. Basics physical mechanisms included in our simulations are sufficient to explore Z²-FET behavior, i.e. drift diffusion, constant mobility and SRH generation/recombination models. This is consistent with literature [3], which demonstrated that sharp switching phenomena in Z²-FET operation does not involve impact ionization. We defined basic Z²-FET device (Fig. 1): N-type cathode, P-type anode and intrinsic silicon body with gated and ungated lengths both equal to 200nm. We plotted anode current I_A vs anode voltage V_A for V_G=2V and V_B=-2V (values large enough to ensure sufficient field-induced doping concentration). Fig.2 shows DC hysteresis by sweeping V_A in direct (0 to 2V, dark blue line) and reverse (2 to 0V, light blue line) modes. Sharp switching in direct (V_A=V_{on}) and in reverse (V_A=V_{off}) bias is also captured. However, if DC TCAD Z²-FET is driven by current source, it leads to S-shape I_A-V_A curve (black curve of Fig.2) [1-2] exhibiting negative resistance regime, linking the two switching voltages (V_{on} & V_{off}). We also evidence that, if V_G and/or V_B are not strong enough, Z²-FET behaves as a standard PIN diode (red curve, Fig.2). This behavior was expected because top and back gate need to be sufficiently polarized to build the field-induced doping PNPN structure.

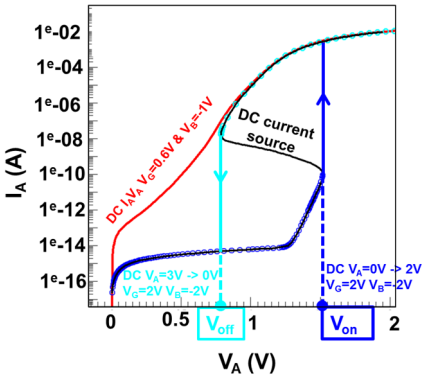


Figure 2: Comparison between Z²-FET I_aV_a obtained by TCAD: red, dark and light blue = voltage driven; Black = current source driven.

III. Z²-FET DC TCAD DEEP ANALYSIS

In the S-shape I_A-V_A curve, five regimes can be identified for Z²-FET DC operation (Fig.3).

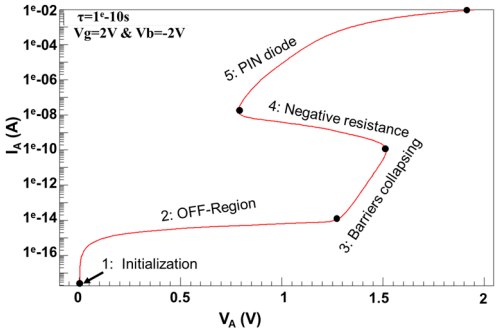


Figure 3: DC current source I_a-V_a with the definition of the five DC operation regimes of Z²-FET.

1-*Initialisation*: V_A=0 and V_G and V_B are respectively positively and negatively polarized to build up N and P-type field-induced doping as illustrated in Fig.4 where carrier densities are plotted along the 1D cut pictured on Fig.1. Barrier potential is thus built up at the junction between gated and ungated regions (see Figure 5). Note that carrier density values in both gated and ungated regions correspond to inversion regime carrier densities of a MOS capacitor. The potential under the gate reaches inversion potential value of MOS capacitor, noted ψ_{Ginv}.

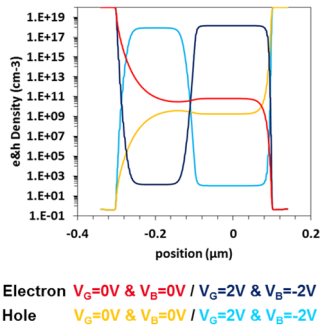


Figure 4: Carrier densities from cathode to anode during *initialization*

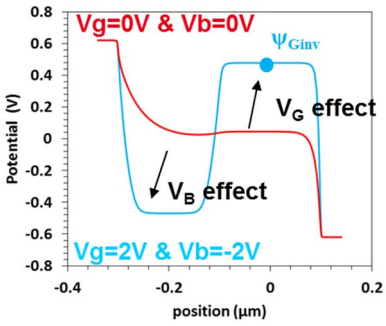


Figure 5: Potential from cathode to anode during *initialization*

For the following steps V_G and V_B are kept constant.
2-*OFF-Region:* V_A is ramped to 1.2V and I_A slightly increases. This produces a lowering of electron density under the gate (field-induced N doping is lowered, Fig.6) which reaches it minimum value, close to intrinsic carrier concentration value. This enables to the PN junctions (P-anode/N-field induced body & N-cathode/P-field induced body) to stay in unpolarized state. This is confirmed by the product of electron and hole densities which everywhere is equal to the square of intrinsic carrier density ($n \cdot p = n_i^2$). The lowering of electron density under the gate produces an increase of the potential, which reaches a maximum value corresponding to depletion regime in a MOS capacitor, ψ_{Gdep} (Fig.6). As potential in gated region increases and is roughly constant in ungated region, the potential barrier between gated and ungated region increases in *OFF-region*.

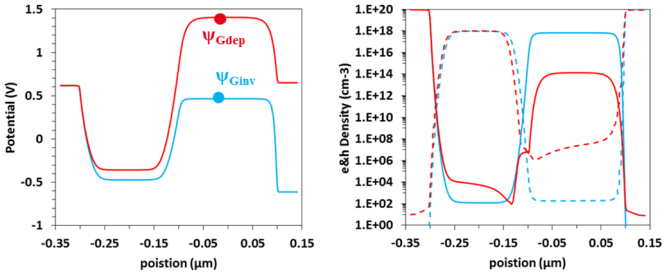


Figure 6: Potential and carrier densities from cathode to anode during *OFF-Region*

3-*Barriers collapsing*: In this regime, while the anode current increases over 4 decades, V_A increases from 1.2 to 1.5V. As all electrons under the gate were removed during *OFF-region*, additional increase of V_A produces the direct polarization of PN junctions. This is evidenced by the product $n.p > n_i^2$ (Fig.7-a) and it also justifies the strong increase of I_A. Similarly, increase of V_A produces an increase of potential in ungated region while potential in gated region stays constant (still equal to its maximum value ψ_{Gdep}), leading to a lowering of potential barrier between gated and ungated region (Fig.7-b). Fig. 7-a also shows that sharp switch (for V_{on}, see Fig.2) occurs when electron density in ungated region is equal to hole density in gated region (corresponding to forward polarized PIN diode condition).

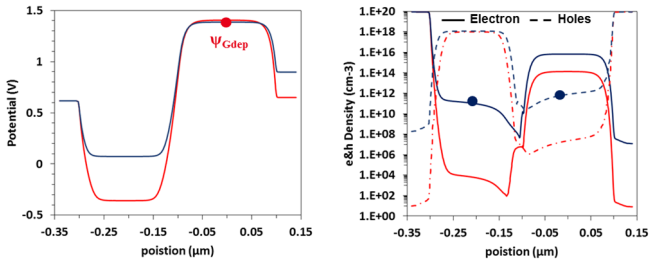


Figure 7: Potential and carrier densities from cathode to anode during *Barriers collapsing*

4-*Negative resistance*: V_A decreases from 1.5V to 0.8V and I_A increases by 2 decades. This regime is a kind of transition between the Z²-FET off and on states. Electron density increases in the gated region while it reaches hole density value in ungated region (Fig. 8-a). This corresponds to sharp switch (V_{off} see Fig. 2). The potential in the gated region moves from depletion to inversion values during the *negative resistance* regime (Fig. 8-b): this provides a usable criterion to evaluate analytically V_{off}.

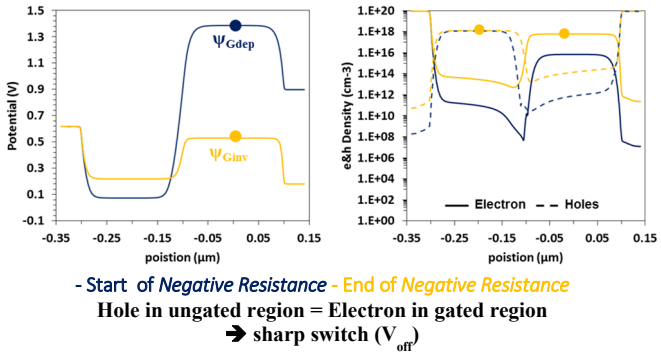


Figure 8: Potential and carrier densities from cathode to anode during *Negative Resistance*

5-*PIN diode*: Z²-FET acts as a PIN diode forward biased (Fig. 9). Electron and holes concentration are superimposed in this regime, what demonstrates that transport mode has moved from classical MOSFET to ambipolar mode.
The full Z²-FET DC operation is sketched on Fig. 10.

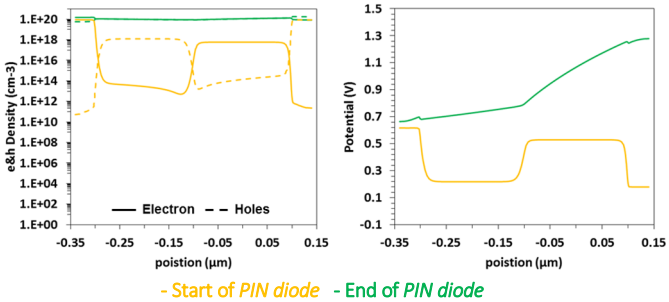


Figure 9: Potential and carrier densities from cathode to anode during *PIN diode* mode operation.

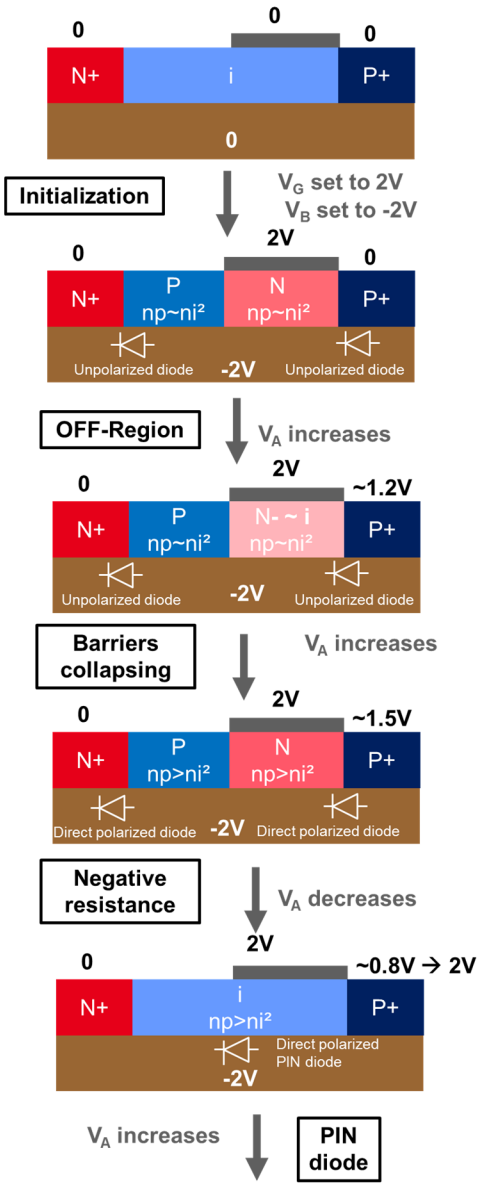


Figure 10: summary of the complete Z²-FET DC operation

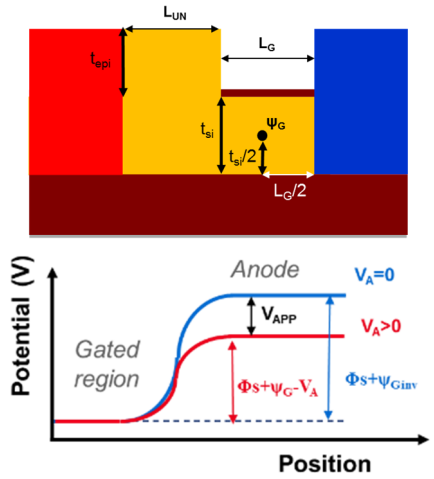
IV. Z²-FET ANALYTICAL DC MODEL

As Z²-FET is a partially gated PIN diode, $I_A(V_A)$ can be modeled using ref. [7] and considering diode ideality factor of 2, leading to:

$$I_A = I_{La}\left(e^{\frac{V_{App}-R_{PIN}I_A}{N.ut}} - 1\right) + I_{Rec}\left(e^{\frac{V_{APP}-R_{PIN}I_A}{N.ut}} - 1\right)^2 \quad (1)$$

where I_{La} and I_{Rec} respectively stand for diffusion and recombination currents, R_{PIN} represents the intrinsic region resistance and $ut = kT/q$. In PIN diode regime, this equation is used natively (V_{APP}=V_A) while in regimes OFF-region and Barriers Collapsing, V_{APP} has to account for change in potential reference through $V_{APP} = V_A + \psi_{Ginv} - \psi_G$ (Fig.11). ψ_{Ginv}

(and ψ_{Gdep}) are analytically evaluated through an adaptation of Leti-UTSOI model [8].



$$V_{APP}=V_A+\psi_{Ginv}-\psi_G$$

Figure 11: Z²-FET modeling parameters and applied voltage V_{APP} evaluation.

The variations of ψ_G and $V_A+\psi_{Ginv}$ are plotted on Fig.12 as a function of V_A. In *OFF-region*, V_{APP} is close to zero (dashed green rectangle on Fig.12) and the square term in I_A can be neglected. As anode current in this regime $I_{AOFF\text{-}Region}$ is weak, the resistance of intrinsic region R_{PIN} can be neglected. It leads to:

$$I_{A_{OFF}-Region} = I_{La_{OFF}-Regime}\left(e^{\frac{V_{App}}{N.ut}}-1\right) \quad (2)$$

In *barriers collapsing* regime, $V_{APP}>>R_{PIN}I_A$ (dashed blue rectangle on Fig.12) and the first term of (1) can be neglected and similarly to OFF regime, intrinsic region resistance can be neglected, leading this expression of anode current in *barriers collapsing* regime, I_{ABC}:

$$I_{A_{BC}} = I_{Rec_{BC}}\left(e^{\frac{V_{App}}{N.ut}}-1\right)^2 \quad (3)$$

Since the *negative resistance* region is too complex for physics-based analytical model, we used a behavioral linear dependency of I_A (in log scale) with V_A (Fig.2 & 3) linking both switching positions. Fitting our model on TCAD results allowed to reach good accordance as illustrated on Fig. 13.

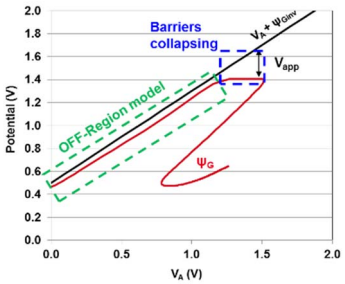


Figure 12: Potential in gated region ψ_G (red) and $V_a+\psi_{Ginv}$ as a function of V_a extracted from TCAD.

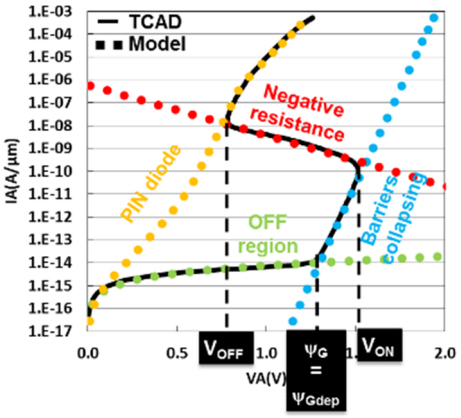


Figure 13: Z²-FET analytical models validation by DC TCAD.

V. Conclusion

In this paper, we revealed and explained the complex DC behavior of Z²-FET and also proposed an analytical model validated by TCAD simulation. To achieve compact model, analytical evaluation of boundary conditions between each operating regime are necessary (ψ_{Gdep}, V_{on} and V_{off} shown on Fig.13) together with smoothing functions between each regime to ensure continuity. This model is compatible with the conventional SPICE simulator to finally enable Z²-FET circuit simulation and design studies.

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