Sub 0.5 V bias voltage operation of a triple-topgate graphene tunnel field effect transistor

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***Abstract*—We propose a triple-topgate graphene tunnel field effect transistor (GTFET) and report the device performance based on non-equilibrium Green function (NEGF) simulations for the bias voltage lower than 0.5 V. The proposed GTFET structure shows a remarkable device performance such as the subthreshold swing (SS) of 28 mV/dec and the ON current lager than 500 μA/μm in the saturation region. We found that the negative differential resistance on the output characteristics arises from a strong coupling between the electrodes and the p- and n-type regions. Moreover, we develop a GTFET compact model, which works consistently with NEGF simulation results for the bias voltage $\geq$ 0.1 V.**

***Keywords*—Graphene, Tunnel field effect transistor, Triple-topgate electrostatic doping, GTFET compact model.**

I. Introduction

The circuit performance of the very large scale integrated (VLSI) circuits have been improved by down scaling of complementary metal-oxide-semiconductor (CMOS) devices and advanced circuit design technologies. However, the continuous miniaturization of CMOS devices reaching to sub-10 nm gate lengths brings not only performance improvement, but also an increase of the static power consumption [1], [2]. This power is mainly determined by the leakage current and subthreshold swing (SS). For CMOS devices with such small dimensions, the leakage current is increased due to the short channel effect. On the other hand, the SS is limited to at least 60 mV/dec at room temperature because the drain current depends on conduction carriers which follow the Boltzmann distribution [3]. In order to overcome these issues, it is necessary to develop novel switching devices based on new physics.

The tunnel field effect transistor (TFET) is a promising candidate for the beyond CMOS era. The ON-current of TFETs is governed by the band-to-band tunneling (BTBT) between the p-type and the intrinsic region. The OFF-state current, on the other hand, is determined by the Fermi-tail blockage of the p-type region and carrier tunneling blockage of the intrinsic region. Furthermore, the subthreshold slopes (SS) lower than the thermal limit of 60 mV/dec for MOSFETs are possible for BTBT in TFETs, and the drain current depends on the tunneling probability. Recently, TFETs based on various semiconductors have been demonstrated [4]. However, the ON current is very low due to the high tunnel resistance. In order to overcome the inherent low ON current issue for TFETs, graphene has been proposed as the channel material [5] due to its extremely high carrier mobility and finite band gap realized by controlling the width of a graphene nanoribbon (GNR). Moreover, large-scale planar graphene device fabrication is possible. In this work, we study the proposed graphene triple-topgate TFET based on NEGF simulations and a newly-developed compact model which works quite well with the same set of parameters for bias voltages $\geq$ 0.1 V.

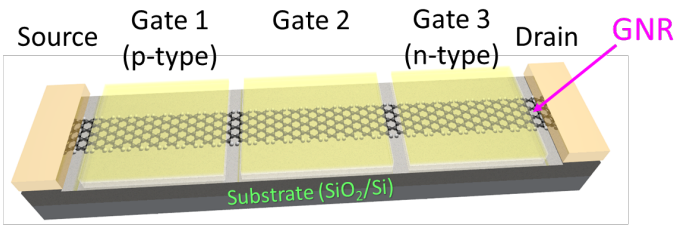

Fig. 1. GTFET device structure. Gate 1 and 3 voltage set to -1.1 V and +1.1 V. The bias voltage is applied symmetrically.

II. Novel GTFET Structure and Computational Method

We study the GTFET device structure that is schematically illustrated in Fig. 1. It is composed of a GNR with source and drain contacts, as well as regions with individual top gates. The edge of GNR is terminated by hydrogen atoms. The dielectric constant of gate dielectric is 4.0 ϵ_0. The thickness of metal gate electrodes and gate dielectric is 0.1 nm. The perfect GNR has a width (W) of 0.9 nm, corresponding to 1.3 eV band gap opening. High mobility semiconductors typically suffer from high direct tunneling leakage current [6], however, this is mitigated here by the large band gap opening. Experimentally, the largest reported band gap of GNR is in the range of 0.4 eV by using the unzipped carbon nanotube [7]. The tunneling probability according to the WKB approximation is describe for GNR based TFETS by [5]

$$T_{\mathrm{WKB}}(E) = \exp(-\pi E_{\mathrm{g}} W_{\mathrm{T}}/\hbar V_{\mathrm{F}}) \quad (1)$$

where E_{g} and W_{T} are energy band gap and tunneling length, respectively. The $\hbar$ and V_{F} indicate the reduced Plank constant and Fermi velocity. Thus, the lower energy gap can be mitigated by using a longer channel region and thus larger W_{T}. The electrostatic doping of carbon-based materials is an essential technique for its use in semiconducting applications as conventional doping is difficult in these materials [8]. Here, gate 1 (gate 3) is biased to form the $p(n)$-doped source(drain) region, while gate 2 is varied from negative to positive voltage to switch the device. Although BTBT in graphene has been recently demonstrated experimentally in a two top gate structure [9], the triple top gate structure as shown in Fig.1 is used as

TABLE I. DEVICE PERFORMANCE OF GTFET.

V_{bias} (V)	SS (mV/dec)	Maximum I_{ON} (μA/μm)	Minimum I_{OFF} (fA/μm)	ON/OFF ratio ($\times 10^9$)
0.5	28.5	1282.1	805.3	1.6
0.3	34.1	820.0	126.0	6.5
0.1	31.8	305.7	12.5	24.5
0.005	46.6	85.1	0.7	118.1

it can realize lower OFF-state current. The source and drain region are defined by metallic AGNR [10]. The influence from substrate is not considered in our simulation. We used the self-consistent NEGF simulations based on the Slater Koster tight-binding (SKTB) model that is implemented in the Atomistix ToolKit (ATK) [11]. Here, we use the mio parameter in the calculation [12]. The developed compact model is based on the Kane-Sze expression [13].

III. RESULTS AND DISCUSSION

Figure 2 shows the local density of states at the OFF- and ON-states, for the symmetric bias voltage V_{bias} of 0.5 V. The source and drain potential (μ_s and μ_d) are indicated by the dashed lines. For all these simulations, we use a gate 1 voltage of -1.1 V, and gate 3 voltage of +1.1 V, while gate 2 is used as the control gate with variable bias V_{G2}. In the case of the OFF state ($V_{G2} = 0$ V), the transmission probability between the p-type and n-type regions is reduced by the band gap in the intrinsic channel region (Fig. 2(a)). The small transmission probability inside the bias window indicates the direct tunneling between p-type and n-type region (Fig.2 (b)). In the ON state ($V_{G2} = 1.0$ V), the conduction band edge in the region below gate 2 shifts to a lower energy than the valence band edge of the p-type region below gate 1 (Fig. 2(c)). In this case, the BTBT probability inside the bias window is drastically increased, leading to a high transmission probability (Fig. 2(d)).

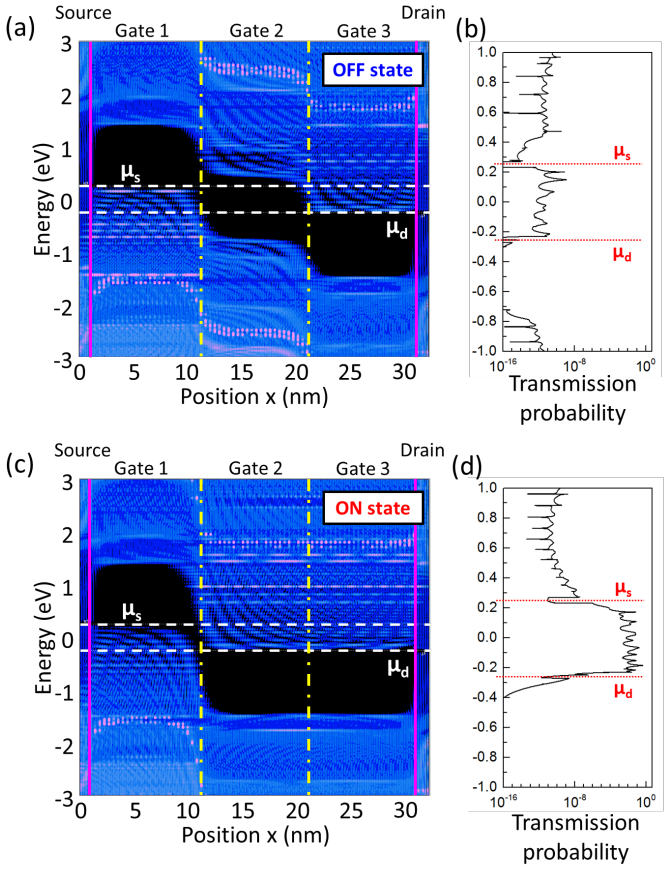

Fig. 2. Local density of states and transmission spectrum; (a) and (b) is LDOS and transmission spectrum at OFF state ($V_{G2} = 0$ V), respectively. (c) and (d) at ON state ($V_{G2} = 1.0$ V). The dashed line indicates the bias window region.

Figure 3 shows the calculated transfer characteristic. When 0.2 V $< V_{G2} <$ 0.3 V and $V_{bias} = 0.5$ V, the minimum SS of 28 mV/dec and the ON current larger than 500 μA/μm at the saturation region are achieved together with the OFF current smaller than 1 pA/μm. The maximum ON current (at $V_{G2} = 1.3$ V) and the ON/OFF ratio are 1233.8 μA/μm and 2.9×10^9, respectively. According to the WKB approximation, same OFF current is achieved by extending the channel by 30 nm for a GNR with a band gap of 0.4 eV. The device characteristics under various V_{bias} configurations (compare Figure 3) are summarized in Table 1. The SS tends to increase with the decrease in V_{bias}. Although the ON current decreases with decreasing V_{bias}, the maximum ON current is still larger than 100 μA/μm at $V_{bias} = 0.05$ V. Contrary, the OFF current is drastically reduced. The ON/OFF ratio is increased for low bias.

Figure 4(a) shows the output characteristic of the GTFET as function of V_{bias} for different V_{G2}. At high gate voltage ($V_{G2} > 0.6$ V), drain current saturation around $V_{bias} = 0.1$ V is noted. For bias voltages below 0.1 V, the tunnel resistance-dominated (TRD) and channel resistance-dominated (CRD) regions [14] can be observed. The negative differential resistance (NDR) appears at $V_{G2} < 0.5$ V. It is attributed to the strong coupling between the electrodes and p-type (n-type) density of states (DOSs) with van Hove singularity under gate 1 and gate 3 (Fig. 5 (a+b)). The NDR can be regarded as instability of device performance. However, in practice it will be thermally smeared and it can be further reduced by replacing the GNR in the source and drain region by a wider GNR or graphene sheet.

For circuit simulation, a (semi-empirical) model able to reproduce the ab-initio simulation results is required for reasons of speed and computational cost. We developed such compact model (CM) based on the WKB approximation [5] and analytical TFET model [15],

$$I_{ds} = \alpha \cdot f \cdot V_{tw} \cdot \zeta \cdot T_{WKB}(\zeta) \quad (2)$$

$$V_{tw} = \ln\left[1 + \exp(\{V_{gs} - V_{th}\}/U)\right] \quad (3)$$

$$U = R_0 \cdot V_t \cdot N_1 + (1 - R_0) \cdot V_t \cdot N_1 \cdot V_{goe}/V_{th} \quad (4)$$

$$f = \{1 - \exp(-V_{ds}/\Gamma)\}/\{1 + \exp([V_{thds} - V_{ds}]/\Gamma)\} \quad (5)$$

$$T_{WKB}(\zeta) = \exp(-\zeta/\zeta_0) \quad (6)$$

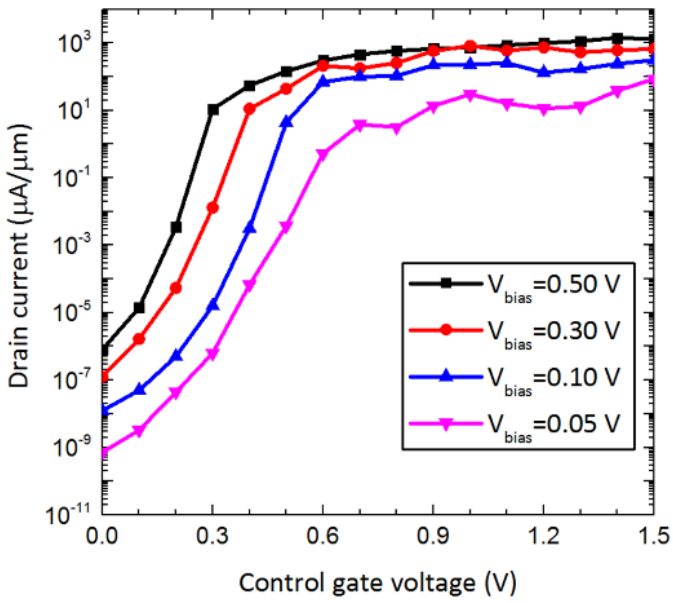

Fig. 3. Transfer characteristic with different bias voltages.

$$\zeta = \zeta_0(1 + \gamma_1 V_{ds} + \gamma_2 V_{gs}) \tag{7}$$

f and U are the dimensional and Urbach factors, respectively. Other parameters are listed in Table 2. Figure 6 compares the developed compact model (CM) with the ab-initio simulation results. A good consistency of this model is achieved when $V_{bias} \geq 0.1$ V. For $V_{bias} = 0.05$ V, a larger subthreshold ideality factor N_1 and a reduced saturation shape parameter Γ are used in the different parameter compact model (DPCM), which accurately reproduces the GTFET characteristics.

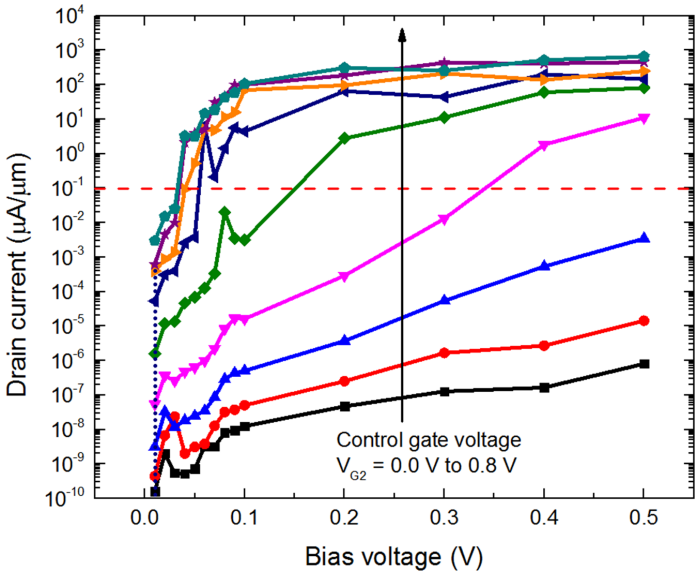

Fig. 4. Output characteristic. The red dashed line is the ON state current threshold.

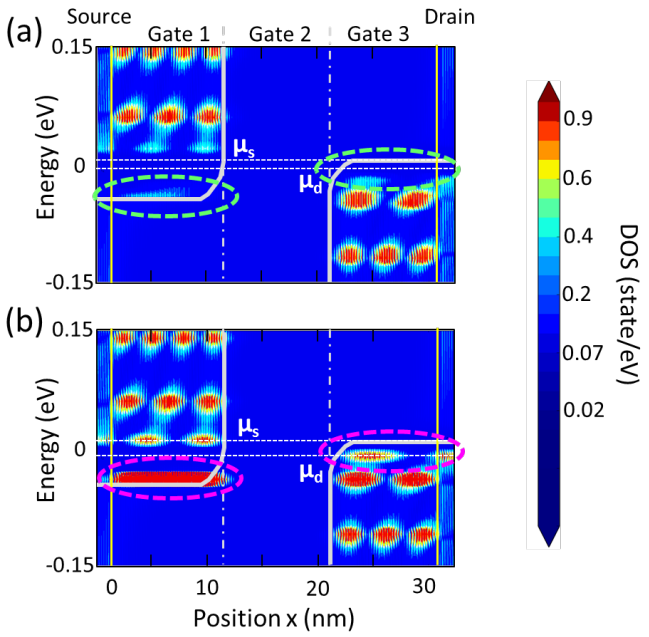

Fig. 5. Electrode coupling; (a) local density of states at $V_{bias} = 0.02$ V and (b) 0.03 V with $V_{G2} = 0.1$ V. The coupling regions are indicated.

IV. Conclusion

In this work, we have proposed a triple-topgate GTFET structure and reported its superior performance based on the NEGF simulation with the Slater-Koster tight-binding parameters. We also developed a GTFET compact model which consistently works with the same set of parameters for $V_{bias} \geq 0.1$ V. The parameters need to be modified only for < 0.1 V. Furthermore, the NDR observed in the output characteristics is

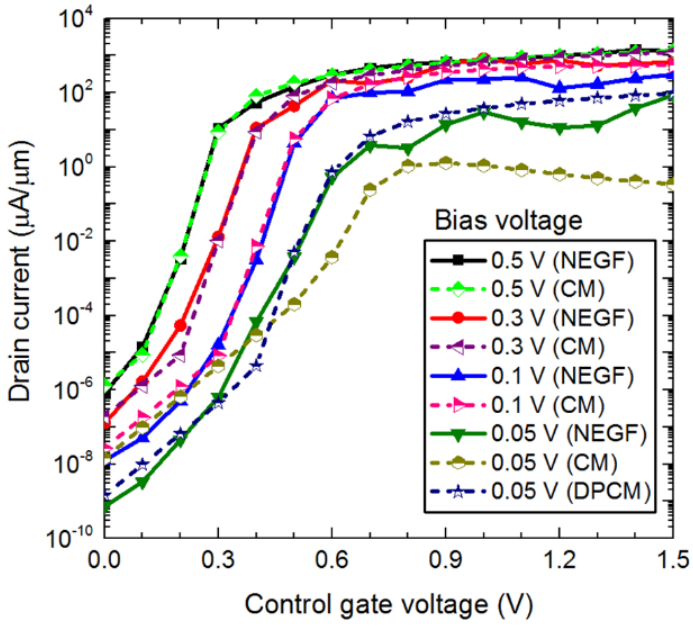

Fig. 6. Comparison of the transfer characteristics of compact model with NEGF results. The CM and DPCM are the compact model and different parameter compact model, respectively.

TABLE II. LIST OF COMPACT MODEL PARAMETERS

Parameters	Description
α	Material dependent property
V_{tw}	Tunneling window
V_{gs}	Gate-source voltage
V_{th}	Threshold voltage
V_{t}	Thermal voltage
V_{ds}	Drain-source voltage
V_{goe}	Ratio of $(V_{\text{gs}} - V_{\text{OFF}})$ and $(V_{\text{ds}} - V_{\text{OFF}})$
V_{thds}	Drain threshold voltage
ζ	Electric field in junction region
ζ_0	Built-in electric field in junction region
R_0	Tunneling window parameter
N_1	Subthresold ideality factor
Γ	Saturation shape parameter
γ_1	Electric field parameter
γ_2	Electric field parameter

attributed to the strong coupling of the DOS in the channel and the DOS of the electrodes via van Hove singularities. These results show a promising way to overcome inherently low ON currents in the conventional TFETs and may contribute to further development of beyond CMOS ultra low power circuits.

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