Accurate BEOL Statistical Modeling Methodology with Circuit-Level Multi-Layer Process Variations

Young-Seok Song[(1)(2)], Chun-Yee Chu[(1)], Jongwook Jeon[(1)], Ui-Hui Kwon[(1)], Keun-Ho Lee[(1)] and SoYoung Kim[(2)]
[(1)] CAE team, Semiconductor R&D Center, Samsung Electronics Co. Ltd.
Hwasung-City, Gyeonggi-Do, Republic of Korea
[(2)] College of Information and Communication Engineering, Sung Kyun Kwan University
Suwon-Si, Gyeonggi-Do, Republic of Korea
yseok.song@samsung.com, *ksyoung@skku.edu*

***Abstract*— As technology scales down, the impact of BEOL (Back-end of Line) interconnect resistance (R) and capacitance (C) on speed and power of digital circuits have been ever-increasing. Furthermore, in 3-D structured transistors, such as FinFETs and Nano-wire FETs, the parasitic R & C of MOL (Middle of Line) have larger impact on performance and power of the products. Hence, analysis of impact on variations of BEOL and MOL on parasitic component change is necessary. The conventional interconnect corner model uses extreme BEOL variations. However, the possibility of such extreme conditions occurring is stochastically very rare. Therefore, tightened corner models were proposed in order to reduce excessiveness in corner simulations. But this tightened corner models still have excessive ranges because each layer is statistically analyzed separately. In this study, we propose a circuit-level multi-layers aware BEOL corner (CMBC) based on Monte Carlo (MC) simulation of ring-oscillator circuits. This modeling methodology takes into account of both MOL process variations and multi-BEOL layers. As a result, the proposed corner model has a tighter distribution ranges of R & C. Therefore the proposed model allows circuit designers to reduce unnecessary efforts.**

Keywords*— *BEOL corner model, Process variations

I. INTRODUCTION

Conventionally, designers validate a chip design to ensure functionality at extreme PVT (Power-Voltage-Temperature) conditions. However the impact of Back End of Line (BEOL) resistance and capacitance on performance and power of product has been increasing across technologies [1][2][8][9]. It is reported that the interconnect delay will become the dominant factor in 10nm and beyond as shown in figure 1 [6]. The delay gap between interconnect and gate has widened to be more than 10,000 times at 10nm node.

Furthermore, both resistance and capacitance (RC) of middle of line (MOL), which connects gate or active regions to the metal layer, have a larger impact on performance of product in 3-D device, such as FinFET and Nano-wire FET as shown in figure 2 [13]. Hence, process variations of BEOL and MOL have become more important and accurate analysis is necessary.

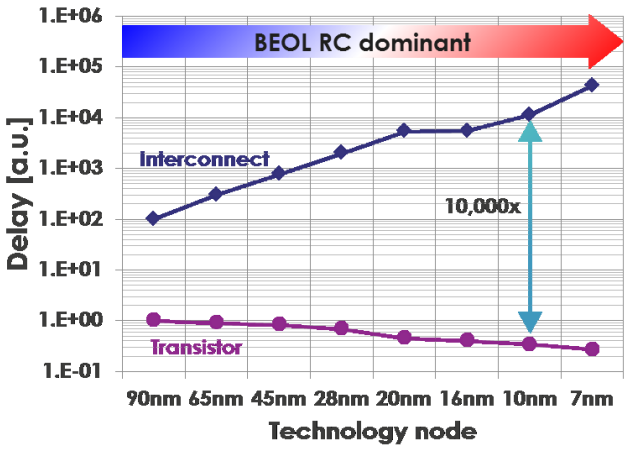

Figure 1. As scaling down, impact of interconnect RC on speed been ever-increasing. At advanced technology nodes, interconnect delay will become the dominant factor.

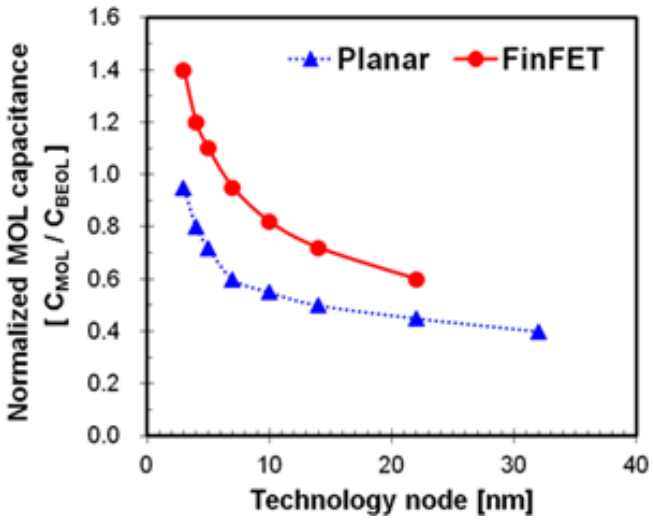

Figure 2. Trend of MOL capacitance with regard to BEOL capacitance for BEOL wire Length of 70 metal pitches

Conventional BEOL corner model uses extreme BEOL variations as shown in Table 1 [12]. However such minimum (or maximum) corner conditions occur very rarely. Because probability of having minimum (or maximum) simultaneously is extremely low, if parameters are not fully correlated. Therefore this condition is too pessimistic.

To avoid the overestimation of conventional BEOL corner model, tightened BEOL corner model is used in current industry as shown in figure 3 [4]. However such tightened model doesn't take account of multi-layers. Hence it is still pessimistic.

To reduce the pessimism, BEOL variation aware timing analysis method is proposed based on a parasitic extraction tool [5]. The parasitic extraction tool can annotate BEOL parameters to a netlist. Hence timing variation considering BEOL variation can be simulated with SPICE. But there is no commercial EDA tools that have the functionality to extract and annotate BEOL parameters to a netlist. And this variation aware analysis is slower and more complex than corner based timing analysis.

Table 1. Conventional BEOL corners with biased parameters.

	ILD Thickness	Metal Thickness	Metal Width
Nominal	Nominal	Nominal	Nominal
Cmin	Maximum	Minimum	Minimum
Cmax	Minimum	Maximum	Maximum
RCmin	Maximum	Maximum	Maximum
RCmax	Minimum	Minimum	Minimum

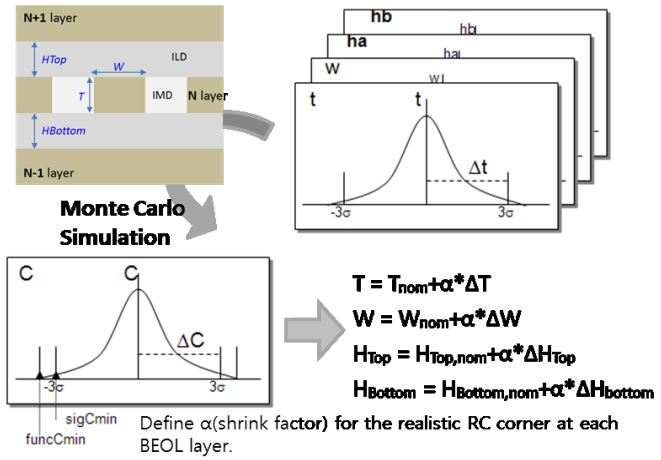

Figure 3. Illustration of tightened BEOL corner methodology.

For corner-based timing analysis, there are various studies to find optimized BEOL corner [3][10][11]. To reflect actual interconnect in silicon, Calibration of BEOL corners method is proposed using on-chip ring oscillators [7]. It contains extraction of ring-oscillator delay as function of interconnect resistance and capacitance, reflection of measured delay on that function, and methodology how BEOL corner should be modulated. However this calibration methodology is not adequate until process is mature because it calibrate based on measured silicon data.

In this study, for corner based timing analysis, a circuit-level multi-layers aware BEOL corner (CMBC) is proposed taking account of both MOL process variation and multi-BEOL layers.

II. Experiment Methodology

In this study, the circuit-level multi-layers aware BEOL corner is proposed to reduce the pessimism of conventional corner model as shown in figure 4. Two improvements are as follow:

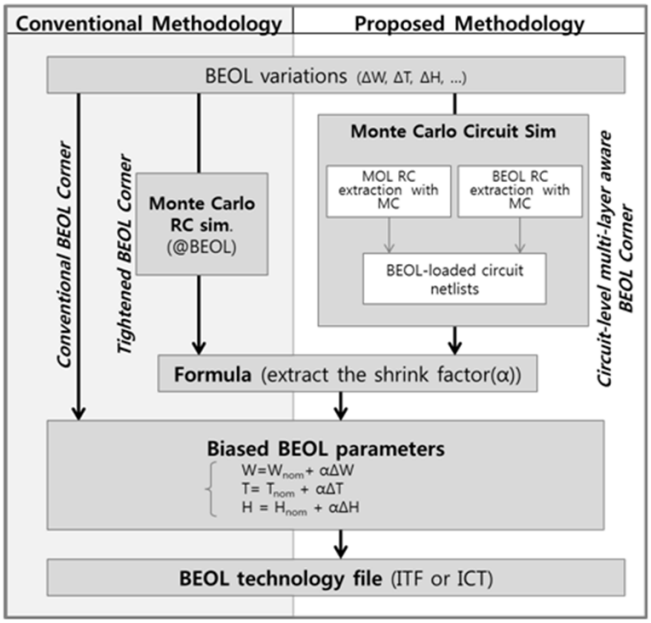

Figure 4. Comparison conventional and proposed BEOL modeling methodology.

Tightened BEOL corner model considering MOL process variation

Resistance and capacitance of MOL have a larger impact on performance in 3-D device such as FinFET and Nano-wire FET. Furthermore unlike BEOL layer which can be simplified as 2-D simple structures, MOL structure is difficult to be defined for RC extraction because there are 2 or more layers in the MOL region. Hence, 3-D field solving simulation with all process variations in MOL layers simultaneously is mandatory as shown in figure 5.

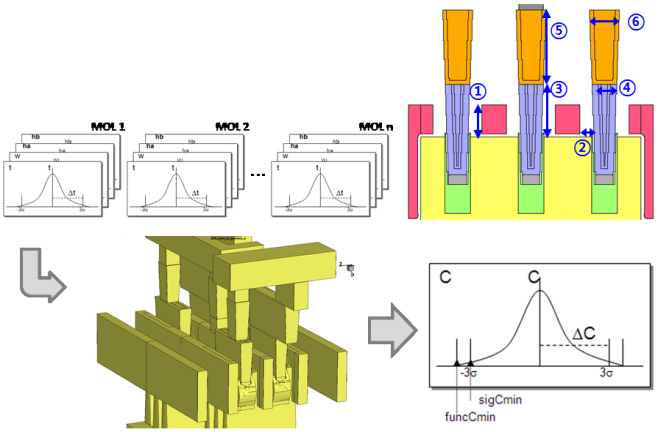

Figure 5. Illustration of profile of typical MOL stack and MOL process variation-aware corner modeling methodology.

A. BEOL corner model taking account of multi-BEOL layers

Conventional tightened BEOL corner model takes no account of multi-layer. Therefore, condition of such corner model is still pessimistic because it is very unlikely that all BEOL layers skew towards the minimum (or maximum) simultaneously. To avoid the pessimism of conventional tightened BEOL corner model, statistical method, which is based on ring-oscillator, is proposed. One-stage of ring-oscillator with fan-out 3 with loaded RC model is as shown in figure 6.

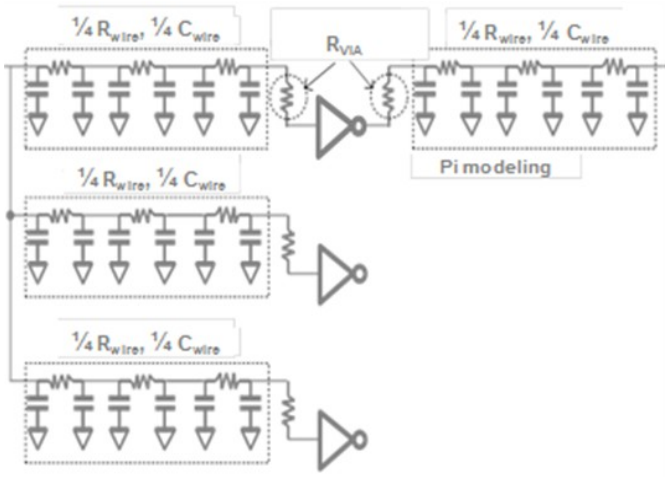

Figure 6. Illustration of 1-stage of BEOL-loaded ring-oscillator for Monte Carlo simulation.

This ring-oscillator consists of inverters with BEOL wires, which are modeled as three “pi-model”, between inverter and fan-out 3. MOL process variations are considered in inverters. BEOL wire is loaded according to the amount of usage in chip and all process variations of each layer are reflected in RC of BEOL wire as shown in figure 7.

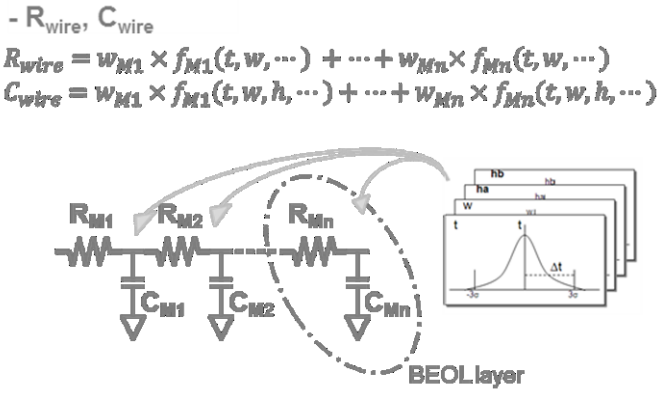

Figure 7. Illustration of multi-layer aware BEOL-loading method to reduce the pessimism of conventional BEOL corner model.

III. Result and Discussion

Figure 8 shows the RC distribution of the Monte Carlo simulation results of two difference nets using the MOL 3-D field solver. If we consider all process variations in MOL layers at the same time, from capacitance and resistance point of view, corner model can be reduced by up to 54.6% / 23.7%, respectively, compared with conventional BEOL corner. Therefore, considering all variations in MOL layer at the same time can reduce pessimistic of corner model in 3D-device architecture.

Figure 9 shows the performance of proposed ring-oscillator circuit considering both MOL process variations and multi-BEOL layers. We can observe that conventional BEOL corners are unnecessarily pessimistic. Hence, it needs unnecessary efforts of designer to meet circuit design specification. But the CMBC can reduce capacitance corner by 51.7% compared with conventional tightened BEOL corners. We can reduce chip development schedule.

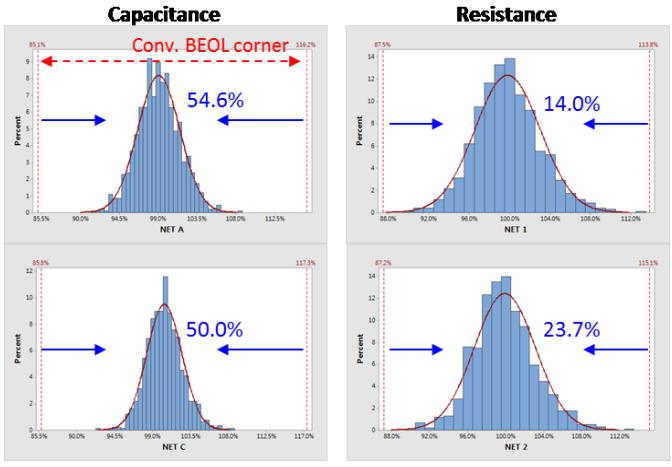

Figure 8 Histogram plot of Monte Carlo simulation result for MOL capacitance and resistance of two different net taking account of process variations.

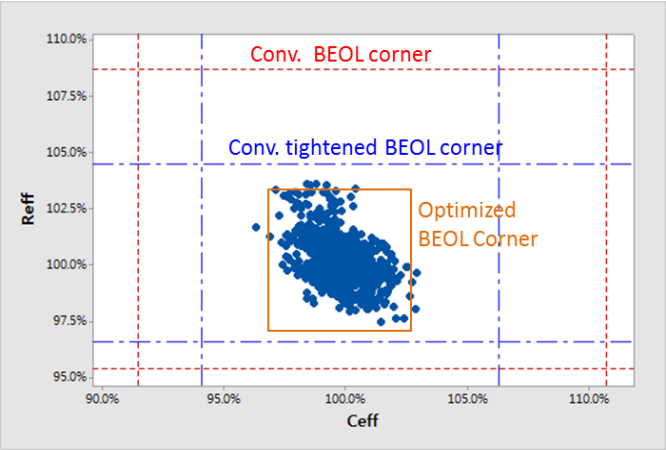

Figure 9 Histogram plot of Monte Carlo simulation result for performance of ring-oscillator considering both MOL process variation and multi-layer of BEOL

IV. Conclusion

Conventional BEOL corner definitions are no longer adequate as the impact of process variations on circuit performance. We propose the CMBC modeling methodology to take account of both MOL process variations and multi-BEOL layers. With the newly proposed method, the CMBC can reduce the capacitance orner by 51.7 % compared with the conventional tightened corner. The proposed methodology allows designers to minimize unnecessary efforts to meet circuit design specification, hence chip development schedule can be reduced.

V. Acknowledgement

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