Compact Modeling of Normally-on MOSFET Applicable for Any Technology Generations

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***Abstract*— A physics-based, compact modeling approach is applied to normally-on MOSFET, resulting to a complete description of the device internal potential distribution. The surface current and the resistive current in the neutral region are expressed as a function of the calculated potential distribution. The model is verified to reproduce total drain current as well as capacitances for different device generations. It is demonstrated that the coupling between the charge induced at the surface and that induced due to the *p*/*n* junction modify the potential distribution under different conditions, which leads to the carrier mobility modification as well.**

Keywords—compact model; depletion mode MOSFET; surface potential distribution, leakage current

I. INTRODUCTION

The MOSFET is still being intensively investigated as the main stream device. Advantages of the device are that it has been well-studied extensively and technology for the fabrication is well-established. Therefore many descendants of MOSFETs have been proposed for different purposes. The normally-on depletion-mode (DM) MOSFET shown Fig. 1 is one of the MOSFET descendants [1,2], which is frequently used for low-power applications of analog circuits requiring accurate modeling even for derivatives of current characteristics [3,4]. Many compact models have already been developed phenomenologically [5-7]. The reason for lack of accurate DM model applicable for analog circuits is due to the complicated characteristics which are very much dependent on the device structure as well as operation conditions. Thus, it is hard to reproduce all such characteristics with simple equations.

Our investigation focuses on a compact model development based on device physics to realize high accuracy. For the purpose, a complete surface-potential based modeling has been done by solving the Poisson equation in a consistent way. It is shown that the origin of the complicated device characteristics is attributed to the remaining neutral region in the buried layer, which is sensitive to the bias condition. It is shown that the characteristics can be well reproduced by use of the potential distribution solved accurately. To analyze the DM-MOSFET features, 2D-device simulation is performed, which provides microscopic origin.

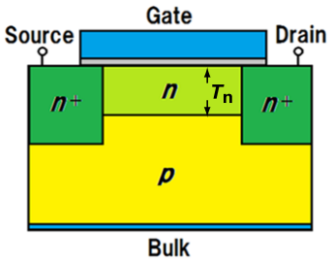

Fig. 1. Normally-on depletion-mode (DM) MOSFET cross-section.

II. CHARACTERIZATION OF DM MOSFETS

Compared to the enhancement-mode MOSFETs, there are several specific features in DM MOSFETs. Fig. 2a shows 2D-device simulation results of I_{ds}-V_{gs} characteristics for different bulk voltage V_{bs} values at drain voltage V_{ds}=0.1V. The flat-band voltage V_{fb} is verified to be nearly zero. It is seen that the current starts to flow much earlier than V_{gs}=V_{fb}, and the V_{bs} dependence is very drastic. The difficulty in modeling is, thus, the model equations must be valid for all gate voltage V_{gs} conditions, crossing V_{gs}=V_{fb}.

The threshold voltage V_{th} is studied to characterize the device features [8-9]. The GMLE (g_m-max linear extrapolation) method is applied to extract V_{th} [10]. Fig. 2b shows the g_m plot and the V_{th} extraction by the GMLE method. Two distinct contributions to the drain current I_{ds} stand clear; one is the surface current I_{acc}; which is independent of V_{bs}, and the other is I_{res}, the drain current originating from the neutral region in the buried n-layer. However, for higher V_{ds} (=5V), these two contributions cannot be distinguished separately as seen in Fig. 2c. Different from the V_{ds}=0.1V case, the V_{bs} dependence is no more locally detected but spreads over the whole V_{gs} range. For the V_{ds}=5V case, the extracted V_{th} shows very strong V_{bs} dependence as well as summarized in Table I.

Fig. 3 shows separated I_{acc} and I_{res} for studied two V_{ds} cases. For the V_{ds}=5V case, I_{res} does not saturate beyond V_{gs}=V_{fb} but shows clear V_{gs} dependence. The V_{bs} dependence of I_{res} is caused by the coupling of the gate control with the bulk control occurs, namely the fully depleted condition is created. The V_{gs} dependence of I_{res} under high V_{ds} condition is attributed to the quasi-Fermi modification according to the relationship between V_{gs} and V_{ds} as well as V_{bs}.

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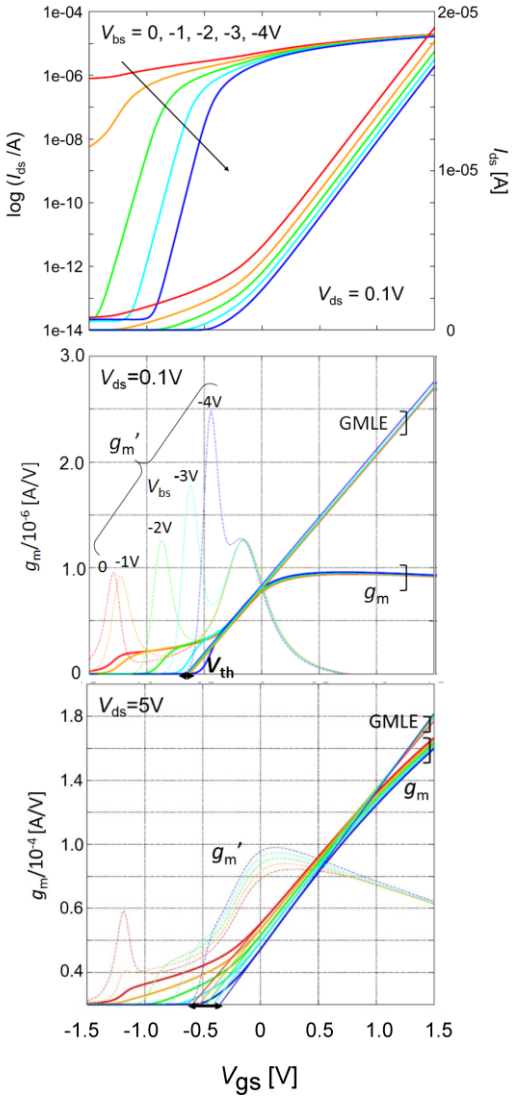

Fig. 2. 2D-device simulation results of I_{ds}-V_{gs} for different buried-layer thicknesses. Separated accumulation current I_{acc} and leakage current I_{res} are shown together for (a) V_{ds}=0.1V and (b) V_{ds}=5V.

TABLE I. EXTRACTED THRESHOLD VOLTAGE FOR TWO V_{ds} CASES

V_{bs} \ V_{th}	V_{ds}=0.1V	V_{ds}=5V
0	-0.626	-0.592
-1V	-0.630	-0.532
-2V	-0.638	-0.471
-3V	-0.651	-0.410
-4V	-0.656	-0.351

III. COMPACT MODELING OF DM MOSFETS

We have developed model equations by solving the Poisson equation, which results to a potential distribution along the depth direction as well as the channel direction. (Please refer to the equations at the end.)

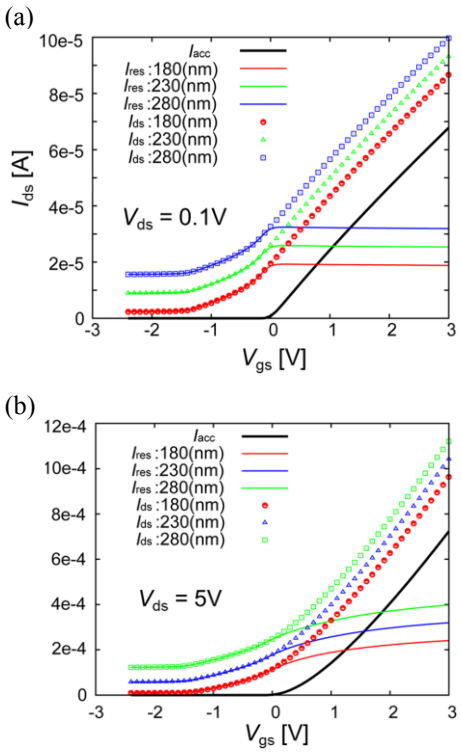

Fig. 3. 2D-device simulation results of I_{ds}-V_{gs} for different buried-layer thicknesses. Separated accumulation current I_{acc} and leakage current I_{res} are shown together for (a) V_{ds}=0.1V and (b) V_{ds}=5V at V_{bs}=0.

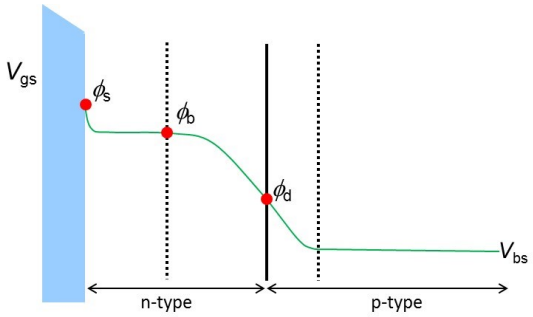

Fig. 4. Potential distribution along the depth direction where ϕ_s, ϕ_b and ϕ_d are calculated in our model with the use of the Poisson equation.

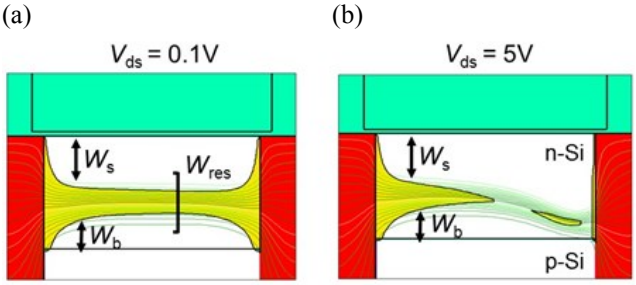

Fig. 5. Extension of depletion region from 2D-device simulation. Electron current flowlines are shonw in thin green lines at V_{gs}=-1V and V_{bs}=0 for two different V_{ds} values. Region shaded in yellow represents the neutral region where electron concentration is athe same order of the concentration.

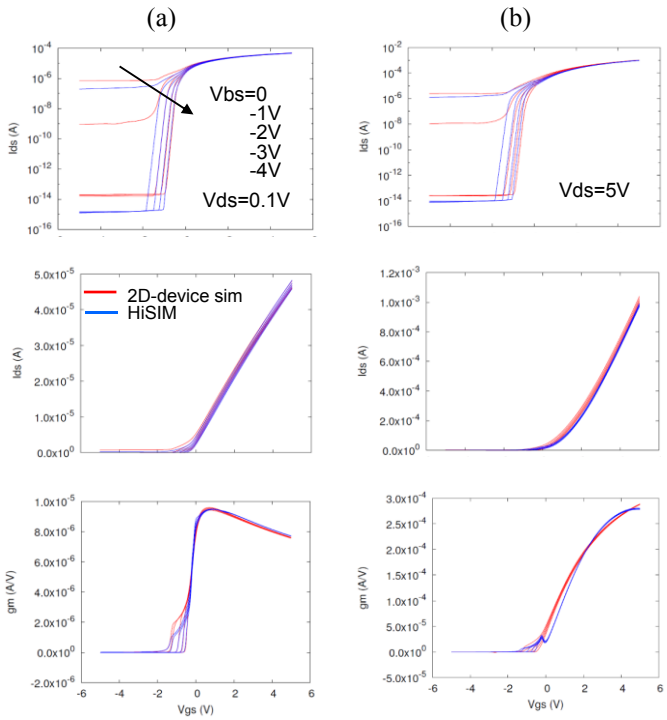

Fig. 6. I_{ds}-V_{gs} calculated by the compact model for (a) V_{ds}=0.1V and (b) V_{ds}=5V in comparison with 2D-device simulation results. V_{bs} ranges from 0 to -4V.

Fig. 4 shows the calculated potential distribution along the depth direction. The distribution describes the extension of the depletion width from the surface as well as that of the *n*/*p* junction, which are functions of ϕ_s and ϕ_b. The accumulation current I_{acc} is expressed only as a function of ϕ_s. The leakage current I_{res} flows within the neutral region shown in Fig. 5. This is written as a function of the width of the remaining neutral region W_{res} from the depletion extensions W_s and W_b, which are again functions of the potentials ϕ_s and ϕ_b. As can be seen in Fig. 5b the neutral region disappears at the drain side with increased V_{ds}. However, the carrier injection occurs from the source side, and the injected carriers flow into the drain contact by the field induced by V_{ds}. This feature is modeled by the quasi-Fermi potential, which is the solution of the Poisson equation under the saturation condition.

The low-field mobility for MOSFETs takes the universal form including Coulomb scattering, phonon scattering, and surface-roughness scattering. All three scattering mechanisms are taken into account for I_{acc} together with the saturation velocity V_{sat}. However, it is verified that the high field effect along the channel is negligible in comparison to the field induced by V_{gs}.

For the I_{res} flow, drift and diffusion contributions are considered explicitly. Modeling the drift part is done in the same way as the resistor current in HiSIM_HV [11]. The main cause for the drift current flow is the field applied between source and drain. On the contrary the origin for the current flow under low V_{ds} condition is the diffusion mechanism. Under the condition, the charges induced in the two depletion regions cause carrier scattering flowing in between, which is modeled by the electric field induced within the depletion regions.

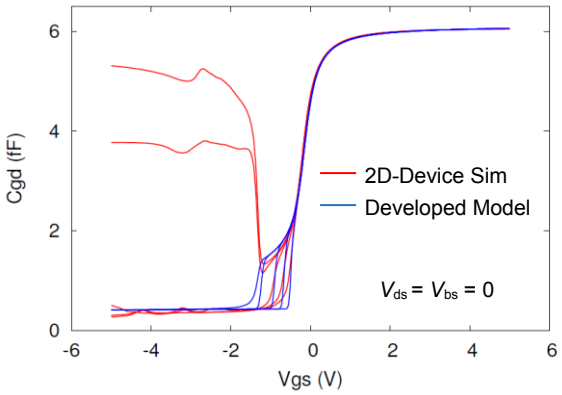

Fig. 7. C_{gd} – V_{gs} characteristics calculated by the model in comparison with 2D-device simulation results.

IV. Verification of Simulation Results

Fig. 6(a) demonstrates that calculated I_{ds} (=I_{acc}+I_{res}) characteristics reproduce 2D simulation results well at V_{ds}=0.1V. Results for the higher V_{ds} case is depicted in Fig. 6(b).

Capacitances are mostly determined by the potential values calculated by solving the Poisson equation. Thus the capacitances strongly reflect the device parameter values for describing the structure. Fig. 7 depicts calculated C_{gd} characteristics showing good reproducibility of 2D-device simulation results. The C_{gd} increase for V_{gs} < V_{fb} observed in the device simulation is due to the node connection setup of V_d and V_b nodes. To verify the robustness, the developed DM-MOSFET model is applied for different technologies. Namely, validity of the model can be proved for different generations with different buried-layer thickness T_n in Fig. 8. Comparison is shown only for C_{gg}. If T_n is thick, the depletion from the surface can never fill the layer. With reduced T_n, the coupling between the gate control and the bulk control occurs. The depletion from the *p*/*n* junction strongly influences C_{gg} especially for small V_{gs}. Therefore, C_{gg} is determined only by ϕ_s. Since the developed model is based on the potential distribution determined by the structure as well as by the bias condition applied, calculated C_{gg} characteristics reproduce the feature observed in 2D-device simulations are well reproduced.

V. Conclusion

In conclusion, we have developed a DM MOSFET model based on the surface-potential distribution by solving the Poisson equation explicitly. The coupling feature of the surface current and the resistive current in the neural region within the n-layer is considered in the model in the quasi-Fermi potential as well as in the mobility. The model verifies its applicability for wide-range of technology generations.

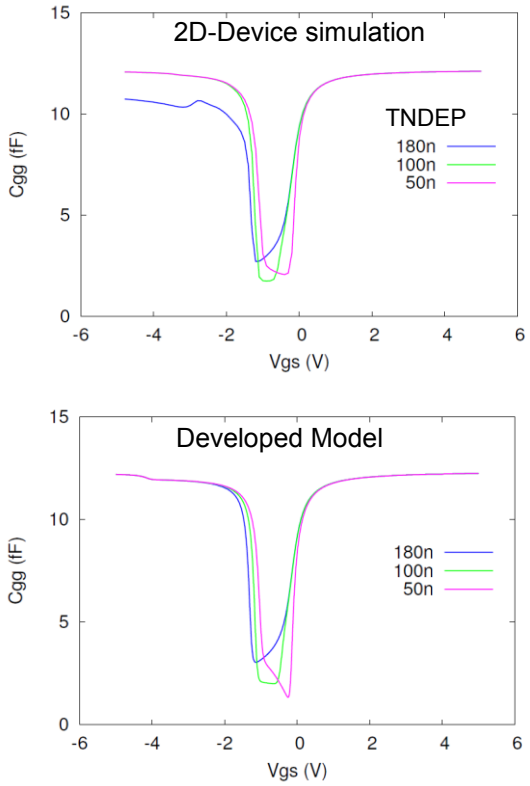

Fig. 8. Scalability for various thicknesses of the n-region (180n, 100n, 50n) is verified for the C_{gg}-V_{gs} characteristics. For the thick buried-layer thickness, the C_{gg} feature is determined by the layer. For the thin buried-layer case, it is determined by the substrate。

MODEL EQUATIONS

$$\frac{d^2\phi}{dx^2} = -\frac{\rho}{\varepsilon_s} \tag{1}$$

$$\rho = Q_s + Q_b + Q_{sub} \tag{2}$$

$$Q_s = \pm cnst0\sqrt{\exp(\Phi) - 1 - \Phi + CNT} \tag{3}$$

$$\Phi = \phi_s - \phi_b \tag{4}$$

$$CNT = cnst1\left(\exp\left(-\beta\left(\phi_s - V_{bs}\right)\right) - \exp\left(-\beta\left(\phi_b - V_{bs}\right)\right)\right) \tag{5}$$

$$Q_b = qN_{dep}\sqrt{\frac{2\varepsilon_s}{qN_{dep}}\left(\phi_b - \phi_j\right)} \tag{6}$$

$$Q_{sub} = qN_{dep}\sqrt{\frac{2\varepsilon_s}{qN_{sub}}\left(\phi_j - V_{bs} + V_{bi}\right)} \tag{7}$$

$$cnst0 = \sqrt{\frac{2\varepsilon_s \cdot q \cdot N_{dep}}{\beta}} \tag{8}$$

$$cnst1 = \frac{n_i^2}{N_{dep}^2} \tag{9}$$

where x is the device depth direction, ε_s is the permittivity of Si, q is the electron charge, N_{dep} is the impurity concentration in the buried channel, and β is the inverse of the thermal voltage. The potential value at the p/n junction is denoted by ϕ_j and the built-in potential of the junction is V_{bi}.

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