Simulation of GaN MOS capacitance with frequency dispersion and hysteresis

Koichi Fukuda, Junichi Hattori, Hidehiro Asai, Mitsuaki Shimizu
AIST
Tsukuba, Japan

Tamotsu Hashizume
Research Center for Integrated Quantum Electronics RCIQE
Hokkaido University
Sapporo, Japan

Abstract— *C-V* curves of GaN MOS capacitors are analyzed by transient-mode semiconductor device simulation. Problems of numerical convergence in the device simulation caused by the wide range time scales of the deep level trap physics are solved by a new discretization scheme of the trap formula that takes into account the dynamic change of their ionization rates. Consequently, frequency dispersions, hysteresis characteristics, and other non-ideal characteristics of *C-V* curves are stably obtained for various conditions. The present method could be a strong analysis tool, providing detail trap information when compared to a wide range of *C-V* measurements of GaN MOS capacitors. The present method is not restricted to GaN, and is applicable to MOS capacitors or other characteristics of other semiconductor materials suffering influences of the deep level traps.

Keywords—GaN; MOS; C-V; Simulation

I. INTRODUCTION

GaN MOSFET is actively studied as one of the good-candidates to build devices with speed and power beyond that of silicon technologies [1]-[4]. Although good MOS *C-V* characteristics were obtained recently [5], influences of bulk and interface deep traps in GaN MOS present numerous critical issues in general. There are many types of deep level traps; the origins of the traps are still unclear, deep level trap energy level distributions differ case by case, and so on. Therefore, from an experimental point of view, it is an urgent task to clarify and classify the origins of the non-ideal *C-V* characteristics of GaN MOS measurements, in order to realize good GaN MOS qualities for commercial applications.

To clarify or classify the origins of non-ideal *C-V* curves, it is important to compare measured curves with a theoretical approach, and the best theoretical tool is the semiconductor device simulation. However, because of wide range discrepancies in the time scales between the capacitance measurements and the carrier dynamics of the deep level traps, device simulations often cause convergence problems in their Newton iterations. In this work, such convergence problems in capacitance simulations with deep traps are overcome by a transient mode approach, with a modification to the discretization scheme of the deep-level trap formulation.

In this paper, the present simulation method is explained in section II. In section III, simple cases of *C-V* curves influenced by the deep-level traps are presented. In section IV, more complicated cases are discussed, followed by some conclusions.

II. SIMULATION METHOD

An issue of the deep trap modeling in device simulation is related to AC analysis. Normally device capacitances are obtained by small signal analyses based on a semi-steady-state formulation of the AC analysis mode. This conventional approach cannot be applied to deep trap cases because the time scales of the trap dynamics differ from those of free carriers. Furthermore, trap charges are incorporated as a time-dependent term in the right hand side of the Poisson's equation, which has no time-dependent term, in general. In the present approach, however, *C-V* characteristics are obtained by a transient analysis technique where not only capacitance measurements but also voltage bias sweeps are continuously simulated with time steps as shown in Fig. 1.

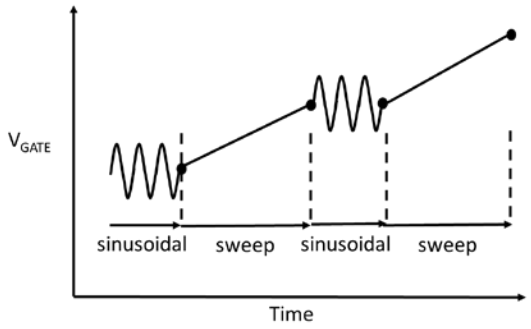

Fig. 1. A schematic of the present method used in the *C-V* simulation. Both sinusoidal voltage signals for the capacitance measurements and the voltage sweeps to the next bias steps are treated by the transient analysis waveform. Thus, all the carrier and the trap dynamics are included in the simulation.

Another issue is the time steps of the transient simulation. Different time scales between the frequencies of the capacitance measurements, voltage sweeps, and the time scales of various deep-level traps should be consistently handled in each simulation. Taking an acceptor type trap for an example, transient behavior of ionized trap density is governed by (1).

$$\partial N_{TA}^{-}/\partial t = E_n \cdot N_{TA}^{-} - C_n \cdot n \cdot (N_{TA} - N_{TA}^{-}) + E_p \cdot (N_{TA} - N_{TA}^{-}) - C_p \cdot p \cdot N_{TA}^{-} \quad (1)$$

In (1), N_{TA} is a total acceptor trap density, N_{TA}^{-} is an ionized trap density, E_n and E_p are electron and hole emission rates of the trap, C_n and C_p are electron and hole capture rates, and n and p are electron and hole concentrations respectively. Because of the depth of the trap energy level, these emission

rates E_n and E_p are much slower than the normal carrier dynamics by several orders of magnitude.

Physical image of this equation is shown in Fig. 2. If long time steps are applied to (1), the generation-recombination (GR) rates change during one time step. These GR terms of the ionized traps directly correspond to the GR terms of the electrons and holes. The device simulator requires constant carrier GR rates for each time step. In the present approach, (1) is solved in time domain, and not the initial GR rates, but the average effective GR rates during the time steps are used for each device simulation time step. This modified method allows much longer time steps to be used in obtaining good convergences of *C-V* simulations.

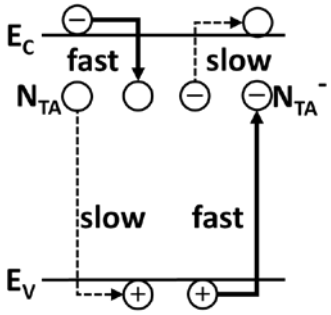

Fig. 2. Trap-detrap behaviors of the acceptor-type traps. The trap level is below the conduction band minimum, and electrons are fastly trapped to make negatively ionized traps. Electron emission processes are slow for their thermal energies to get rid of the trap energy depth.

III. Simulation of *C-V* Curves

The present model is implemented into the three-dimensional technology CAD (TCAD) system HyENEXSS [6] through its physical model API. By using the physical model API, HyENEXSS easily incorporates new physical models and equations. Once the models have been implemented, the simulator enables the device simulation of complicated device structures including non-orthogonal cases. Even the device-circuit mixed mode analyses are possible on the user-defined physics.

A simple MOS capacitor in Fig. 3 is assumed in the following simulation examples.

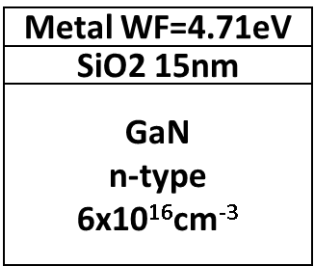

Fig. 3. A MOS capacitor assumed in the simulation examples. The substrate is n-type, the insulator is 15 nm thick, and the gate workfunction is assumed to be 4.71 eV. The interface traps are assumed to be on the GaN / insulator interface.

Fig.4 shows obtained *C-V* simulation results for several trap density levels, 0, 10^{11}, 10^{12}, 3×10^{12}, and 10^{13} cm^{-3}, of the acceptor type interface traps at 0.4 eV deep from the conduction band minimum. The *C-V* frequency 3 MHz is faster than the time scale of the trap energy depth, and the sweep speed 10 μs / bias point is slower. In the cases with trap densities more than 10^{12} cm^{-3}, so-called "*C-V* plateau" is clearly observed. On the other hand, no hysteresis characteristics are observed while the gate bias is swept in both positive and negative directions. This comes from the slow sweep speed compared with characteristic time scale of 0.4 eV in the room temperature.

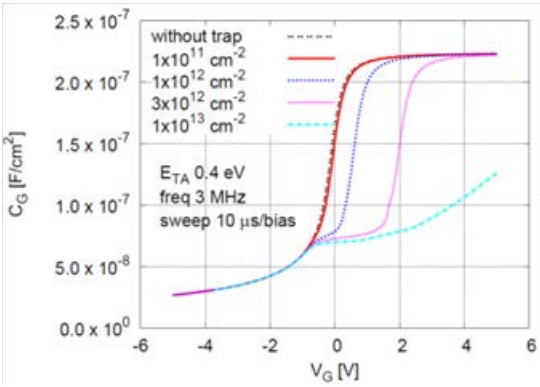

Fig. 4. Simulated *C-V* curves by the present method. "Plateau" of *C-V* curves can be seen as commonly observed in GaN MOS measurements.

In these plateau regions, the band potential bending is blocked by the interface trap charge. Fig. 5 shows the potential depth profile near the interface, and the concentration of ionized interface traps, as an example case of the trap density 10^{12} cm^{-3}. In this figure, the ionized trap density is changed from the gate voltage of -1.0 to +0.4 V, which is the plateau-range of the *C-V* curve. This trap charge prevents the gate electric field from accumulating carriers at the MOS surface. The present method enables the quick understanding of the complicated physics related to the deep-level traps.

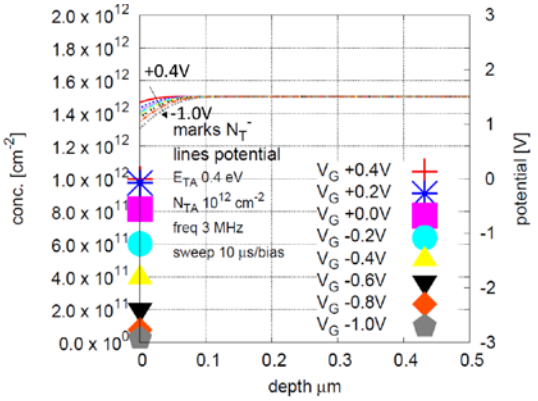

Fig. 5. Band bending of the MOS capacitor in Fig. 4 with 10^{12}cm-2 traps. Ionized trap density changes for the gate biases in the plateau-range from -1 to +0.4 V. This charge delays the creation of electron accumulation layer at the MOS surface.

Charged trap density around the gate bias of 0 V is shown in Fig. 6, where the solid line shows the ionized trap density N_T^- in the left axis, and the dashed line shows the electron concentration in the right axis. The time shift between the electrons and the ionized traps, both are negative charges, are observed. The electron peaks correspond to the timing of the trap charge increase. Thus, dynamics of the MOS capacitor including the behaviors of the trap and the electron can be understood visually in the present method.

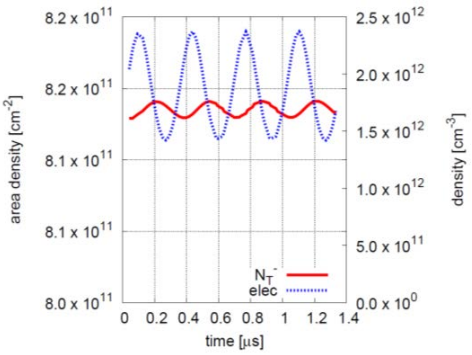

Fig. 6. Charge distributions during the *C-V* simulation of the MOS capacitor in Fig. 4 with 10^{12} cm^{-2} traps for the gate bias of 0 V. Ionized trap area density N_T^- (solid line) corresponds to the left axis and electron density (dashed line) to the right axis.

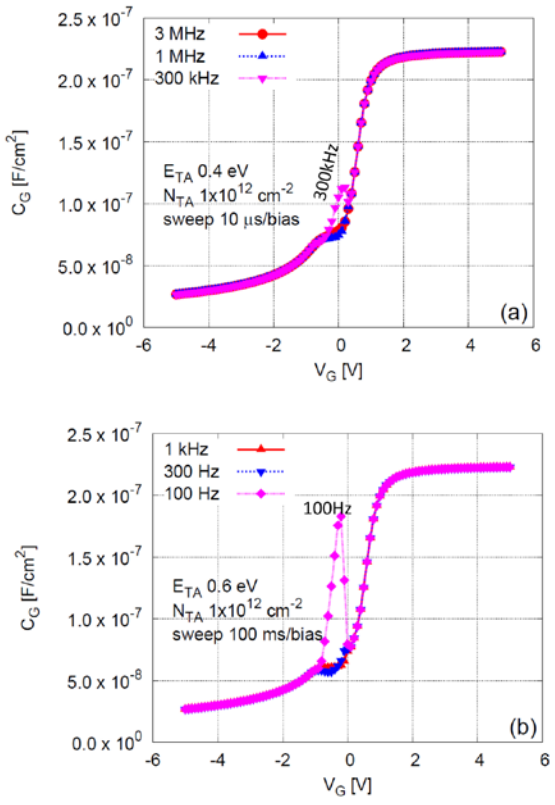

Fig. 7. Frequency dependent *C-V* characteristics for interface trap density of 10^{12}/cm^2. (a) is for 0.4 eV depth traps from the conduction band, and (b) is for 0.6 eV.

Frequency dispersions of *C-V* curves for 0.4 eV deep traps are shown in Fig. 7 (a). Measurement of this dispersion is important to characterize deep interface traps in the fabricated capacitors. The effect of the deep-level trap is observed at low frequencies. Fig. 7 (b) is for 0.6 eV deep traps and frequency dispersion is observed at lower frequencies, such as 100 Hz. Such quantitative insights are also easily obtained by the present method.

When the bias sweep speed is high, hysteresis characteristics are observed, as shown in Fig. 8. In this figure, the trap energy depth is 0.5 eV and the sweep speed is 100 μs / bias point which is faster than the time scale of the 0.5 eV trap. Hysteresis is observed under electron depletion conditions with the electrons remaining in the traps for a negative bias sweep, but the electrons are easily captured by the traps during a positive bias sweep.

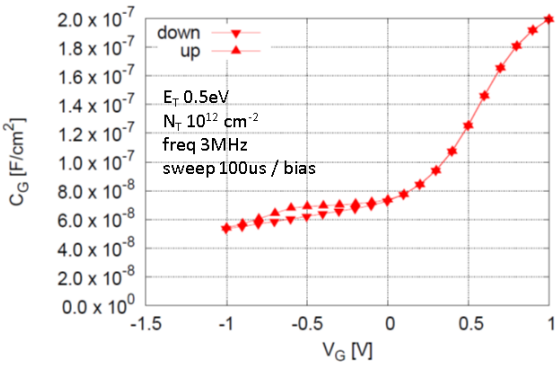

Fig. 8. Hysteresis characteristics for interface trap density of 10^{12}/cm^2 and trap energy of 0.5 eV.

In Figs. 4, 7, and 8, fundamental non-ideal *C-V* characteristics of the GaN MOS capacitors, "*C-V* plateau," frequency dispersions, and hysteresis, are successfully described by the present transient-mode method. Because of the nature of semiconductor device simulation, transient behaviors of carriers and traps behind such non-ideal *C-V* characteristics can be understood by observing the internal distributions of them, as in Figs. 5 and 6. Consequently, the present method is proven to be the stronger tool in investigating the physics of GaN MOS capacitors, both quantitatively and visually.

IV. Complicated and Realistic Cases

The examples discussed in the last section are very simple cases, which focus on each physical aspect of the *C-V* characteristics or on the energy of each trap. However, fabricated MOS capacitors and their *C-V* measurements include much more complicated phenomena arising from the combinations of several traps. Because of such combinations of plural traps, it is very hard to distinguish them without the support of theoretical and quantitative tools. Although more sophisticated measurements such as the deep level transient spectroscopy (DLTS) are often used to distinguish multiple traps, the technique has still limitations in terms of device size, energy depth, and careful measurements. Therefore the *C-V*

measurement is an important and practical tool in developing good MOS capacitors. The applicability of the present method in such realistic *C-V* cases is discussed in this section.

Effects of the trap energy distribution are shown in Fig. 9, where the trap energy peak is at 0.3 eV and the standard deviation of energy is treated as a parameter. The frequency for the capacitance measurements is 100 MHz, which is faster than the specific time scale of 0.3 eV at room temperature. As the standard deviation increases, the frequency dispersion peaks are observed, as shown in Fig. 7. These peaks are from the shallower energy part of the traps. Compared with Fig. 7, more capacitance values are observed between the dispersion peak and the accumulation capacitance. This is the effect of the trap energy distribution. Thus, *C-V* curves include information from trap energy distributions, which are successfully obtained by the present method.

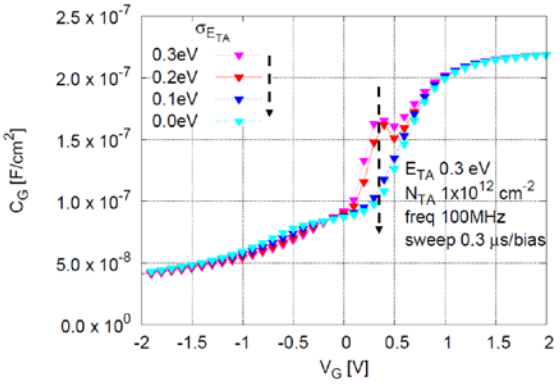

Fig. 9. *C-V* curves dependent on energy standard deviation. The energy peak is at 0.3 eV, and the energy standard deviation $\sigma(E_{TA})$ is the parameter.

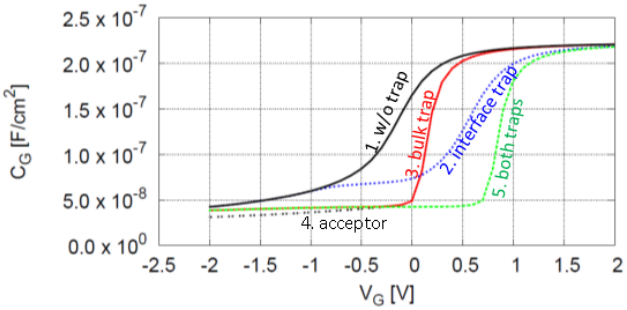

Fig. 10. Comparison of 5 cases, 1: no trap, 2: interface trap, 3: bulk trap (depth 0.1um), 4: acceptor (depth 0.1um), and 5: both traps. Although area density of the case 2 and 3 is identical, two curves are different. The bulk trap case 3 is similar to the acceptor case.

More complicated cases, which include both interface and bulk traps, and bulk traps are distributed only in the limited depth assuming implantation damages are simulated as shown in Fig. 10. In case 2, with the interface trap, and case 3, with the bulk trap, the total trap area densities are identical. Because of the 1 µm depth distribution of the bulk trap, case 3 is quite similar to case 4, with a simple acceptor with the same distribution.

Thus, the present method is a powerful modeling tool to study more complex and realistic trap phenomena. Finally, it should be mentioned that this approach is also applicable to other semiconductor MOS capacitors and to the *I-V* characteristics of MOSFETs.

V. Conclusions

The transient-based device simulation method, with a modification to discretization method, succeeds in obtaining GaN MOSFET *C-V* characteristics with frequency dispersions and hysteresis characteristics. The method can be used to obtain trap information from measured characteristics. This could be an important tool to realize future GaN MOS-based devices. The present method itself is not limited to GaN and can be applied to MOS capacitors of any materials.

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References

[1] K. S. Im, J. B. Ha, K. W. Kim, J. S. Lee, D. S. Kim, S. H. Hahm, and J. H. Lee, “Normally off GaN MOSFET based on AlGaN/GaN heterostructure with extremely high 2DEG density grown on silicon substrate,” IEEE Electron Device Letters, vol. 31, no. 3, pp. 192-194, 2010.

[2] W. Huang, T. Khan and T. P. Chow, “Enhancement-Mode n-Channel GaN MOSFETs on p and n-GaN/Sapphire Substrates,” IEEE Electron Device Letters, vol. 27, no. 10, pp. 796-798, 2006.

[3] C. Y. Tsai, T. L. Wu and A. Chin, “High-Performance GaN MOSFET With High-κ LaAlO3/SiO2 Gate Dielectric," in IEEE Electron Device Letters, vol. 33, no. 1, pp. 35-37, 2012.

[4] A. Sunny, and S. S. Chauhan, “Thermal and threshold voltage analysis of GaN MOSFET with AlGaN/GaN heterostructure,” International Conference on Communication and Signal Processing (ICCSP), IEEE, pp. 1218-1221, 2016.

[5] S. Kaneki, J. Ohira, S. Toiya, Z. Yatabe, J. T. Asubar, and T. Hashizume, “Highly-stable and low-state-density Al2O3/GaN interfaces using epitaxial n-GaN layers grown on free-standing GaN substrates,” Applied Physics Letters, vol. 109, no. 16, p. 162104, 2016.

[6] HyENEXSS