Analysis of Screening Effects in Multiple-Gate and Gate-All-Around Si NW array FETs

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I. ABSTRACT

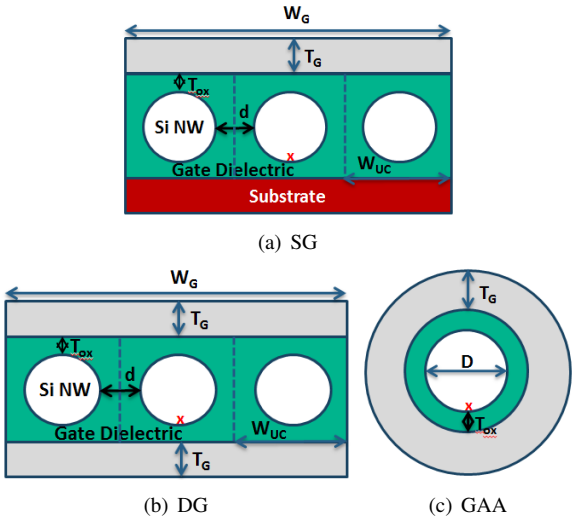
The performance of Silicon nanowire (NW) FETs with multiple parallel cylinderical channels can significantly be affected by screening effects depending on the gate structure. This work analyzes electrostatic screening effects in single gate (SG) and double gate (DG) structures and compares the related transistor performance to gate-all-around (GAA) Si nanowire (NW) FET structures. As a measure for screening effects, the current density per gate width is studied for the above mentioned structures and the results are discussed for different distances between the channels in SG and DG structures. The impact of screening effects on the transit frequency (f_{T}) of the SG, DG and GAA structures is evaluated based on a small-signal frequency dependent analysis. It is shown that the screening effect varies significantly not only with the distance between Si NWs (possible number of channels) but also with the device structure (SG and DG Si NW FETs).

II. INTRODUCTION

Circuit applications typically demand currents larger than the current carried by a single nanowire (NW). To reduce the overall footprint of the transistor, the NWs are commonly as closely packed as the design rules allow. With the down-scaling of all transistor dimensions, the distance d between the NWs will also shrink and electrostatic interaction between the NWs will start to significantly affect the overall transistor performance due to mutual screening effects. The latter depends on the device architecture.

We consider three gate configurations for Si NW FETs. Based on 3D numerical device simulations screening effects in single gate (SG) and double gate (DG) Si NW field effect transistors (FETs) are studied and important transistor figures-of-merit are compared with those of a gate-all-around (GAA) device architecture (see Fig. 1). Identical parallel Si NWs are assumed in an array with different channel density controlled by the distance d between the NWs. The GAA single Si NW FET has been considered as an ideal and reference device with high DC performance and no screening effect due to the gate shielding and ideal control.

Screening effects have already been studied by several authors but have mainly focused on an analytical model for the effective gate capacitance in Si NW arrays [1] and Carbon nanotube FETs [2], [3], [4], [5]. However, a detailed analysis for Si NW arrays regarding the implication for DC and AC device characteristics to offer insights for device design is missing.



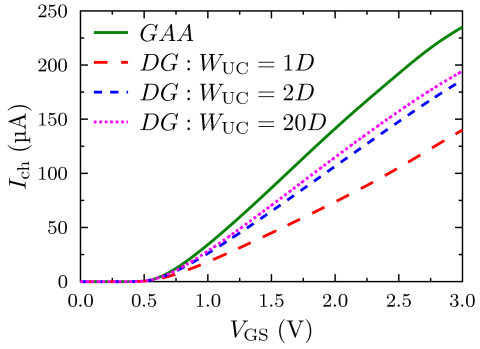
(a) SG (b) DG (c) GAA

Fig. 1: Schematic cross-section of a **(a)** SG FET, **(b)** DG FET and **(c)** GAA FET.

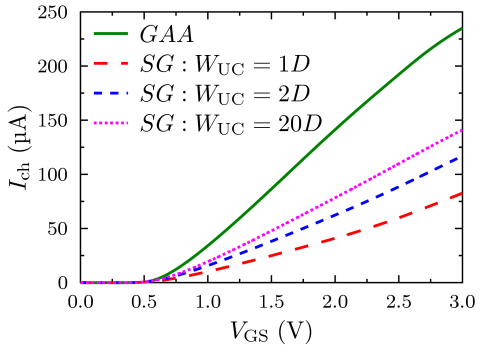
III. STRUCTURES, RESULTS AND DISCUSIONS

The simulated devices have a Si NW diameter D of $12\,\mathrm{nm}$, a channel length L_{ch} of $90\,\mathrm{nm}$, an oxide thickness T_{ox} of $1.8\,\mathrm{nm}$ and $6\,\mathrm{nm}$ respectively, a gate thickness T_{G} of $30\,\mathrm{nm}$ and d ranging from 0 to $20D$. The contact regions are highly doped in order to suppress contact related effects. The $90\,\mathrm{nm}$ channel length represents a sweet spot for radio-frequency applications. Drift-diffusion transport and surface scattering are considered in the simulations while quantization effects are neglected due to the relatively large D.

To reduce the simulation time, a single unit cell with a width of $W_{\mathrm{UC}} = D + d$ for SG and DG structures (see Fig. 1) and a width of $D + 2T_{\mathrm{ox}} + T_{\mathrm{G}}$ for the GAA structure were simulated with symmetry boundary conditions at the simulation domain boundaries of the unit cell. This captures the electrostatics in homogenous NW arrays and thus the screening effects.

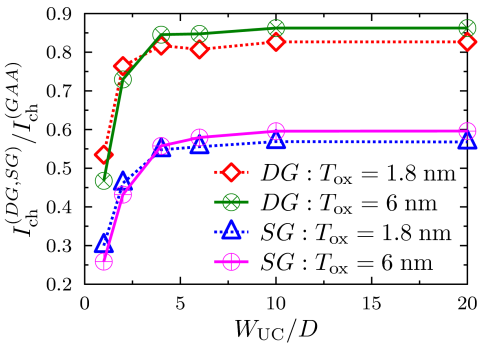


(a) DG Si NW FET

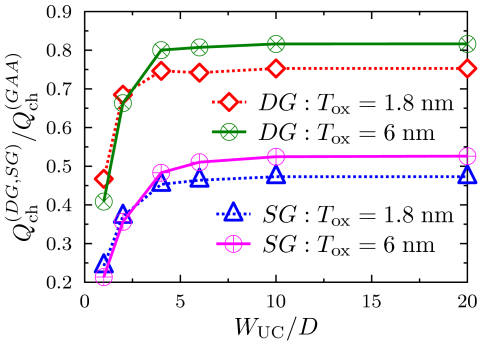


(b) SG Si NW FET

Fig. 2: Simulated transfer characteristics of single channel with different unit cells (see legend) for **(a)** DG Si NW FET and **(b)** SG Si NW FET compared to the GAA Si NW FET with the same dimensions at T_{ox} of 1.8 nm and $V_{\mathrm{DS}} = 1\,\mathrm{V}$.



(a) channel current



(b) channel charge

Fig. 3: **(a)** channel current and **(b)** channel charge of a SG and DG FET normalized to the current and channel charge of the GAA FET with the same dimensions at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 1\,\mathrm{V}$.

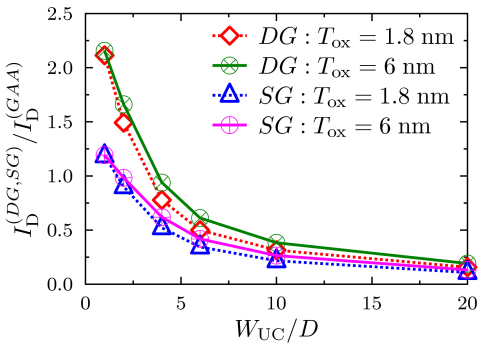
Fig. 2 shows the simulated transfer characteristics of a single channel of DG and SG structures for different unit cell widths compared to the GAA structure at T_{ox} of 1.8 nm and $V_{\mathrm{DS}} = 1\,\mathrm{V}$. When decreasing the unit cell width, the current per single channel (see Fig. 2) of the SG and DG structures decreases due to screening while the corresponding increase in channel density results in an increase of the current per gate width in an NW array. Hence, the question is at which NW density the screening by neighboring channels does not lead anymore to an increase of current per gate width with increasing NW density. In the simulation results discussed below, the current I_{GAA} and the charge Q_{GAA} of the GAA structure are taken as a reference.

Fig. 3 shows the current ratio I/I_{GAA} and the charge ratio Q/Q_{GAA} of the SG and DG structures for a single channel versus W_{UC}/D at $V_{\mathrm{DS}} = V_{\mathrm{GS}} = 1\,\mathrm{V}$. Both are normalized to the current and the charge of the GAA structure, respectively, and indicate that the critical unit cell width W_{crit} is about $4D$. Dropping d in NW arrays below $3D$ causes screening effects to decrease the single channel current and channel charge up to 30 %. Above W_{crit}, screening effects due to the electrostatic interaction between the NWs become negligible.

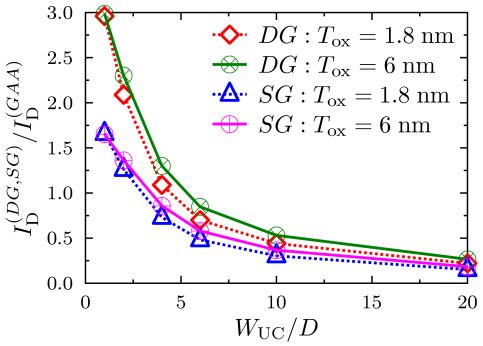
Evaluating the current per gate width in NW array FETs reveals another interesting aspect. Assuming the above mentioned dimensions and an oxide thickness T_{ox} of 6 nm, the NW density N_{GAA} in GAA architecture would be about 18 NWs/µm and would further decrease to 13 NWs/µm if T_{G} is increased from 30 nm to 50 nm.

Assuming a unit cell width of $1D$, $2D$ or $4D$ (i.e. below and up to W_{crit} for the SG and DG architectures) results in a channel density n_{ch} of 83, 41 or 20 NWs/µm independent of T_{ox} and T_{G}. Thus, even if the current per NW in a SG and DG FET is smaller compared to the current of a GAA architecture (see Fig. 2) and even if the current is affected by screening effects, the current per gate width, which is the essential figure of merit for circuit applications can be much larger in SG and DG architectures due to the much higher packing density.

Decreasing the distance d between the NWs for a given device area increases the number of channels n_{ch} and drive current of the device (Fig. 4) regardless of the reduction of the single channel current due to screening (Fig. 2). Therefore, the simulation results show that it is reasonable to decrease the distance between the channels as much as technology allows in order to increase the number of channels and accordingly the current density for a given area.

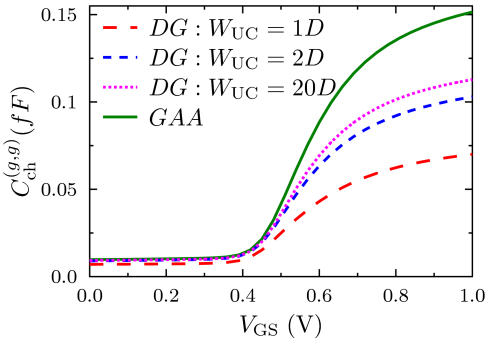


(a) current density at $T_G = 30$ nm

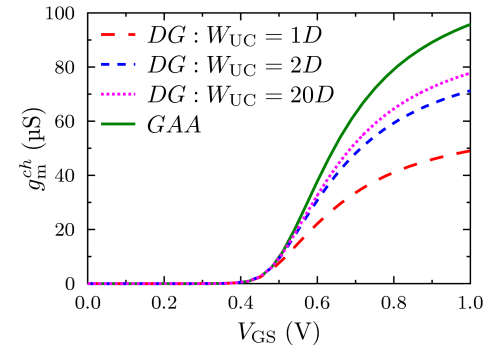


(b) current density at $T_G = 50$ nm

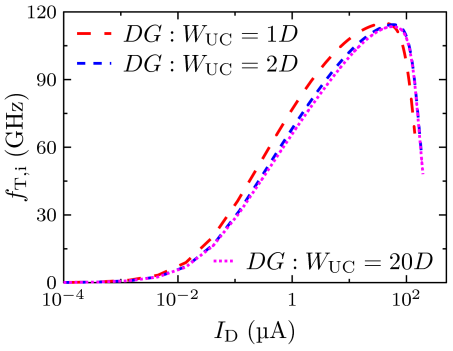
Fig. 4: Current density of a SG and DG FET normalized to the current density of the GAA FET with the same dimensions at **(a)** $T_G = 30$ nm and **(b)** $T_G = 50$ nm.



(a) gate capacitance



(b) transconductance



(c) intrinsic transit frequency

Fig. 5: Simulated **(a)** gate capacitance, **(b)** transconductance and **(a)** intrinsic transit frequency $f_{T,i}$ of a single channel with different unit cells (see legend) of DG compared to the GAA Si NW FET with the same dimensions at T_{ox} of 1.8 nm and $V_{DS} = 1$ V.

The I_{on}/I_{off} ratios of the transistors with a channel length of 90 nm are slightly affected by the gate structure mostly by an increase of I_{off}. It decreses by two orders of magnitude from 1e10 for the GAA structure to 1e8 for the SG structure. However, for the 20 nm channel length I_{off} increases drastically due to short channel effects which could partially be compensated by a reduction of wire diameter.

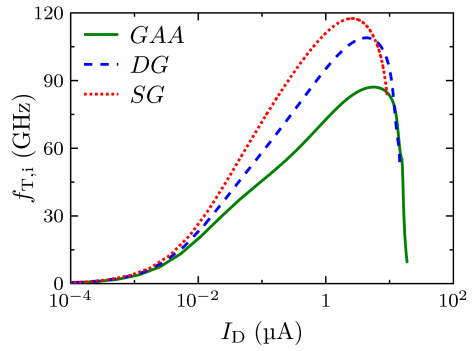
The device speed is another interesting figure of merit to be discussed with the number of channels and screening in an NW FET array. Smaller channel distance suffer stronger screening in the gate region due to limited available area for the electric field termination thus resulting in reduced gate capacitance as well as transconductance of a single channel as shown in Fig. 5(a),(b). In fact, the transit frequency f_T of a single channel depends only weakly on the distance d between the NWs and thus the number of channels per gate (cf. Fig. 5(c)).

In general, the extrinsic transit frequency f_T of an array is defined as:

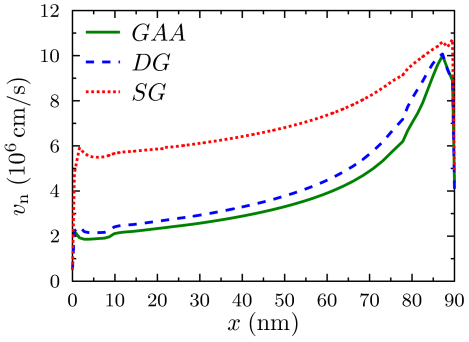
$$f_T = \frac{n_{ch}.g_m^{ch}}{n_{ch}.C_{ch}^{(g,g)} + C_{Par}}, \quad (1)$$

where n_{ch} is the number of channels in a given area, g_m^{ch} is the transconductance of a single channel, $C_{ch}^{(g,g)}$ is the gate capacitance of a single channel and C_{Par} is the parasitic capacitance.

As the number of channels n_{ch} increases, the influence of the parasitic capacitance decreases thus resulting in a higher extrinsic transit frequency f_T. In fact, a closely spaced

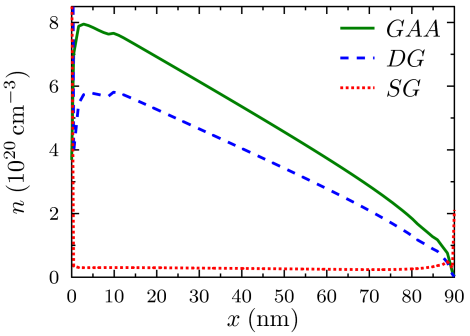


(a) intrinsic transit frequency

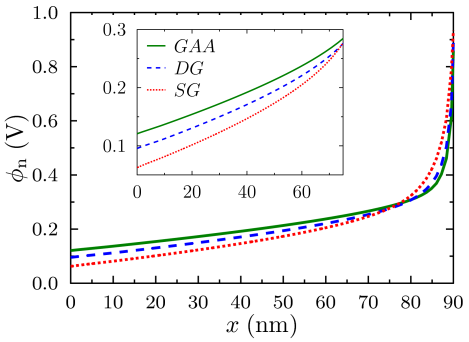


(b) electron velocity

Fig. 6: **(a)** Intrinsic transit frequency $f_{T,i}$ and **(b)** electron velocity v_n along the channel at the interface to the gate oxide and to the substrate of a GAA, DG and SG FET (see the crosses in Fig. 1) at $W_{UC} = 2D$ and $V_{DS} = V_{GS} = 1\,V$.



(a) electron density



(b) quasi-Fermi potential

Fig. 7: **(a)** Electron density n and **(b)** quasi-Fermi potential φ_n (Inset shows zoom in) along the channel at the interface of a GAA, DG and SG FET (see the crosses in Fig. 1) at $W_{UC} = 2D$ and $V_{DS} = V_{GS} = 1\,V$.

channels in a given area (a large collection of channels in an array configuration) is attractive as it improves not only the drive current of the array but also the device speed. To evaluate the device speed accurately, it is necessary to include the parasitic capacitance which is out of the scope of this work.

Fig. 6 compares the intrinsic transit frequency $f_{T,i}$ and electron velocity v_n along the channel of SG, DG and GAA Si NW FETs. Surprisingly, the $f_{T,i}$ of the SG structure is about 30 % larger than $f_{T,i}$ of the GAA structure which is typically assumed to be the ideal device structure.

The performance gain in the SG architecture can be explained by the electron density n and the quasi fermi potential φ_n along the channel as shown in Fig. 7. φ_n of the SG structure has a larger gradient along the channel. Since in the employed drift-diffusion model the electron velocity depends on the gradient of φ_n, the carriers are faster in the SG FET leading to a higher $f_{T,i}$. In fact, in a GAA structure, the band edges are almost flat due to the excellent gate control. Thus the gradient of the band edges is small as well as the carrier velocity.

IV. Conclusions

The screening effect of multiple conducting Si NW channels has been analyzed based on 3D TCAD simulations for SG, DG and GAA devices. These analyses give insights into the Si NW device performance in terms of channel density. The simulation results show that from the device DC and AC performance point of view, it is reasonable to decrease the distance between the channels as much as possible. A large channel density in a NW FET array configuration is attractive and improves the drive current of the array andthus also the extrinsic device speed.

The intrinsic f_T of the SG structure with single channel is larger than the intrinsic $f_{T,i}$ of the GAA structure with a single channel. This counterintuitive result is a consequence of a higher drift field in the channel of the SG structure due to a weaker gate control there.

References

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