A Computationally Efficient Compact Model for Leakage in Cross-point Array

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***Abstract*—Cross-point architecture, while being appealing in consideration of high integration density, suffers from leakage through sneak paths across the array. The leakage current flowing through half-accessed and in some cases, unaccessed cells (and the corresponding leakage power) are important determinants of array performance. Proper estimation of these components is computationally challenging and often demands rigorous simulation efforts. This paper presents a computationally efficient compact model to assess the leakage in cross-point array employing threshold switch selectors. We provide closed form mathematical expressions that govern our model and explain the derivation methodologies. We analyze and verify the validity of the model by cross-checking with results from conventional rigorous array simulations. The model shows excellent matching (~99% accuracy) with rigorous simulations for different array sizes (16×16 through 256×256). The model has been tested with various ranges of *selector* OFF resistance (0.1 MΩ to 1 GΩ), interconnect resistance (1 mΩ/□ to 10 Ω/□) and access voltage (0.2V to 1V). The test results from the model show accurate response in comparison with those obtained from intensive array simulations.**

Keywords— array leakage; cross-point architecture; half-accessed cells; interconnect; magnetic tunnel junction; metal-insulator transition; selector.

I. INTRODUCTION

Humungous growth in digital data from a multitude of sources necessitates reliable and robust memory storage. Through decades of innovation and evolution, several types of memory technologies and architectures have been engineered. With an advent of systems demanding tight power budget such as mobile/wearable electronics, energy scavenging systems and implantable devices significant interest has been drawn towards non-volatile memory technologies, which allow complete shut-down of power supply in stand-by mode [1]. In addition to *zero* stand-by leakage, such memories offer a promise of high integration density. However, standard memory architectures [2] cannot harness the full density benefits offered by non-volatile memory devices due to a much larger footprint of the access transistor and the contact pitches required in a three-terminal cell design [3]. Cross-point array architecture [4] is a cutting-edge technique to pack memory cells in a smaller area. In this architecture, memory cells are sandwiched between two orthogonally running metal lines, named- word lines (WL) and bit lines (BL) (Fig. 1(a)). The cell footprint significantly reduces since the use of access transistor is averted and the number of terminals in the memory cell is reduced to 2. In place of access transistors, *selector* [4] devices with extremely non-linear *I-V* behavior are used to selectively access the memory elements [5]. These *selectors* exhibit very high resistance below a critical voltage and thereby suppress current through the unaccessed memory cells. On the contrary, *selectors* are driven into low resistive state during read/write access of accessed cells. Special biasing schemes (*V/2* and *V/3*-Fig. 1 (b) [5]) are implemented to provide sufficient voltage across the cells to be accessed and lowest possible voltage across all other cells. However, due to presence of sneak paths, the conventional biasing schemes of cross-point array generate leakage current through the half-accessed row (HAR), half-accessed column (HAC) and even through un-accessed (UA) cells (in case of *V/3* biasing). These leakage components contribute to power drainage and reduce robustness of current sensing during read operation [5]. Hence, accurate modeling and prediction of the array leakage is extremely important. However, the conventional process [6, 7] to calculate array leakage requires extensive computational effort as the entire array needs to be simulated for sufficiently accurate estimation. *In this work, we present a compact model that performs accurate computation of array leakage without simulating the entire array*. *The model is valid for designs that use threshold-switches [8] as selector elements. We implement different sizes of cross-point array in SPICE simulator and run rigorous simulation to obtain leakage current and power. We then cross-check the obtained results with those calculated from our compact model and prove the validity of our approach. We also evaluate the accuracy of the model for different selector resistance, interconnect resistance and access voltages.*

II. MODELING METHODOLOGY

As mentioned before, our compact model for leakage is suited to be used for arrays with *threshold switch* type

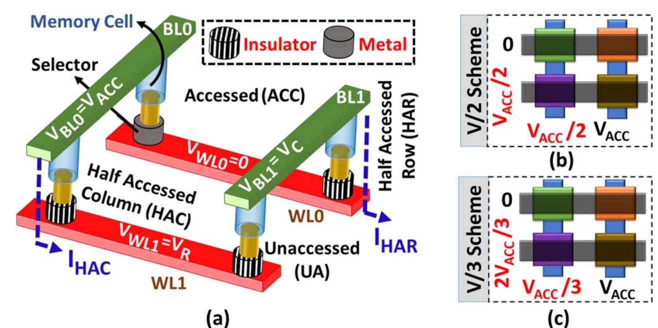

Fig. 1: (a) Typical cross-point memory array structures. Scenario of two types of schemes – (b) *V/2* and (c) *V/3* used for biasing a cross-point array. V_{ACC} represents read/write voltage.

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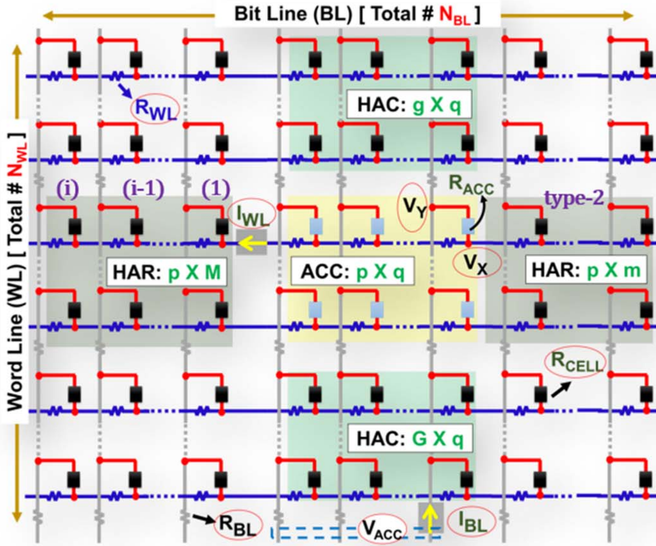

$$I_{HAR} = (p/R_{CELL})[(M/N)V_{ACC} - (I_{WL}R_{WL})M(M+1)/2 + m.(V_{ACC}/N - V_X)]$$

$$I_{HAC} = (q/R_{CELL})[(G/N)V_{ACC} - (I_{BL}R_{BL})G(G+1)/2 + g.\{V_Y - (N-1)V_{ACC}/N\}]$$

$$I_{UA} = \{(N_{BL} \times N_{WL}) - p(M+q+m) - q(G+g)\}\{(N-2)/R_{CELL}\}(V_{ACC}/N)$$

$$P_{HAR} = (p/R_{CELL})[V_{ACC}\{(M/N^2)V_{ACC} - (2/N).(I_{WL}R_{WL})M(M+1)/2\} + \{(I_{WL}R_{WL})^2 M(M+1)(2M+1)/6\} + m.(V_{ACC}/N - V_X)^2]$$

$$P_{HAR} = (q/R_{CELL})[V_{ACC}\{(G/N^2)V_{ACC} - (2/N).(I_{BL}R_{BL})G(G+1)/2\} + \{(I_{BL}R_{BL})^2 G(G+1)(2G+1)/6\} + g.(V_{ACC}/N - V_Y)^2]$$

$$P_{UA} = \{(N_{BL} \times N_{WL}) - p(M+q+m) - q(G+g)\}\{(N-2)/R_{CELL}\}(V_{ACC}/N)^2$$

Fig. 2: A detailed illustration of different variables and metrics used for modeling the leakage in a cross-point array. The governing closed-form equations of the compact model are also listed.

selectors [8]. This type of selectors exhibits abrupt switching from high resistance state (HRS) to low resistance state (LRS) beyond a critical current/voltage level. Several of such materials (*e.g.* Single Crystal (SC) VO_2, Ag-doped HfO_2, Doped Chalcogenides etc. [9]) are being considered promising for cross-point applications. Our model is general with respect to materials as long as the threshold switching behavior is involved. The basic methodology of our compact model is as follows.

A block of accessed cells in a cross-point array concurrently yields HAR, HAC and UA cells around itself (Fig. 2). Distributed interconnect resistances throughout the BLs and WLs produce gradients in supply voltage across the array and therefore each cell in the array produces different amount of leakage. Hence, for accurate estimation, traditionally the entire array is implemented and leakage through each cell is monitored. For larger size of array, this demands extensive computation. On the contrary, in our approach, we only need to simulate the accessed block, which is usually a tiny fraction of the entire array. We express the block of accessed cells as an equivalent circuit (Fig. 3) with distributed per cell interconnect resistances (R_{BL} and R_{WL}). We assume the resistances of the HAR and HAC cells to be significantly high (due to having *selectors* in OFF state) compared to R_{BL} and R_{WL}. Therefore, the effect of HAR and HAC cells are coupled to the accessed block through lumped resistances R_{HAC} and R_{HAR} (Fig. 3), whose values are functions of the location of the accessed block. We simulate this simplified equivalent circuit in SPICE (instead of implementing and simulating entire array) to obtain four parameters (I_{BL}, I_{WL}, V_X and V_Y - in Fig. 3). We use I_{BL}, I_{WL}, V_X, V_Y, R_{BL} and R_{WL} to formulate progressions of node voltages across the array and attain their mathematical equivalent to capture effect of voltage gradient. Based on these parameters along with several other array, cell and material level constants (Fig. 2), we deduce closed form expressions for the leakage current and power (P_{HAR}, P_{HAC}, P_{UA}, I_{HAR} and I_{HAC}) considering a general (V/N) biasing scheme. To avoid repetition, only the steps for deducing the expression for P_{HAR}

Table I: Sample of The Derivation Process

$P_{HAR\,(1)} = (V_{ACC}/N - I_{WL} \times R_{WL})^2 / R_{CELL}$ …… (1)	$I_{HAR\,(1)} = (V_{ACC}/N - I_{WL} \times R_{WL}) / R_{CELL}$ …… (1)
$P_{HAR\,(2)} = (V_{ACC}/N - 2 \times I_{WL} \times R_{WL})^2 / R_{CELL}$ …… (2)	$I_{HAR\,(2)} = (V_{ACC}/N - 2 \times I_{WL} \times R_{WL}) / R_{CELL}$ …… (2)
………………………………………	………………………………………
$P_{HAR\,(I)} = (V_{ACC}/N - I \times I_{WL} \times R_{WL})^2 / R_{CELL}$ …… (I)	$I_{HAR\,(i)} = (V_{ACC}/N - i \times I_{WL} \times R_{WL}) / R_{CELL}$ …… (i)
$P_{HAR\text{-}TYPE\text{-}2} = (V_{ACC}/N - V_X)^2 / R_{CELL}$	$I_{HAR\text{-}type\text{-}2} = (V_{ACC}/N - V_X) / R_{CELL}$

$$\begin{aligned} P_{HAR\,(TOTAL)} &= P \times [\{\textstyle\sum_{i=1}^{M} P_{HAR\,(I)}\} + M \times P_{HAR\text{-}TYPE\text{-}2}] \\ &= P \times [\{\textstyle\sum_{i=1}^{M} (V_{ACC}/N - I \times I_{WL} \times R_{WL})^2 / R_{CELL}\} + M \times (V_{ACC}/N - V_X)^2 / R_{CELL}] \\ &= (P/R_{CELL}) \times [\{\textstyle\sum_{i=1}^{M} (V_{ACC}^2/N^2 - 2 \times I \times I_{WL} \times R_{WL} + I^2 \times I_{WL}^2 \times R_{WL}^2)\} + M \times (V_{ACC}/N - V_X)^2] \\ &= (P/R_{CELL})[V_{ACC}\{(M/N)^2 V_{ACC} - (2/N).(I_{WL}R_{WL})M(M+1)/2\} + \{(I_{WL}R_{WL})^2 M(M+1)(2M+1)/6\} + M.(V_{ACC}/N - V_X)^2] \end{aligned}$$

$$\begin{aligned} I_{HAR\,(TOTAL)} &= P \times [\{\textstyle\sum_{i=1}^{M} I_{HAR\,(I)}\} + M \times I_{HAR\text{-}TYPE\text{-}2}] \\ &= P \times [\{\textstyle\sum_{i=1}^{M} (V_{ACC}/N - I \times I_{WL} \times R_{WL}) / R_{CELL}\} + M \times (V_{ACC}/N - V_X) / R_{CELL}] \\ &= (P/R_{CELL})[(M/N)V_{ACC} - (I_{WL}R_{WL})M(M+1)/2 + M.(V_{ACC}/N - V_X)] \end{aligned}$$

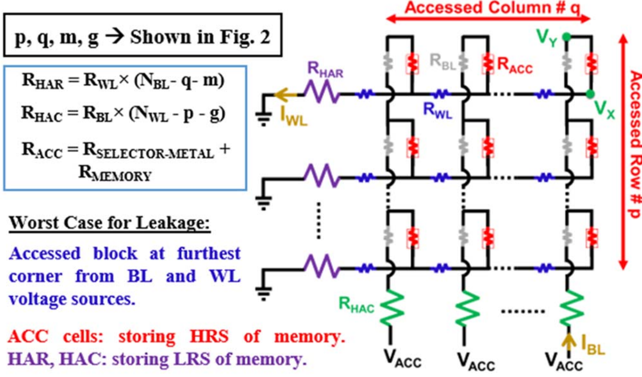

Fig. 3: Equivalent circuit for the p×q accessed block in the array (shown in Fig. 2). The resistances of the HAR and HAC cells are expressed using two equivalent resistances (R_{HAR} and R_{HAC}). We obtain I_{BL}, I_{WL}, V_X and V_Y from SPICE simulation of this circuit.

and I_{HAR} has been shown in Table I. But, all of such expressions have been illustrated in Fig. 2. This approach leads to substantial reduction in computation complexity. To justify the utility of the proposed approach, we implement a simulation framework based on both conventional and proposed technique of computation. We discuss that in next section.

III. Description of Simulation Framework

To validate the results obtained from our model, we implement full cross-point array frameworks of different sizes (16×16, 32×32, 64×64, 128×128 and 256×256) in SPICE. We choose magnetic tunnel junction (MTJ) as memory element and use a compact model from [10] to obtain its properties. In addition, we use an in-house SPICE model [9] for insulator ↔ metal transitioning threshold switch *selectors*. This model considers constant resistances of the selector in metallic and insulating state and captures the state transition as a function of electrical stimuli. The selector model coupled with MTJ model forms the model for a memory cell in the cross-point array. The parameters used for simulation and in the proposed compact model are shown in Table-II.

IV. Analysis and Verification

To keep consistency, in all of our analyses we consider a 1×8 accessed block (except in Fig. 8) at the furthest corner of the array from the voltage sources. For the analysis, we focus on *V/2* biasing (although our model is applicable for V/3 biasing scheme as well). We calculate total leakage power and current through the HA cells for different sizes of array (Fig. 4) (Note, in a V/2 scheme, leakage in UA cells is 0) The results attained from the compact model are with excellent

Table II: Default Simulation Parameters and Specifications

Memory Element	Magnetic Tunnel Junction (MTJ). T_{OX-MTJ}=1.1nm, D_{MTJ} =45nm, H_{SAT}= 80 KA/m
Selector Type	Insulator ↔ Metal Transition Threshold Switch SC VO_2 : $\rho_{MET} \approx 5\times10^{-6}$ Ω m, $\rho_{INS} \approx 0.8$ Ω m
Interconnect	$\rho_{WIRE\ (Cu)} = 1\times10^{-6}$ Ω.cm, $R_{S,WIRE}$ = 0.22 Ω/□

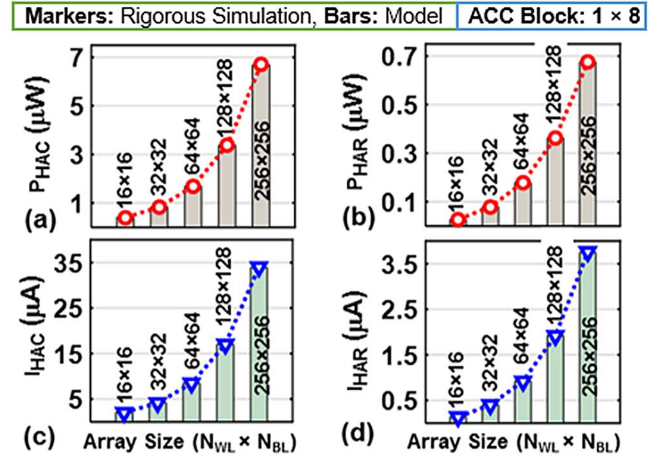

Fig. 4: The leakage power (a, b) and current (c, d) for HAR and HAC in different sizes of array. The values obtained from the compact model matches accurately with those obtained through rigorous simulation of complete array (V/2 biasing scheme).

agreement with values obtained through rigorous simulation. Next, we fix the size of the array to 256×256 and examine the effectiveness of the model in capturing impact of major design aspects.

A. Impact of OFF State Resistance of Selector

Higher OFF state resistance of the selector ($R_{SELECTOR-OFF}$) reduces leakage power and current significantly (Fig. 5). To obtain I_{HAR} < 1µA, $R_{SELECTOR-OFF}$ needs to be over 50 MΩ. The model provides accurate (~99%) estimation of leakage if $R_{SELECTOR-OFF}$ > 1 MΩ. For very low $R_{SELECTOR-OFF}$ (< 0.2 MΩ), we observe up to 10% mismatch in estimation**.** The reason for that is, lower $R_{SELECTOR-OFF}$ allows a portion of I_{WL} to flow through the HAR cells. So, the assumption of considering I_{WL} constant through the accessed WL (see Fig. 3) becomes less accurate. Similarly, the assumption of considering constant I_{BL} through the accessed BL (see Fig. 3) also becomes less appropriate. Note, a useful *selector* device is expected to have larger OFF state resistance and the model has excellent precision for practical range of values for $R_{SELECTOR-OFF}$.

B. Impact of Interconnect Resistance

Similar analysis with sheet resistance of interconnect (Fig. 6) shows that, our model can provide accurate results with up to 5 Ω/□ sheet resistance (~23X of nominal value for Cu). The interconnect resistance distorts the approximation in our model only if it becomes comparable to the metallic state

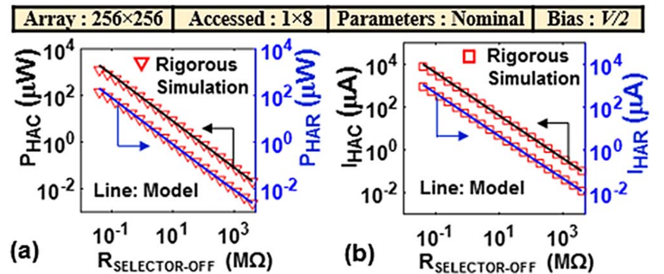

Fig. 5: The compact model precisely captures the effect of the OFF-state resistance of selector ($R_{SELECTOR-OFF}$) on (a) leakage power and (b) leakage current of half accessed (HA) cells.

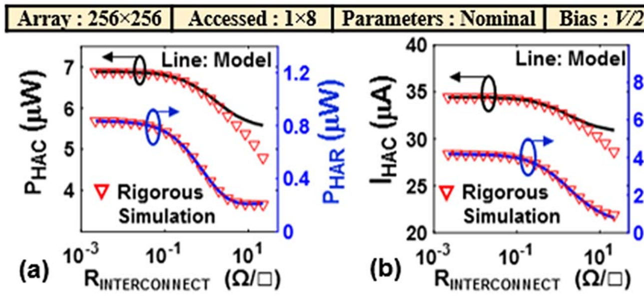

Fig. 6: The distributed interconnect resistance model considered to formulate the closed-form equations (in Fig. 2) yields accurate results up to $R_{INTERCONNECT} \approx 5\Omega / \square$.

resistance (LRS) of the *selector*. In such scenario, using lumped resistance technique to calculate R_{HAC} and R_{HAR} becomes less accurate. Note, the approximations used in the model is perfectly reasonable within practical values of interconnect resistance.

C. Impact of Access Voltage

The array leakage current and power increases with access voltage (Fig. 7). The leakage current through HAR is significantly low compared to that through HAC cells. This is due to using 1×8 accessed block which yields more HAC than HAR cells. For, access voltage of 0.4V (considered for read), leakage current through HAR cells is ~4 µA as opposed to that through HAC cells being ~40 µA. Most importantly, the compact model provides a close match to the rigorous array level simulations for different access voltages (Fig. 7).

D. Effect of Size of the Accessed Block

Finally, we examine the generality of the model by cross-checking the leakage for different sizes of accessed block. We consider 1×4, 1×8, 1×16 and 1×32 accessed blocks. As shown in Fig. 8, leakage power and current through HAC cells increases for larger accessed blocks because of the increased number of columns. Concurrently, leakage through HAR cells reduce mainly because the number of HAR cells reduces with increased size of accessed block. Moreover, the increased number of columns sink in more current from the BL and add them to yield larger current in the accessed WL. As a result a larger voltage gradient occurs throughout the WL which leads to decreased effective voltage across the HAR cells. That also contributes in reducing the leakage in HAR cells. Assuring to note, the model captures the trends well and provides accurate results for different sizes of accessed blocks.

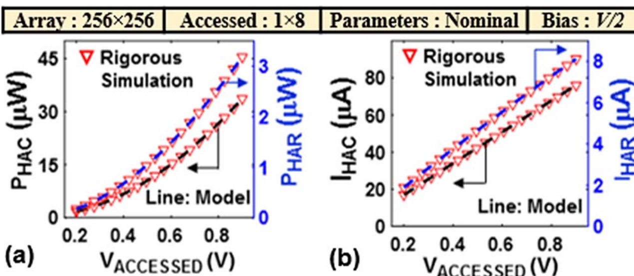

Fig. 7: Leakage (a) power and (b) current of the HA cells increases with access voltage ($V_{ACCESSED}$). For all values of $V_{ACCESSED}$, the compact model provides accurate results.

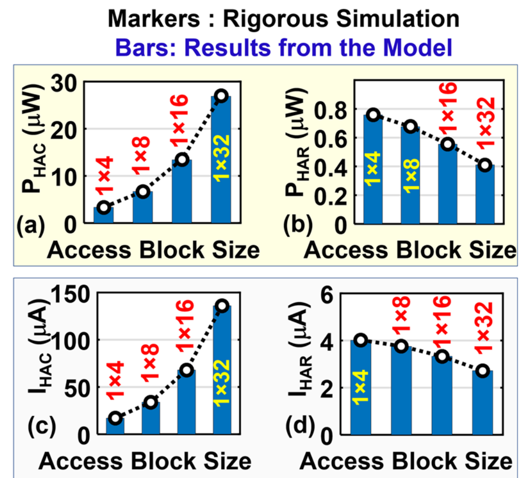

Fig. 8: Leakage (a, b) power and (c, d) current of the HA cells is a function of the size of the accessed block. If the number of row in a accessed block increases with fixed number of column, P_{HAC} and I_{HAC} increase, whereas P_{HAR} and I_{HAR} decrease.

V. Conclusion

We presented a computationally efficient approach to model the total array leakage of cross-point array averting the need for rigorous and intensive simulation of entire array. We deduced closed form expressions for leakage power and current components and coupled that to variables obtained through simplified equivalent circuit simulation of the accessed block only. The compact model is up to ~99% accurate (in comparison to results obtained through full array simulation) within ranges of practical interconnect, selector and array parameters.

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