FinFET NBTI Degradation Reduction and Recovery Enhancement through Hydrogen Incorporation and Self-Heating

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***Abstract* — Negative-Bias Temperature Instability (NBTI) degrades the drive current of p-channel FinFET because defect centers are depassivated as hydrogen diffuses away under negative bias and elevated temperature. We propose incorporating hydrogen in the gate stack to reduce hydrogen depassivation rate and, thus, NBTI degradation. This approach is also expected to enhance NBTI recovery. Besides, we also propose using punch-through stop implant in bulk FinFET as an effective mean for on-chip self-heating and self-healing to enhance NBTI recovery. TCAD simulation is used to verify the ideas.**

Keywords* — *NBTI, TCAD Simulation, Hydrogen, Stress, Recovery

I. Introduction

Negative-Bias Temperature Instability (NBTI) remains an important degradation mechanism in sub-22nm p-channel FinFETs and nano-wires [1][2][3]. NBTI means that the p-MOSFET's threshold voltage (V_{TH}) becomes more negative after ON-state operations ($V_G < 0V$), resulting in lower drain current over time. The effect is exacerbated at elevated temperature when there is self-heating in the device. At $V_G = 0V$, the devices usually experience recovery but the process is very slow. It would be very beneficial if the degradation can be reduced or the recovery can be enhanced.

To reduce NBTI degradation, various methods have been proposed in the literature, including optimization of device geometries [1][2] and gate dielectric material engineering [4]. Since NBTI is due to electrochemical reaction involving hydrogen atoms and molecules as end products (Fig. 1), in this paper, we propose hydrogen incorporation in the gate stack to reduce degradation. At the same time, it is expected that this will also enhance recovery.

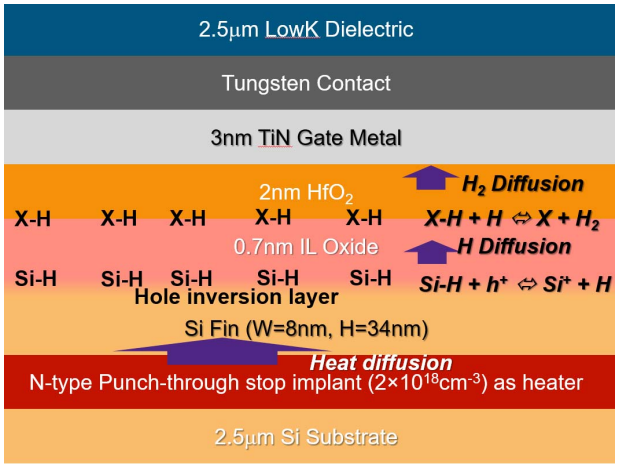

Fig.1. Schematic showing the stack layers involved in the 3D FinFET NBTI simulations. Layer thicknesses are not in scale for clarity.

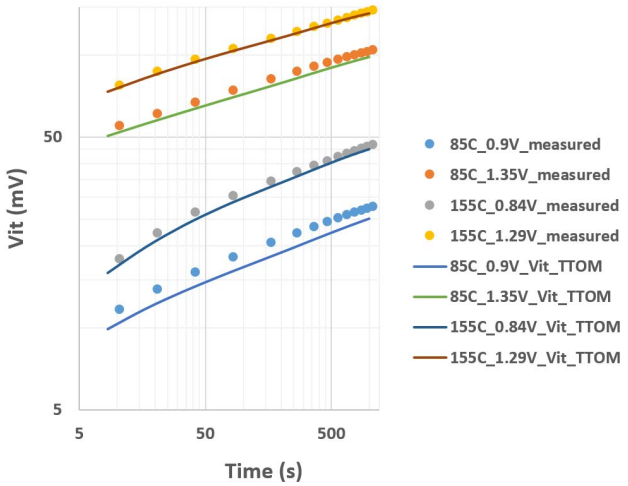

Fig. 2. Experimental and simulated bulk FinFET degradation at different temperatures and gate voltages.

To enhance recovery, besides incorporating hydrogen atoms in the gate stack, it can be achieved by using elevated temperature because the electrochemical reaction obeys Arrhenius Law and this has been confirmed in various experiments [3][5]. In this paper, we propose using punch-through stop implant in bulk FinFET as an effective mean for on-chip self-heating and self-healing.

TCAD simulations with calibrated parameters are used to verify the proposed concepts [8].

II. Simulation Framework and Setups

In the TCAD simulations, 7 equations, namely Poisson equation, electron continuity equation, hole continuity equation, heat transport equation, hydrogen atom and molecule diffusion equations and hole density gradient (for quantum correction) equation are solved self-consistently with Multi-State-Configuration (MSC) modeling reaction equations (Fig. 1). The parameters used have been calibrated to experiment at various temperatures up to 428K [1][2]. A calibrated example is shown in Fig. 2. Bulk hole traps have been isolated from the experimental data. Therefore, Fig. 2 represents the threshold voltage (V_{TH}) due to interface depassivated defect centers. Trap occupation is taken into account through Transient Trap Occupation Model (TTOM) [1][2].

III. Hydrogen Incorporation

Fig. 3 shows the NBTI degradation of FinFET stressed for 1000s at V_G = -1.2V at 358K followed by

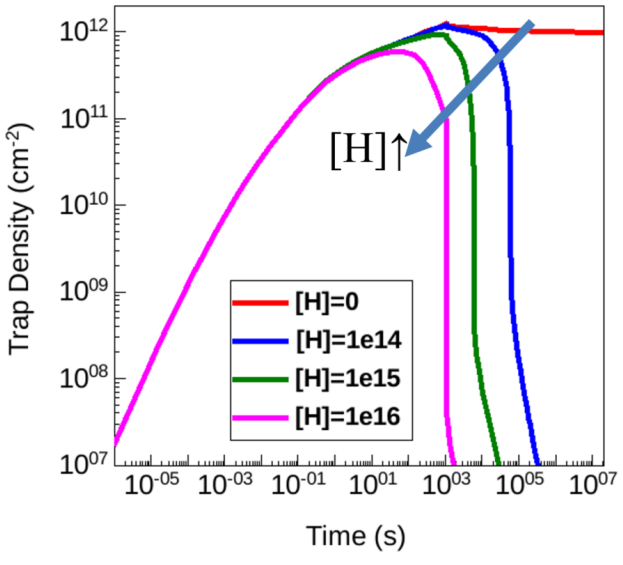

Fig. 3: Trap density evolution as a function of initial TiN/Tungsten H concentration (cm^{-3}). Before 1000s is stress, V_G = -1.2V at 358K. After 1000s is recovery, V_G = 0V at 300K.

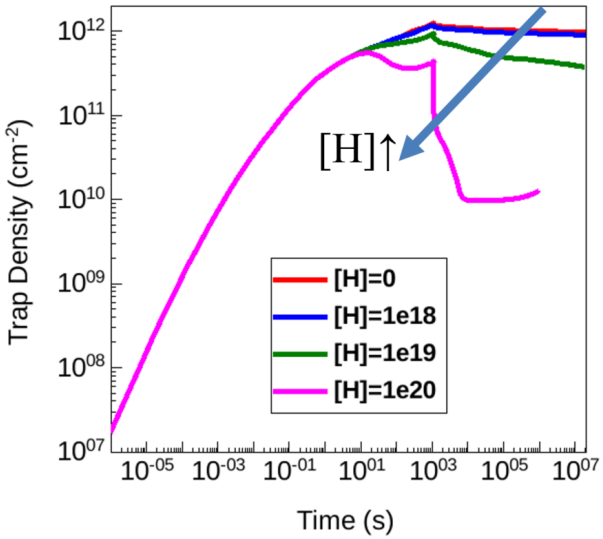

Fig. 4: Trap density evolution as a function of initial H concentration (cm^{-3}) in TiN gate. Before 1000s is stress, VG=-1.2V at 358K. After 1000s is recovery, VG=0V at 300K.

recovery. If the fabrication process can be modified such that there are initially $10^{16}cm^{-3}$ H atoms in the gate TiN and Tungsten, degradation can be substantially reduced and recovery (V_G = 0V at 300K) can also be enhanced (almost fully recovered within 1000s). This is because NBTI degradation involves the reaction of Si-H with hole to form Si+ and H atom (Fig. 1). By incorporating hydrogen atoms in the gate stack, the reaction is shifted to the left and thus retards the forward reaction (i.e. degradation).

In the literature, there have been efforts to incorporate H in gate TiN for workfunction modifications. In this case, minor modification to the fabrication process is needed. We investigated by incorporating H in the 3nm TiN only (instead of both TiN and Tungsten plug), it will then require $>10^{19}cm^{-3}$ H atoms to reduce degradation and enhance recovery (Fig. 4). The required H concentration is higher because of the smaller volume of TiN.

IV. On Chip Self-heating and Self-annealing

On chip annealing using built-in heaters have been proposed and demonstrated in the literature. The advantage of built-in heater is that it will heat up the gate dielectric locally to very high temperature (>1000°C) in short time (ns) without damaging, for example, metal contacts. Demonstrations were mostly done by using poly-Si gate as heater [6][7][8]. And it has been used to cure hot carrier injection damage [6][7] and radiation damage [8]. Such idea might be applicable to NBTI.

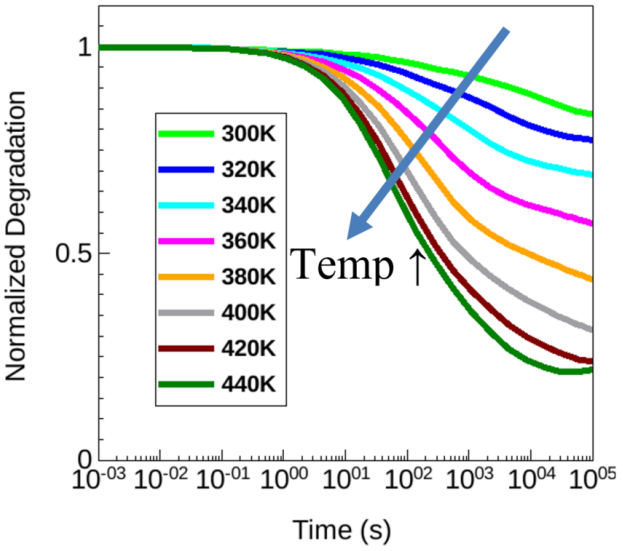

Fig. 5. Recovery as a function of ambient temperature at V_G = 0V. The structure was stressed at 358K at -1.2V for 1000s.

We first simulate the effect of temperature on the recovery in NBTI after a structure was stressed at 358K at -1.2V for 1000s. Recovery at different ambient temperatures (from 300K to 440K) after stress were simulated (Fig. 5). Since the parameters were only calibrated to 428K as mentioned earlier, the simulation is limited to 440K. With higher temperature, recovery becomes faster (e.g. at 440K, it can reach 40% healing within 100s compared to 4% at 300K). The trend is consistent with the experimental result in [3].

To incorporate the "heater", one may use dummy poly in the standard cell layout. For simplicity, we assume alternating dummy poly and gate metal (Fig. 6). Doping of the dummy poly is $10^{20}cm^{-3}$. A voltage that will result

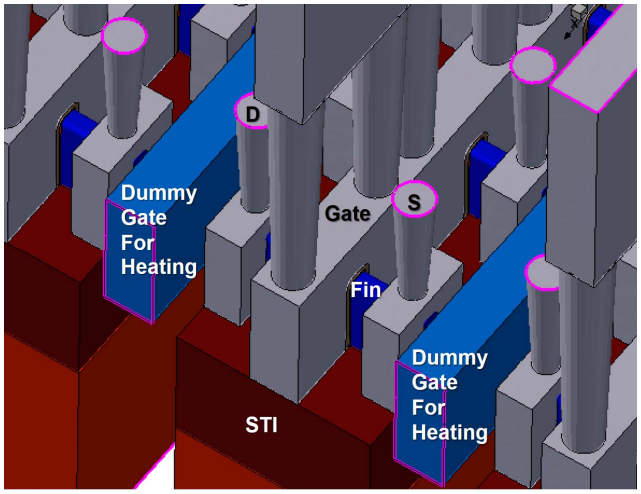

Fig. 6. Structure used in the self-heating simulation with dummy gate heater. Due to symmetry, only a portion is used with reflective boundary conditions.

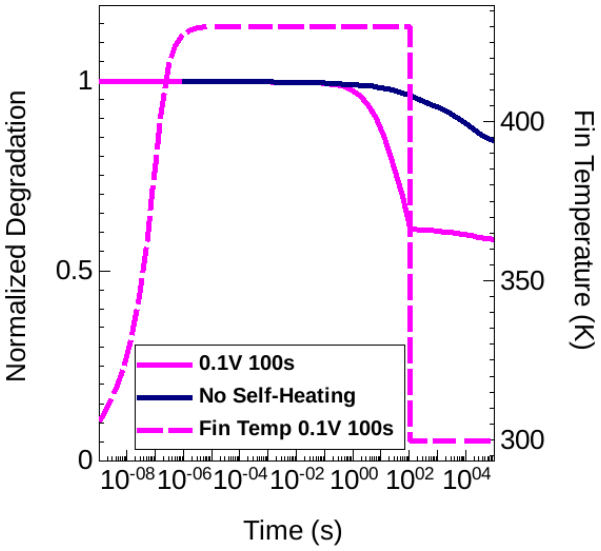

Fig. 7. Recovery as a function of time without and with self-heating (using dummy gate heater). The heat pulse is turned on at 1ns and last for 100s.

in E-field of 0.1V/35nm is turned on for 100s after stress (Fig. 7). It can be seen that the fin temperature reaches 430K in less than 1µs and 40% of the degradation recovered in 100s (compared to 4% without heating), which is orders of magnitude faster than room temperature recovery.

However, dummy poly consumes too much layout space and may result in non-uniform heating in different standard cell design. We propose a more effective way by utilizing the punch-through stop implant as the heater (Fig. 8). The punch-through stop implant is a heavily doped region (e.g. $5\times10^{18}cm^{-3}$ n+) under the Fin (e.g. p-type FinFET) as showed in Fig. 8. If one can apply voltage to both ends of the punch-through stop implant, the current will be confined to the implant which acts as a

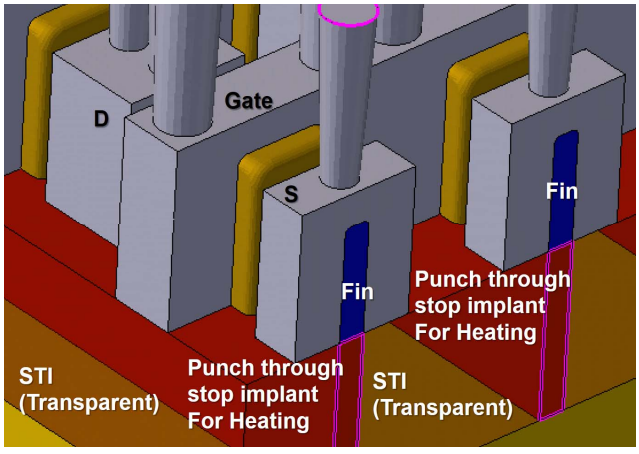

Fig. 8. Structure used in the self-heating simulation with punch-through-stop-implant heater. Due to symmetry, only a portion is used with reflective boundary conditions.

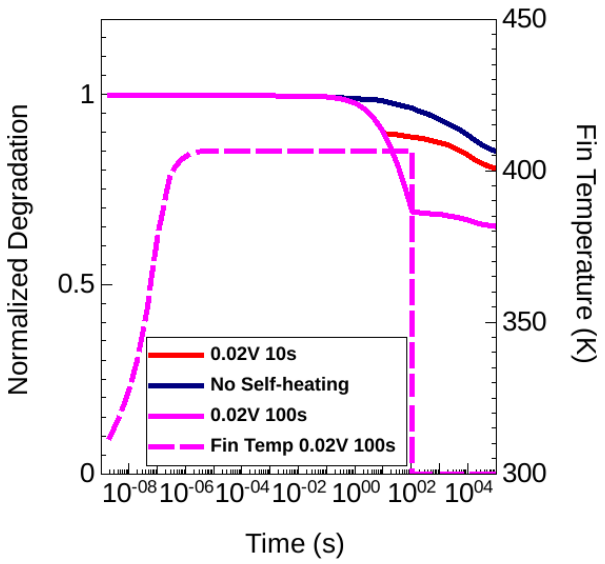

Fig. 9. Recovery as a function of time without and with self-heating (using punch-through-stop-implant heater). The heat pulse is turned on at 1ns.

heater. It has three advantages. Firstly, every FinFET has punch-through stop implant beneath it and they are in closed proximity. Therefore, all FinFET can be heat up more uniformly. Secondly, since it is sandwiched between STI oxide, less power consumption is needed to reach the desired temperature (e.g. E field ~ 0.02V/45nm is needed to reach 410K in the Fin) (Fig. 9). Finally, it saves area and has less impact on standard cell design.

In terms of power consumption, the FinFET used in this example has ON-state power consumption ~ 10^{-5}W while the heater power consumption is about 10^{-8}W. In the simulation of Fig. 9, since the stress time is 1000s while it takes only 100s to have substantial recovery, it represents <0.01% of the active power consumption of the FinFET for this particular DC stress/recovery scenario.

V. Conclusion

Using TCAD simulations with parameters calibrated to experiments at different temperatures (300K ~ 428K), we verified the possibility of using H incorporation in gate stack to reduce NBTI degradation in FinFET and using on-chip heater to enhance recovery through self-annealing.

If the fabrication process can be modified such that there are 10^{16}cm^{-3} H in the TiN/Tungsten gate stack or 10^{19}cm^{-3} H in the TiN alone, NBTI degradation can be substantially suppressed and recovery is greatly enhanced.

With on-chip self-heating using poly heater or punchthrough stop implant heater, NBTI recovery can be enhanced. However, using punchthrough stop implant heater is the most effective and efficient approaches. With small power consumption (~0.01% of total active power), 40% of degradation can be recovered (compared to 4% in non-self-heating case) in 100s in a DC stress/recovery scenario.

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