Circuit-Aging Modeling Based on Dynamic MOSFET Degradation and Its Verification

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***Abstract*—The reported investigation aims at developing a compact model for circuit-aging simulation. The model considers dynamic trap-density increase during circuit operation in a consistent way. The model has been applied to an SRAM cell, where it is believed that the NBTI effect dominates. Our simulation verifies that the hot-carrier effect has a compensating influence on the NBTI aging of SRAM cells.**

Keywords— Aging; Circuit Simulation; Compact Model; Hot Carrier; NBTI; SRAM

I. Introduction

Device degradation, origin of the circuit degradation, has become a serious problem due to advanced technologies utilizing scaled device dimensions and critical operation conditions, both of which complicate the assurance of sufficient safe-operating area [1]. *Bias Temperature Instability* (BTI) and *Hot Carrier* (HC) are the most dominant aging effects in the nano-scale CMOS technology era [2, 3]. Thus, for robust circuit design, accurate prediction of circuit aging based on their origins is one of the high priority prerequisites. Circuit-aging prediction requires a compact model, which considers the carrier-trapping events during dynamic stress/relax repetitions, which are the origin for both effects.

In this work a compact circuit aging model is presented, which enables to simulate dynamic MOSFET degradation. To evaluate the proposed aging model, aging of a 6T-SRAM cell is investigated, in which the reliability issue is becoming a serious problem due to aggressive transistor downscaling. It is known that NBTI is mostly responsible for aging of the SRAM-based memory structures due to long-term fixed-bias stress that transistors experience during SRAM operation [4]. The results show, that the different influences of NBTI and HC effects on device aging lead to SRAM-cell-reliability dependence on circuit-operation conditions, which may result in dominance of one of the two effects. It is demonstrated here that the HC effect can even compensate the degradation caused by the NBTI effect.

II. Origin of Transistor Aging

Fig. 1 shows two different stress conditions which occur during circuit operation. Fig. 1a is the case when the drain voltage V_d is relatively large. Hot carriers are induced, when carriers gather high kinetic energy from the high electric field during moving from source to drain along the channel and become hot. If the hot carrier strikes a *Si* atom in the crystal, it can generate extra electrons and holes due to the *Impact Ionization* effect. Some of these carriers can be trapped at the interface between the substrate and the gate insulator. This leads to an increase of the carrier trap density [5]. The drain side of the interface is mostly affected by hot carriers, because these carriers get the largest kinetic energy due to the highest electric field at the drain.

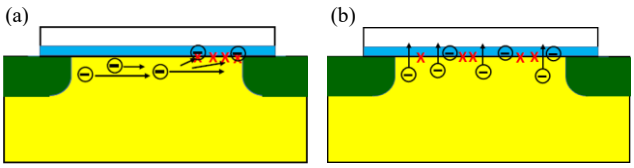

Fig. 1. (a) HC effect: Interface Traps are generated at the drain side, due to high-energy charge carriers which are accelerated due to electrical field between the source and the drain. (b) BTI effect: Interface Traps are generated due to high electric field between the transistor's gate and the substrate.

Fig. 1b refers to the case when not V_d but the gate voltage V_g is relatively large. Under this bias condition, carriers are trapped at the whole gate-oxide interface due to the high electric field within the gate oxide. The effect is frequently observed for pMOSFETs and is called NBTI, whereas it is called PBTI for nMOSFETs. A characteristic feature of the BTI effect is that most of the MOSFET degradation due to the stress is recovered after removing the stress. Therefore, the BTI aging rate is dependent on the signal waveform applied on the gate insulator during circuit operation. The specific NBTI feature has been explained by hydrogen atoms which form covalent bonds with *Si* at the interface [6]. Carriers reaching the interface break the bonds and are trapped. When the high electric field is removed from the gate, the trapped carriers are detrapped which leads to a partial recovery from BTI. The remaining trapped carriers are trapped at deep energy states localized deep in the gate oxide, which cannot be detrapped under normal operating conditions.

For the robust circuit design, both HC and BTI effects must accurately be predicted, so that unnecessary large guard-banding can be avoided. For achieving this aim, an accurate compact aging model is required.

III. Circuit-Aging Modeling

In the present investigation, the aging effect is modeled based on the trap-density increase in two aspects. One is induced

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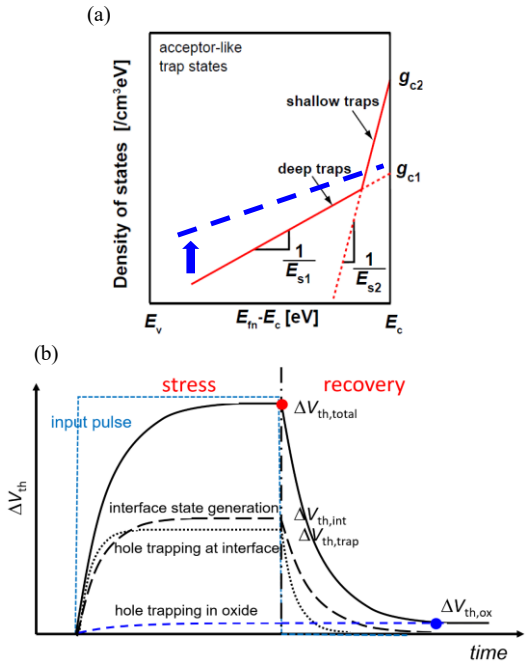

Fig. 2. (a) Trap state-density distribution as a function of energy. Aging is modeled by hot-carrier-induced trap-density increase of the deep states. (b) Aging due to applied E_{ox} is modeled by three different mechanisms, where the $\Delta V_{th,ox}$ is responsible for long-term aging.

by hot carriers (the HC effect), and the other is by the high electric field in the oxide (the N(P)BTI effect).

Modeling of the HC effect is done by considering the trap density increase explicitly. Two independent trap-density distributions (shallow and deep) are considered as shown in Fig. 2a, where the deep-trap level is responsible for the long-term device aging [5]. The tarp density increase is dependent on the stress condition, namely the bias condition and the stress duration. Evaluation of the stress is done by the substrate current (I_{sub}) induced during circuit operation, which is a function of dynamically varying V_g and V_d applied to the MOSFET. Integrated I_{sub} during circuit operation is used for modeling the aging degradation.

The N(P)BTI is usually observed as a threshold voltage shift (ΔV_{th}), which can be described by a homogeneous trap-state distribution within the bandgap. The carrier trap/detrap event (see Fig. 2b) during the stress/recovery process is modeled by the time constants τ_s and τ_r for trapping and detrapping, respectively [7, 8]. This enables an accurate description of the bias-waveform dependency of ΔV_{th}. Modeling of ΔV_{th} is done on the basis of the oxide-electric field change due to the trapped charge.

The dynamically changing trap density N_{trap} is included in the Poisson equation to self-consistently capture its overall effect

$$\nabla^2\phi = -\frac{q}{\varepsilon_s}(p - n + N_D - N_A + N_{trapD} - N_{trap\_A}) \qquad (1)$$

Here N_{trap_D} and N_{trap_A} are the donor-like and the acceptor-like trap densities, respectively. The Gauss law describes the

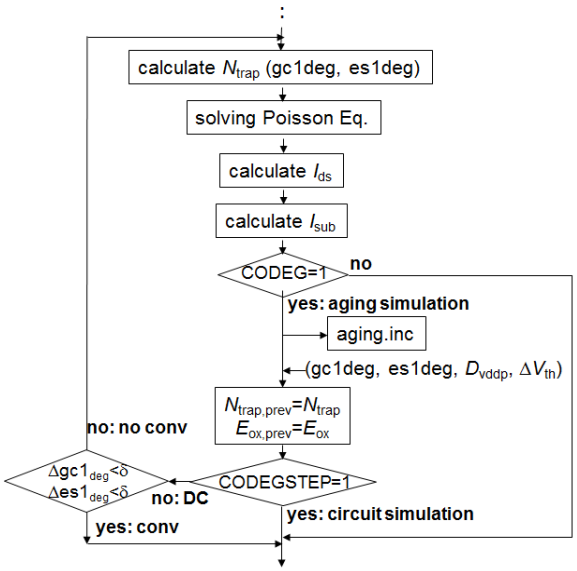

Fig. 3. Flowchart of circuit-aging simulation.

condition to be preserved, where the dynamically changing E_{ox} appears

$$E_s\nabla\phi_s = E_{ox}\nabla\phi_{ox} = E_{ox}\frac{V_{gs} - V_{fb} - \phi_s - \Delta V_{th}}{T_{ox}} \qquad (2)$$

The threshold voltage shift (ΔV_{th}) is modeled again as a function of E_{ox}, so that Eq. 2 must be solved iteratively.

Since the carrier densities p and n as well as N_{trap} and E_{ox} are functions of the electrostatic potential ϕ_s at the channel surface, accurate calculation of ϕ_s is a prerequisite. Thus the Poisson equation is solved iteratively without simulation time penalty together with the Gauss law in the same way as done for the HiSIM compact model [9]. Since the trap density changes the electrostatic potential distribution, all device characteristics such as carrier density and mobility are automatically influenced by this change.

The long-term aging is modeled by integrating physical quantities such as the substrate current I_{sub} for HC and the oxide-field change ΔE_{ox} for N(P)BTI during the circuit operation. Since the physical quantities are dynamically changed, an iterative solution is necessary to achieve a self-consistent solution. The implementation of the aging model in HiSIM is explained in Fig. 3. Circuit-aging simulation is performed conventionally with two steps: At first, stress conditions are characterized for individual devices within the circuit, and then real aging simulation with the aged model-parameter values is performed. As can be seen in Fig. 3, the developed approach requires only one simulation run. The convergence characteristics to a consistent solution during circuit simulation is shown for nMOSFETs in Fig. 4a and for pMOSFETs in Fig. 4b.

IV. 6T-SRAM Aging Evaluation

Fig. 5 shows comparisons of model calculation results and measurements of I_d-V_g characteristics for different DC stress

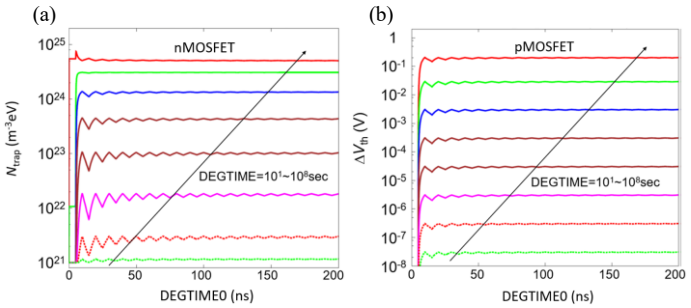

Fig. 4. Convergence characteristic to a self-consistent solution of (a) N_{trap} of nMOSFET and (b) V_{th} shift of pMOSFET as a function of the circuit-simulation length DEGTIME0.

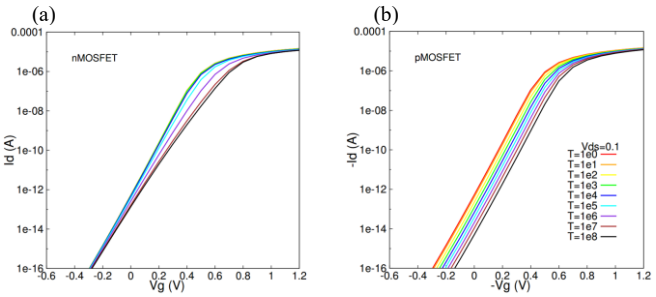

Fig. 5. Effects of (a) HC and (b) NBTI on I_d-V_g characteristic curves of nMOSFETs and pMOSFETs, respectively.

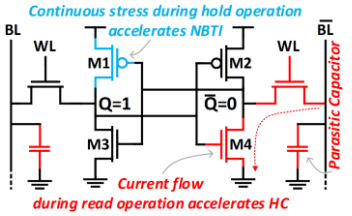

Fig. 6. Structure of the 6-transistor SRAM-cell.

durations. From the measurement features, only the HC effect is considered for nMOSFETs in our present study. On the contrary, the NBTI effect is additionally considered for pMOSFETs. The typical features of the HC effect observed in nMOSFETs are well reproduced as demonstrated in Fig. 5a. The simulation results, show the slope change of the I_d-V_g characteristics curve changes due to the trap density distribution as depicted in Fig. 2a. This concludes that the nMOSFET aging due to the HC effect cannot be modeled simply on the basis of ΔV_{th}, different from the aging modeling of the pMOSFET.

In the pMOSFET case, measured I_d-V_g characteristics are just shifted in parallel with increased stress duration. This can be modeled simply by the ΔV_{th} caused by the E_{ox} reduction due to the trapped carriers. It is seen that the measurements are well reproduced by the developed aging model.

With use of the MOSFET-aging characteristics, a 6T-SRAM cell is studied. The schematic of the 6T-SRAM cell, the most-widely-used SRAM cell, is depicted in Fig.6. The stored value is latched in a positive feedback between two NOT gates. The high utilization of SRAM memories and their vulnerability against aging make simulation techniques, which aim to assess aging effects on the SRAM-cell functionality, highly desirable.

Two circuit conditions that accelerate aging of digital circuits are high drain current due to fast switching with high frequency, and long-term ON-state stress of some MOSFETs. The former condition accelerates the HC effect and the later condition accelerates NBTI [10]. Both of these conditions can be observed for the SRAM cells. The cross coupled structure of the SRAM memory leads to continuous stress condition on two of the six transistors regardless of holding '0' or '1' (See Fig. 6). This is while, when the SRAM cell is accessed during the read operation, nMOSFETs of the SRAM cell experience a high HC aging effect. When a read operation is performed, one of the precharged bit-lines is discharged through one of the access transistors and one of the nMOSFETs of the SRAM cell. Because the bit-lines have high parasitic capacitance, a high current flows through these nMOSFETs and leads to the acceleration of HC aging.

The effect of aging on SRAM cells can be verified as *Static Noise Margin* (SNM) degradation. SNM is the smallest required noise voltage to flip the stored value in a SRAM cell. This noise can be generated by energetic-particle strikes, operating-voltage fluctuations, or electromagnetic interferences.

SNM is usually determined by the edge size of the largest square inside the *Voltage Transfer Characteristic* (VTC) curve. The VTC curve plots the voltage of the two internal SRAM-cell nodes of Q and $\bar{Q}$ (see Fig. 6) versus each other, during '0'→'1' and '1'→'0' switching [10].

The VTC curve of the studied SRAM cell is plotted in Fig. 7 at fresh time and after 10^8 seconds for two different duty cycles of 50% and 90%, utilizing the developed compact aging model. As Fig. 7 demonstrates, the effects of NBTI and HC shift the VTC curve in opposite directions.

For a duty cycle of 50%, shift magnitudes of both NBTI and HC are close to each other. This means the SRAM cell transistors are aged with the same pace. The VTC curve shifts upward due to the HC effect, which causes nMOSFET aging. On the other hand the VTC curve shifts downward due to the NBTI effect for the pMOSFET. Due to the HC aging effect, the pull-down transistor of the SRAM cell is weakened, therefore, higher voltage on the internal nodes is required for bit-flip to be performed. This is while due to the NBTI effect, the pull-up transistor of SRAM cell becomes weak, so that lower internal node voltage (higher gate to source voltage on pMOSFETs) is required for the transition.

The NBTI shift increases drastically, when the duty cycle of SRAM-cell operation is increased to 90% or higher, which can be observed for many SRAM cells of the chip. Under this condition, the NBTI effect becomes dominant and this is the main reason for SNM degradation of the cell. By increase of the number of read and write operations to the SRAM cell, the effect of HC on the SRAM cell lifetime increases.

The reason for lower HC effect in comparison with NBTI is shown in Fig. 8, which demonstrates the drain currents of the

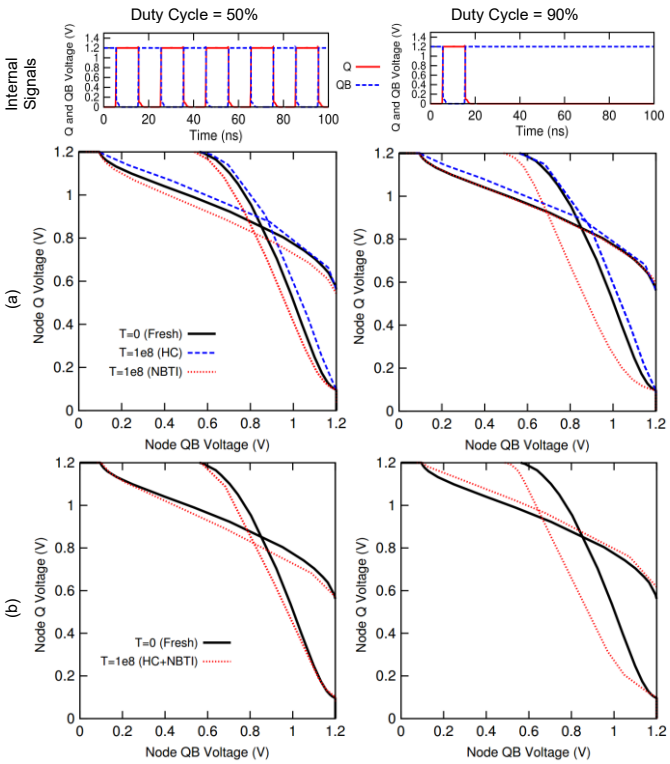

Fig. 7. Effects of NBTI and HC on the VTC curve of the studied 6T-SRAM cell (see Fig. 6) under duty cycles of 50% and 90%, after 10^8 seconds usage. (a) NBTI and HC effects are shown separately, (b) total effect is compared with fresh SRAM cell.

SRAM's transistors. The current flows only during the switching time, which decreases for higher or lower duty cycles.

The results reveal that considering the total effect of NBTI and HC leads to about 15% more SNM degradation for a duty cycle of 90% in comparison to only considering NBTI.

This is while the SNM shift for a duty cycle of 50%, by only considering NBTI, is close to the situation where both NBTI and HC are considered. Thus, the accuracy of SNM assessment is related to the duty cycle of SRAM cells. For higher duty cycles, considering both of NBTI and HC is mandatory, while for duty cycles close to 50%, considering only NBTI delivers remarkable accuracy.

By increasing the read-access rate to the SRAM cell, the HC effect becomes dominant for SNM degradation. Fig. 9a shows the SNM degradation of a 6T-SRAM cell as a function of read access frequency after 10^8 seconds. The read access frequency to most SRAM cells in real applications, like cache memories, is far less than 1GHz. Therefore, the HC effect is not the major aging process in SRAM cells of a normal processor.

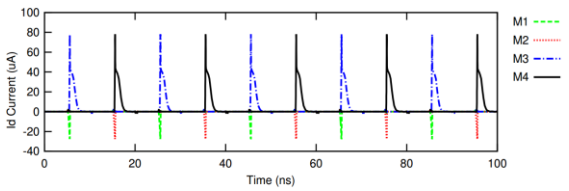

Fig. 8. Transient drain currents of four transistors M1 to M4 (see Fig. 6) of the studied SRAM cell. Drain currents flow only during the switching time.

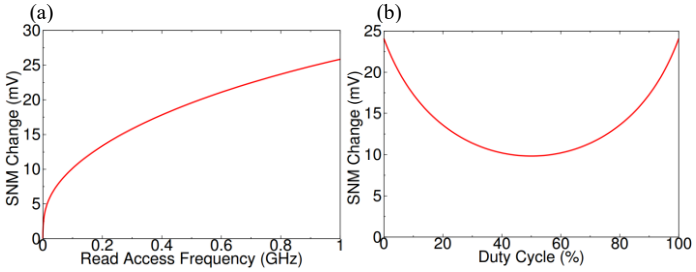

Fig. 9. (a) Effect of read access frequency and (b) different duty cycles on the SNM change of the 6T-SRAM cell after 10^8 seconds of operation.

Fig. 9b shows the duty-cycle effect (the chance of storing '1') on SNM degradation of the 6T-SRAM cell. By increase or decrease of the duty cycle from 50% to 100% or 0%, respectively, the SNM degradation rate increases by up to 131%. Therefore, SRAM cells that should store a constant value for a long time period and are only read frequently, experience the highest aging rate due to HC and NBTI effects.

V. Conclusion

Evaluating aging effects on the reliability of SRAM circuits by using simulation techniques is highly required for reliable VLSI design. In this work the effect of the most important aging effects of NBTI and HC are investigated using a developed model which considers the trap density increase. The results show that the SNM of SRAM cells can be considerably affected due to duty cycle changes. This is while HC is not considerably affected by the duty cycle variations.

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