A Unified Aging Model with Recovery Effect and Its Impact on Circuit Design

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***Abstract*—In this paper we not only discuss how to implement the recovery effect with TMI but also give various examples to show that without considering the recovery effect, the design margin of a system can be either under- or over-estimated. To validate our modeling methodology, the simulation results are benchmarked with measurement data.**

Keywords—TMI, Aging Model, Recovery Effect

I. INTRODUCTION

To ensure a circuit that can function properly over the planned lifetime, aging analysis with different effects has to be included in the design flow. For advanced technologies, aging simulation, particularly estimating performance drift due to HCI and BTI, has become even more indispensable due to the diminishing design margins. Aging models in commercial simulators are proprietary and incompatible to each other. Worst of all, the aging simulation results from different simulators are often different causing confusion. In the past, we have developed HCI and BTI models through TSMC Model Interface (TMI) [1-2]. TMI is an industry standard model interface [3] and has been supported by most commercial circuit simulators. However, existing aging model in TMI doesn't include BTI recovery effect. The simulated device degradation can be too pessimistic. To further tighten the design margin, BTI recovery effect must be considered. Furthermore, device self-heating (SHE) can affect BTI lifetime significantly. SHE and BTI should be linked in the simulation as well. In the paper, we present a unified aging model with BTI recovery effect using TMI. Since we also implemented SHE in TMI, BTI and SHE are naturally linked in our model. This unified aging model can be applied to any simulator supporting TMI without the need for extra licenses as required in some commercial aging simulators. Measurements are also provided to validate this model.

II. MODEL VALIDATION WITH MEASUREMENT DATA

A high-level description of the interaction between TMI and simulators is depicted in Fig.1. Because TMI shared library can get simulation information (such as time, voltages and currents, etc.) from simulators and is able to update model parameters during simulations [2], it allows us to adjust device characteristics shift due to HCI and BTI [2-3]. This paper describes how the BTI recovery is implemented in TMI.

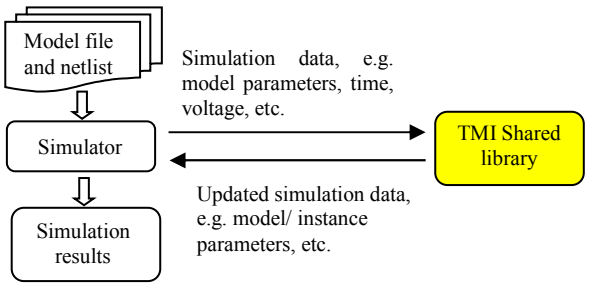


Fig.1 A high-level description of TMI simulation flow

In BTI, degradation and recovery mechanisms co-exist and will cancel out each other. It is found that degradation (recovery) rate is a function of degradation as well as biases. For a given bias, there exists a net degradation (D_r, usually Idsat), where $dD_r/dt = 0$ (i.e. degradation and recovery rates are the same). We call this the balanced point D_b, which can be extracted from measurement. For example, considering a stress waveform either (i) from high to low or (ii) from low to high is applied to a MOS device as shown in Fig.2. After a long stress time, the degradation will reach a steady state when the degradation and recover rates are the same and this measured steady-state D_r is D_b. By adjusting the stress voltages, D_b versus voltage relationship can be obtained.

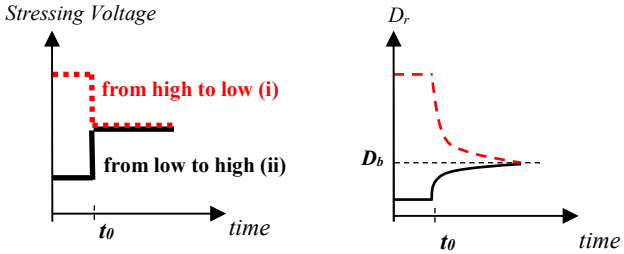


Fig.2 An illustration of extracting D_b under a given condition

Furthermore, as described in [1], there is a one-to-one correspondence between D_r and dD_r/dt for a given bias. This relationship can be readily characterized from the standard stress experiment, i.e. D_r versus time. For example, if a stress waveform as shown in Fig.3a is applied to a device and we know the corresponding dD_r/dt versus D_r curve for each stress voltage level as shown in Fig.3b, we will be able to calculate the net degradation change versus time due to both the degradation and recovery mechanisms.

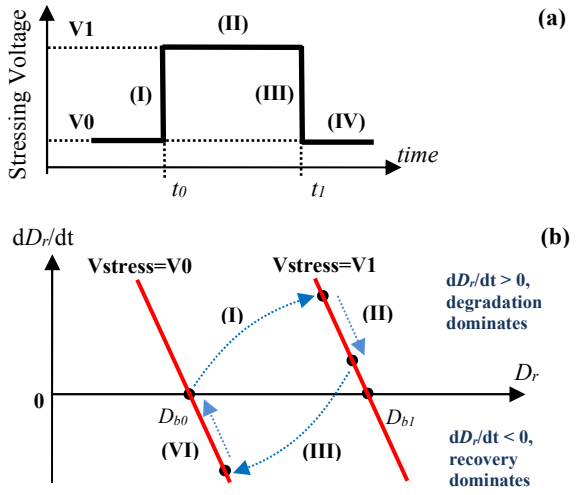


Fig.3a The applied stress voltage waveform. Fig.3b The trajectory of dD_r/dt vs D_r under the stress waveform. The red lines describe the relationship between dD_r/dt vs D_r at V0 and V1, respectively; D_{b0} and D_{b1} are the balanced points at the two voltages.

Under a given bias, if $D_r < D_b$, dD_r/dt is positive. This means the degradation mechanism is stronger than the recovery mechanism, thus D_r will increase with time until it reaches D_b and vice versa. Note that the degradation (recovery) rate also gradually reduces as it reaches the steady state. This is the basic BTI recovery concept we adopt. The unified BTI recovery model adds this bias-dependent D_b and recovery calculation methodology on top of our existing aging model. To validate our model, we stressed a device with a waveform shown in Fig. 4a. To observe the recovery effect more clearly, we used very low cycle pulses. The time between two stress pulses decreases successively, but the pulse widths are the same. The measurement data and simulation results are shown in Fig. 4b.

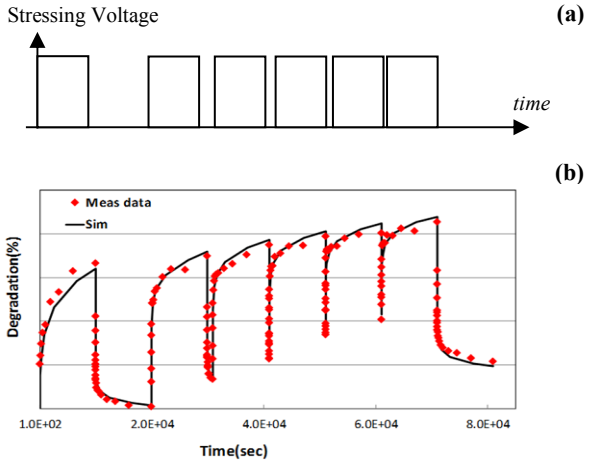


Fig.4a A chain of stress pulses with low cycles. The pulse width is fixed at 10^4 sec. The separation between two pulses varies from 10^4 sec, 10^3sec, 10^2sec, 10sec, to 1 second. Fig.4b The measurement data and simulation results with recovery effect included.

The net degradation D_r continues to increase during the on-state of each pulse because D_r is smaller than D_{bON} of the stressed voltage. However, the degradation rate becomes smaller as D_r reaches D_{bON}. During the off-state, D_r is larger than D_{bOFF}, thus recovery rate dominates and D_r decreases [4]. The simulation tracks the measurement data very well demonstrated our recovery modeling methodology. To further verify our model, we simulated the degradation using periodic pulse chains with different duty cycles at two frequencies. The results are shown in Fig.5.

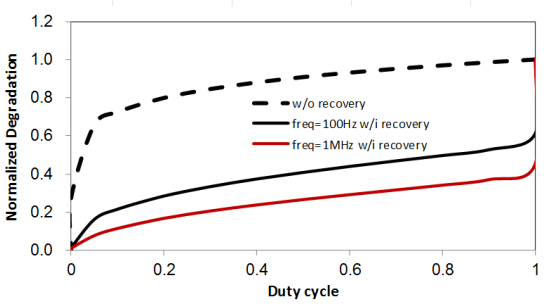


Fig.5 Simulated degradation vs duty cycle.

As expected, D_r increases with duty cycle as the amount of time for recovery decreases. Without the recovery effect, the simulation results for both frequencies are the same because the total amounts of tress time are the same. However, when the recovery effect is included, D_r decreases with the operation frequency because there are more cycles for D_r to recover (note that the recovery rate is the highest when the voltage starts to drop).

The inset of Fig.6 shows the DC and AC stress conditions. The total amounts of stress time in both cases are the same. Due to recovery effect, it is known that the degradation for AC stress will be smaller than that of the DC case. Thus people often use a fixed AC/DC degradation ratio to estimate the AC degradation. Although simple, this approach failed to take into account of the frequency dependence of the recovery effect unless the AC/DC ratio has been calibrated for a particular waveform.

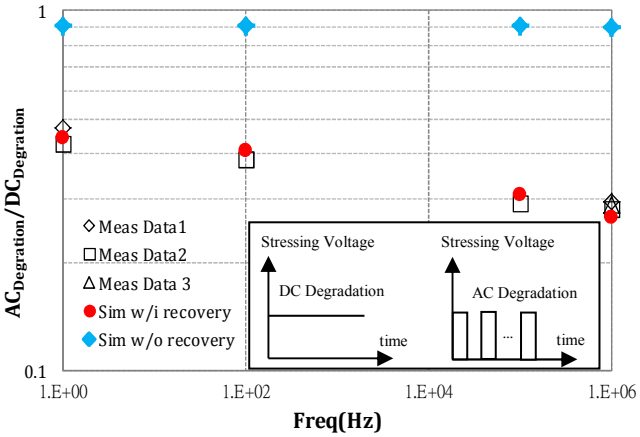


Fig.6. The inset shows the setup of DC degradation and AC degradation with duty cycle equals to 0.5. The total stressing time is 1.0e4 sec for both cases. Assuming AC degradation / DC degradation as a constant to estimate the AC degradation will fail to take the frequency dependence in the AC degradation into account.

In real circuits, the voltage waveforms applied to devices are more complicated. The only way to accurately simulate BTI recovery effect for arbitrary waveforms is to include the recovery effect in the aging simulation. Fig. 7 shows the measured and simulated degradation of an arbitrary stressing voltage. The good agreement again demonstrated that our BTI recovery model and methodology are also valid to any waveforms.

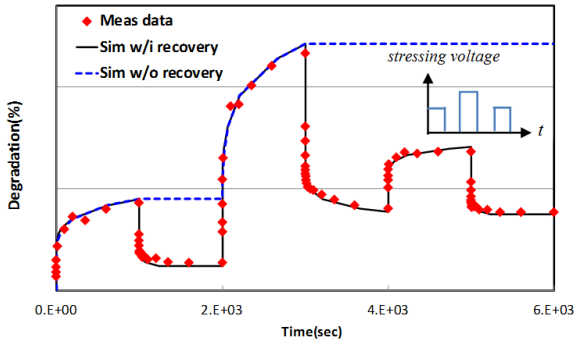


Fig.7 Measured and simulated degradations under an arbitrary pulse train stress.

III. Aging Circuit Simulations with BTI Recovery Effect

There is no difference in the simulation flow compared to the existing aging simulation [3]. All the work is done in the TMI library (Fig.8), which is transparent to users. No extra effort is needed from users except for setting some flags unless users would like to turn on/off recovery and/or SHE effects to study the importance of each effect.

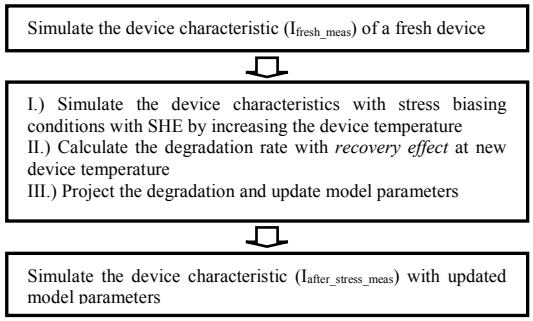


Fig.8 The TMI aging simulation flow with BTI recovery effect and SHE included. The evaluation of degradation rate and degradation projection in (II) and (III) are done in the TMI library automatically.

A simple differential amplifier is used to demonstrate the impact with and without recovery effect included. The circuit, stress waveform, and simulation results are shown in Fig.9. For differential amplifies, the mismatch between the two input transistors is a critical parameter as it affects the output offset voltage. Without the recovery effect, the two transistors will degrade identically as long as they are stressed by the same amount of time. However, due to the recovery effect, even under similar periodic waveforms, the degradation between the two transistors can be different. Without considering the recovery effect, the simulation won't be able to take the degradation induced mismatch into account and won't be able to simulate the output voltage offset drift as the circuit ages.

Furthermore, in digital circuit designs, recovery effect plays an important role in analyzing the time delay in both cell and path levels. In the following studies, we only considered PMOS BTI recovery effect in the simulation as our NMOS devices do not exhibit significant BTI effect.

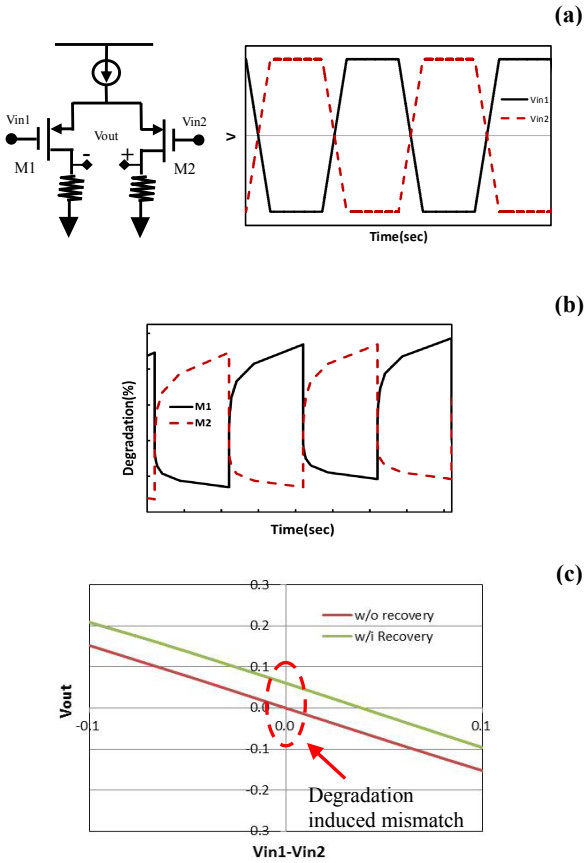
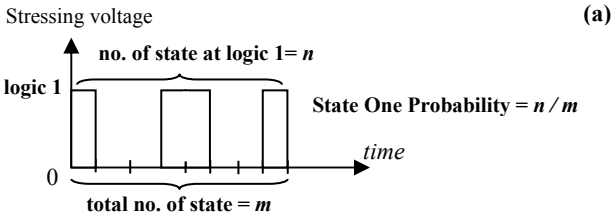


Fig.9a The stress waveform applied to the differential amplifier. Fig.9b The degradation of the differential pair. Fig. 9c The differential output voltage with and without recovery effect

A cell level study is done by applying different state one probability (SP1) as shown in Fig.10a to the input of the PMOS dominated timing arc of a combination logic while the other input are kept constant. The normalized delay degradation under different SP1s is shown in Fig.10b. As expected, different SP1 results in different amount of D_r. However, as shown in the figure, the delay time shift is not a linear function of SP1. Thus it not easy to project delay based on SP1 estimation.



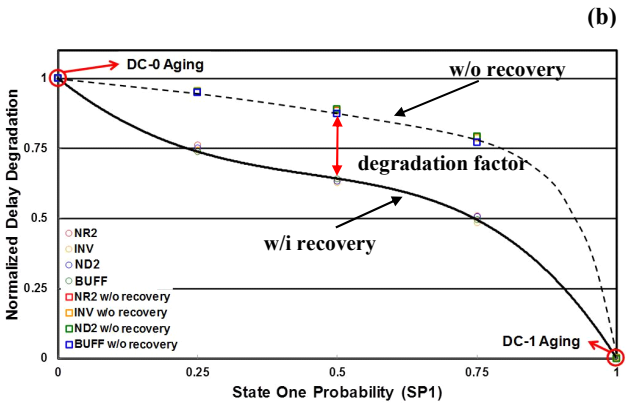


Fig.10a State One Probability (SP1) means that in a time duration, the portion of states at logic 1. Fig.10b The normalized cell level delay degradation under different SP1. SP1 equal to 0 and 1 means that the input signal pulse applied to PMOS is kept stress and unstress, respectively all the time.

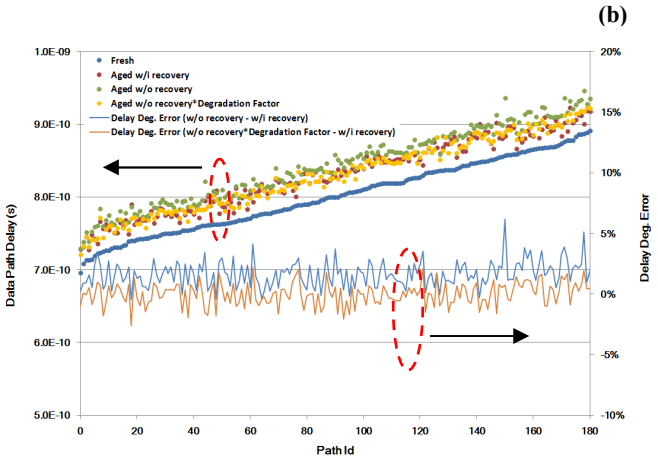
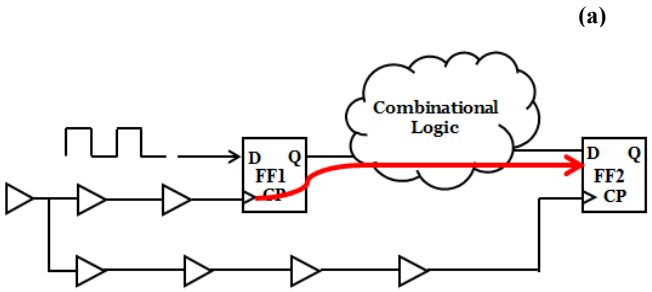


Fig.11 (a) Timing path extraction and AC signal propagation. (b) Timing path simulations with Fresh (before stressing), aging model (i) with recovery, (ii) without recovery, and (iii) without recovery but with a degradation factor.

A path level study is shown in the following. Critical paths are selected from a CPU design and stressed in aging simulations as shown in Fig.11a. After stressing, the data path delays are measured. In Fig. 11b, three cases are considered in aging simulations (i) with recovery, (ii) without recovery, and (iii) without recovery effect but with a degradation factor (the ratio of delay degradation without and with recovery effect at SP1=0.5), as shown in Fig. 10b, to approximate the recovery effect. Let's take (i) as the reference and compare it with (ii) and (iii). As illustrated in Fig.9b, (ii) is too pessimistic and the max error in this case is about 6%. On the other hand, although using a degradation factor, e.g. NBTI factor [5], to include the recovery effect as shown in (iii) is simple, it can under or over-estimate the data path delay. Thus, to accurately characterize the data path delay in aging simulations, bias and frequency dependent recovery effect has to be taken into account. This cannot be simply included by using a pre-determined degradation factor.



IV. Conclusions

We have proposed a model and simulation methodology for BTI recovery effect. The model shows good matching with the measurements. It has been implemented in TMI and is readily linked with SHE to achieve higher accuracy. This model is useful to optimize design while still ensuring reliability robustness.

References

[1] M.C. Jeng, C. Hsiao, K.W. Su, C. K. Lin, "Circuit Reliability Simulation Using TMI2", IEEE CICC, pp.1-7, 2013;

[2] W.K. Lee, K. Huang, J. Liang, J.Y. Chen, C. Hsiao, K.W. Su, C.K. Lin, M.C. Jeng, "Unifying Self-heating and Aging Simulations with TMI2", SISPAD, pp.333-336, 2014;

[3] http://www.si2.org/

[4] Y.S. Tsai, N. K. Jha, Y.-H. Lee, R. Ranjan, Wayne Wang, J.R. Shih, M. J. Chen, J.H. Lee and K. Wu, "Prediction of NBTI Degradation for Circuit under AC Operation", in Proc. IEEE Int. Rel. Phys. Symp., May 2010, pp.665-669;

[5] S. Roy, D.Z. Pan, "Reliability aware gate sizing combating nbti and oxide breakdown," in Proc. of Int'l Conf. on VLSI Design and Embedded Systems, 2014, pp. 38–43.