Does a Nanowire Transistor Follow the Golden Ratio?

A 2D Poisson-Schrödinger / 3D Monte Carlo Simulation Study

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***Abstract*—In this work, we observed the signatures of isotropic charge distributions showing the same attributes as the golden ratio (Phi) described in art and architecture, we also present a simulation study of ultra-scaled n-type silicon nanowire transistors (NWT) for the 5nm CMOS application. Our results reveal that the amount of mobile charge in the channel is determined by the device geometry and could also be related to the golden ratio (Phi). We also established a link between the main device characteristics, such as a drive and leakage current, and cross-sectional shape and dimensions of the device. We discussed the correlation between the main Figure of Merit (FoM) and the device variability and reliability.**

Keywords— Golden ratio, nanowire transistors, Poisson-Schrödinger, simulations, quantum confinement

I. INTRODUCTION

In mathematics, two quantities follow the golden ratio (Phi) if their ratio is the same as the ratio of their sum to the larger of the two quantities. The value of Phi is $\varphi = (1 + \sqrt{5})/2 = 1.618$. The golden ratio appears in some patterns in nature, including the spiral arrangement of leaves and other plant parts, human and animal's bodies, It can also be observed in art, architecture and mathematics [6]. More recently, the signature of the Golden ratios (Phi) has been extended to the periodic system and also to nanotechnology [1]. For example, recently researchers have reported specific signatures showing the same attributes as the golden ratio hidden in solid state matter [1].

The research to date has tended to measure the Phi at nanoscale rather than studying in simulation the impact of this ratio on the performance of Nanodevices. In addition, no research has been conducted in relation to the Phi signature in the novel Nanoelectronic devices such as gate all around (GAA) nanowire transistors (NWTs).

GAA NTWs are a promising device architecture for the next generation technology node and are expected to succeed the FinFET technology in the 5nm technology node due to their superior electrostatic integrity [2]. In nanotransistors, the optimal trade-off between performance and leakage currents can be achieved by engineering the device structures. In our previous publications [3], [4], we demonstrated that the cross-sectional shape of the nanowires has a strong impact on the gate capacitance and the mobile charge in the NWTs. In particular, the NWT with <110> channel orientation and elongated elliptical cross-section with the long diameter parallel to the silicon wafer surface has the highest mobile charge for a given gate voltage [4]. The ratios of the major axis to the minor axis (cross-section aspect ratio (AR) have been identified as an important contributing factor for the device performance. However, a critical design question, including the optimal NWT cross-sectional aspect ratio, remains unanswered.

II. DEVICE DESCRIPTION

Fig. 1 shows the 3D representation and materials details for the NWTs simulated in this work. The Si channel is wrapped by a 0.4nm SiO_2 interfacial layer and a 0.8nm HfO_2 (High-k) layer at the gate region. The doping concentration in the channel is $10^{14}/cm^3$, in extensions $10^{20}/cm^3$, and in the source/drain $4x10^{20}/cm^3$. The direction of charge transport is aligned along the x-axis. Table 1 contains the cross-sectional dimensions for nine elongated elliptical nanowires with the identical cross-sectional areas of 10π nm^2. The NWT diameter along the y-axis varies from 4.44 nm to 9 nm while the corresponding diameter along z-axis varies from 9 nm to 4.44 nm. As a result, the corresponding aspect ratio varies from 2.02 to 0.49. The cross-section dimensions include wires with Phi and 1/Phi values.

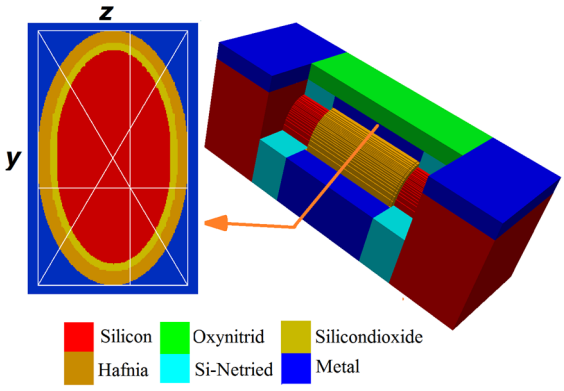

Fig. 1. 3D representation of NWTs with a cross section of 5nm x 8.1 nm. The white lines show the golden ratio drawn in the cross-section in the middle of the channel.

Table 1 Physical cross-section dimensions of simulated devices.

Z(nm)x Y(nm)	Y/Z	Area (nm^2)
4.44x9	2.02	10π
5x8.1 (**Phi**)	1.62	10π
5.7x7	0.81	10π
6x6.66	0.90	10π
6.32x6.32	1.00	10π
6.66x6	1.11	10π
7x5.7	1.22	10π
8.1x5 (**1/ Phi**)	0.62	10π
9x4.44	0.49	10π

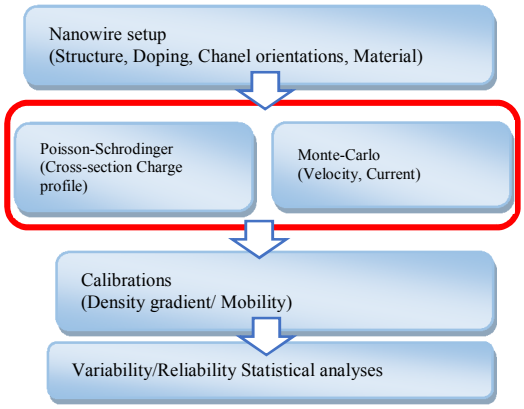

Fig. 2. The simulation tool calibration flow chart.

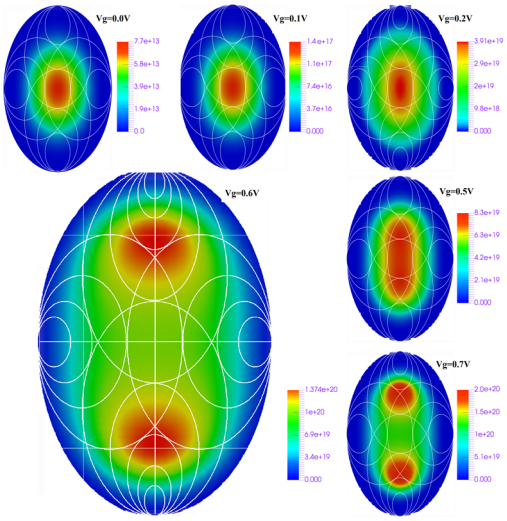

Fig. 3 Comparison of the Phi ovals (white lines) with the charge distribution in the 5 nm x 8.1 nm nanowire cross-section obtained from the Poisson-Schrödinger simulations.

I. METHODOLOGY

In this paper, we deploy both ensemble Monte Carlo (MC) and drift-diffusion simulation techniques with Poisson-Schrödinger (PS) quantum corrections. The flowchart in Fig. 2 illustrates the overall simulation methodology. The quantum corrected MC simulations that capture the non-equilibrium transport effects deliver predictive simulation results. The drift-diffusion simulations, calibrated against the MC results, are used to capture the contact resistance effects. They also can be used to study relative changes in I_{on} for design optimisation and for the efficient statistical variability (SV) and statistical reliability (SR) simulations.

II. RESULTS AND DISCUSSION

The Poison Schrödinger quantum corrections provide an accurate charge distribution in the channel of the simulated NWTs. Fig. 3 shows the Phi ovals plotted on a 2D cross-section at the middle of the gate. The trends of isotropic charge distributions obtained from the Poisson-Schrödinger simulations show the same attributes as the golden ratio. Although the charge distributions are voltage dependent, the signatures of the golden ratio oval are observed at all gate voltages.

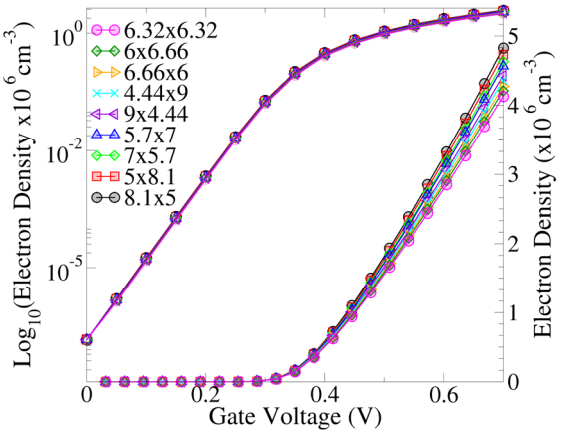

Fig. 4 Gate voltage versus the mobile charge in the channel for the NWTs with different cross sections. The crystallographic channel orientation is <110>.

In order to fairly evaluate the impact of the NWT cross-section dimension on the device performance, Fig. 4 shows the gate voltage versus the mobile charge in the channel for the NWTs shown in Table 1. The Q_M-V_G curves are aligned by modifying the gate work function. Note that the mobile charge is estimated in the middle of the channel. Important conclusions can be obtained from Fig. 4: the NWT with Phi and 1/Phi has the highest amount of the quantum charge in comparison to all other NWTs. Also, the NWT with the perfect circular cross section has the lowest amount of charge in the channel if compared to all other elliptical devices.

Table 2 and Table 3 compare the simulated gate capacitance (C_G) and the mobile quantum charge in the channel per-unit-length (Q_M) at a particular gate voltage V_G for two crystal orientations, <110> and <100> correspondingly. Q_M is directly proportional to the NWT gate capacitance, according to the following expression; $Q_M = C_G(V_G - V_T)$ where V_T is the threshold voltage, and V_G is the gate voltage. Therefore, the reduction of the NWT gate capacitance reduces the mobile charge in the channel and, hence, the transistor performance. From the data presented in both tables it is clear that for both crystal orientations the capacitance is the highest for the wires that follow the golden ratio. Also for the wires with <100> channel orientation, the charge in the Phi and 1/Phi cases is almost identical due identical effective masses in the Y and Z directions.

Table 2 Q_M/C_G ratio at identical Q_M (V_G=0.0V) for NWTs with crystallographic channel orientation <110>.

Z(nm)x Y(nm)	Q_M ($\times 10^7$/cm)	C_G (10^{-10}F/cm)	Q_M/C_G (10^{17}/F)	
<110>				
4.44x9	2.7330	1.1401	2.397	Oblate NWT
5x8 Phi	2.8420	1.1474	**2.476**	Oblate NWT
5.7x7	2.7500	1.1290	2.435	Oblate NWT
6x6.66	2.5801	1.1093	2.326	Oblate NWT
6.32x6.32	2.5480	1.1092	2.297	Circular
6.66x6	2.6316	1.1168	2.356	Prolate NWT
7x5.7	2.7738	1.1352	2.440	Prolate NWT
8x5 (1/Phi)	2.8929	1.1602	**2.491**	Prolate NWT
9x4.44	2.7270	1.1371	2.398	Prolate NWT

Table 3 Q_M/C_G ratio at identical Q_M (V_G=0.0V) for NWTs with crystallographic channel orientation <100>.

Z(nm)x Y(nm)	Q_M ($\times 10^7$/cm)	C_G (10^{-10}F/cm)	Q_M/C_G (10^{17}/F)	
<100>				
4.44x9	2.7322	1.1350	2.4072	Oblate NWT
5x8.1 Phi	2.8900	1.1597	**2.4920**	Oblate NWT
5.7x7	2.7794	1.1384	2.4441	Oblate NWT
6x6.66	2.6403	1.1184	2.3607	Oblate NWT
6.32x6.32	2.6102	1.1166	2.3376	Circular
6.66x6	2.6402	1.1180	2.3615	Prolate NWT
7x5.7	2.7793	1.1380	2.4422	Prolate NWT
8.1x5 (1/Phi)	2.8910	1.1598	**2.4910**	Prolate NWT
9x4.44	2.7321	1.1341	2.4090	Prolate NWT

Fig. 5 compares the I_D-V_G characteristics of the simulated NWTs. Consistent with the data presented so far, the NWTs with the cross-section equal to Phi or 1/Phi show the highest ON-current. This is valid for low and high drain voltage.

Fig. 6 reveals the intrinsic delay τ as a function of the gate length. The intrinsic delay τ can be directly correlated to the speed of the device. The speed of NWTs in terms of the intrinsic delay is defined as follow: $\tau = C_G(V_{DD}/I_{eff})$, where C_G is the total gate capacitance, $I_{eff}=(I_H+I_L)/2$ is the effective current where $I_H=I_D(V_G=V_{DD}, V_D=V_{DD}/2)$ and $I_L=I_D(V_G=V_{DD}/2, V_D=V_{DD})$, V_{DD}=0.6V. The leakage current is I_{off}=0.6 µA/µm. Fig. 6 shows that the NTWs with 8.1nm x 5nm and 5nm x 8.1nm have the smallest intrinsic delay. The evaluation of the intrinsic delay agrees with the results of Q_M/C_G presented in Table 2.

Fig. 7 shows the design of experiments including the effect of gate lengths and effective oxide thickness, and NWT cross-sectional dimensions on DIBL, I_{off}, I_{on} and V_T. In this case, we consider only <110> channel orientation. The obtained data shows that the highest value of the drive current occurs for the NWT with the shortest gate length and EoT. In addition to changing the NWTs' geometry and channel orientation, the electron transport properties in Si NWTs could be improved by introducing a strain in the channel [5].

Fig. 8 shows simulated I_D-V_G characteristics of a 5 nm x 8.1 nm (Phi) NWT with a channel orientation of <110> at four different strain values. From the same figure, it can be concluded that introducing the channel strain indeed improves the saturation current magnitude between 5% and 35%. Applying the 2GPa tensile strain improves the NWT performance by 35% if compared with the unstrained NWT.

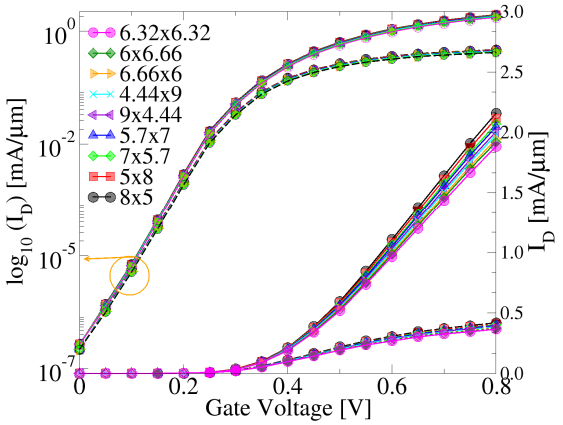

Fig. 5 The impact of the nine-cross-section aspect ratio on the I_D-V_G curves. Dashed lines are at V_D=0.05V, and solid lines are at V_D=0.7V. The crystallographic channel orientation is <110> with L_G= 12 nm.

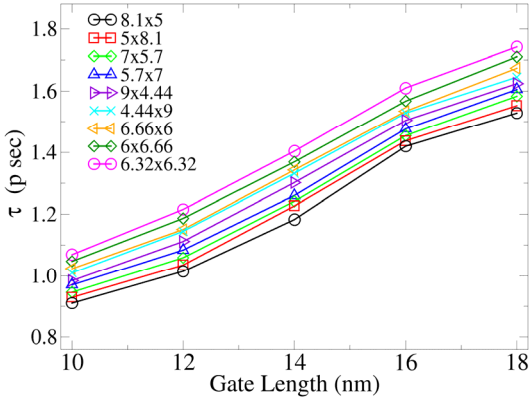

Fig. 6 Impact of five different gate lengths on the intrinsic delay (τ) for devices with nine different cross-section aspect ratios including Phi and 1/Phi. The crystallographic orientation of the channel is <**110**>.

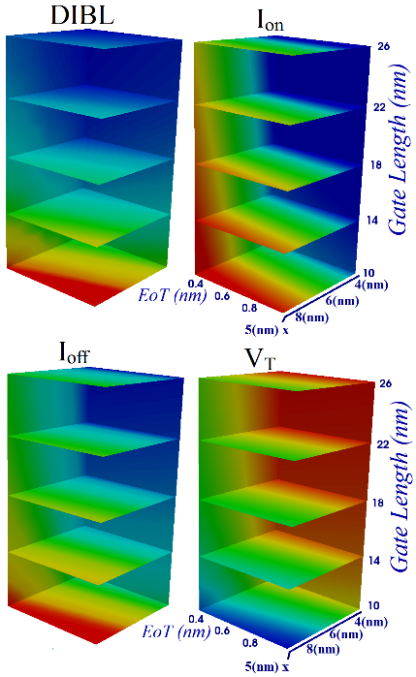

Fig. 7 Design of experiment for NWT and the effects of the size, gate lengths and effective oxide thickness on DIBL, I_{off}, I_{on} and V_T.

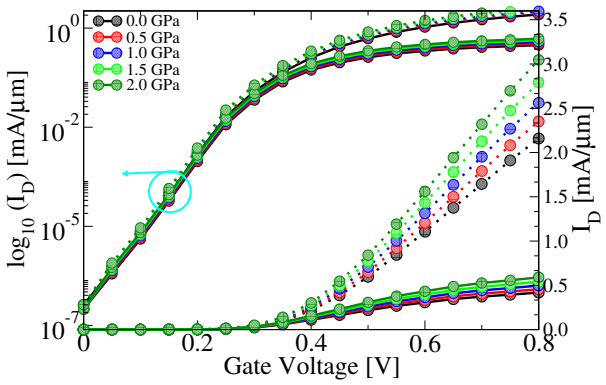

Fig. 8 I_D-V_G curve compares results for the 5nm x 8.1nm strained silicon NWT at four different channel stains. Dashed lines correspond to a high drain voltage V_D=0.7V, while the solid lines are for a low drain voltage V_D=0.05V. The gate length is 12 nm. The crystallographic channel orientation is <110>.

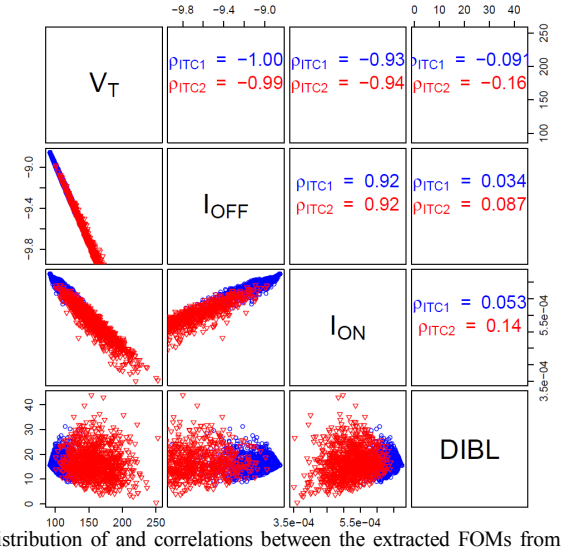

Fig. 9 Distribution of and correlations between the extracted FOMs from the TCAD simulations of an individual ITC; ITC1= 1x10^{12} cm^{-1} and ITC2= 4x10^{12} cm^{-1} without sources of SV.

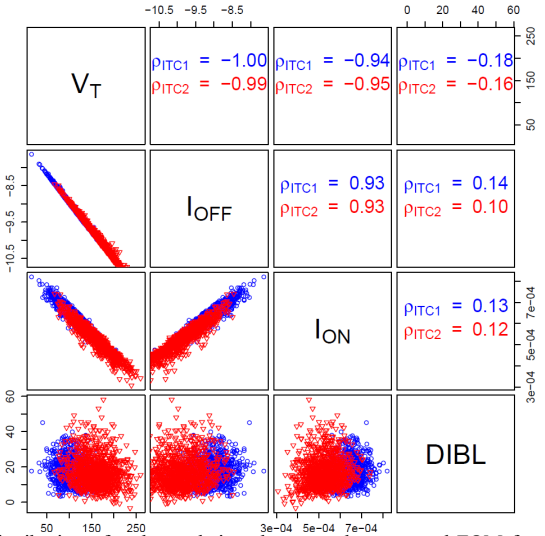

Fig. 10 Distribution of and correlations between the extracted FOM from the TCAD simulations of an individual ITC; ITC1= 1x10^{12} cm^{-1} and ITC2= 4x10^{12} cm^{-1} with sources of SV (RDD, WER, MGG).

In current nanoscale transistor technology, the variability is becoming more important due to the process deviation and the intrinsic properties of semiconductor materials and interfaces. There are numerous sources of statistical variability (SV), such as random discrete dopants (RDD), wire edge roughness (WER), and metal gate granularity (MGG), which dominate the NWT behaviour. Fig. 9 and Fig. 10 show the distribution of and the correlations between extracted figures of merit (FoM) from the TCAD simulations. Fig. 9 presents the correlation plot for the degraded NWT with a trap sheet density of 1x10^{12} cm^{-2} and 4x10^{12} cm^{-2} and Fig. 10 presents the correlation plot of FoM when variability sources (RDD, WER, MGG) are considered together with the two degradation levels. Both figures show a correlation between the V_T, I_{OFF} and I_{ON}. However, there is no correlation between DIBL and the other FoM.

III. Conclusions

In this paper, for the first time, we presented a detailed simulation of the impact of Phi on the electrostatics and device performance of n-type silicon nanowire transistors for the 5nm CMOS applications. Our work revealed that the NWTs shape with the aspect ratio equal or close to the golden ratio (Phi) could improve the gate capacitance and the mobile charge in the channel and intrinsic speed of the device. We observed that the highest mobile charge for a given gate voltage is delivered by an elongated elliptical nanowire with the aspect ratio equal to the golden ratio. We also discussed the impact of the gate length on the time delay and the main FoM, such as V_T, I_{OFF} and I_{ON} and DIBL. The paper also revealed the impact of various sources of statistical variability on the same main FoM.

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