

Finite-difference methodology for full-chip electromigration analysis applied to 3D IC test structure: simulation vs. experiment

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Abstract—A novel electromigration (EM) assessment method based on a finite-difference (FD) approach has been implemented to study EM degradation in 3D integrated circuit (IC) supply current ports. A dual damascene copper through-silicon via (TSV) based EM test structure was used, which consisted of redistribution (RDL) and M1 metal layers connected by four TSVs on one side and a single TSV on the other side. The mean-time-to-failure (MTF) obtained with FD simulation agrees well with the MTF found using a finite-element analysis (FEA) method as well as with the measured MTF. The results demonstrate that the EM-induced MTF in 3D IC structures can be correctly predicted with FD simulations, by representing them as combinations of 1D interconnect branches with suitable boundary conditions (BC) for the branch junctions.

Keywords—*electromigration, finite-difference and finite element analysis, hydrostatic stress, diffusion.*

I. INTRODUCTION

The EM phenomenon is the directional migration of lattice atoms and defects under the action of an electric field and current. This forced redistribution of atoms can lead to non-uniformity in chemical composition, and can introduce non-uniform elastic/plastic deformation and stress. Over time, voids may be formed at locations with high tensile stress in power delivery grids, which results in a resistance increase and IR-drop degradation [1]. The failure criterion for the power/ground (p/g) grid is a voltage drop exceeding a user-specified threshold; the voltage drop is increased as a result of EM-induced resistance increase. This voltage drop threshold would correspond to a critical reduction in the supply voltage for some gate, somewhere on the layout, which affects the cell functionality and violates timing constraints. A dynamic simulation of EM-induced IR-drop degradation in p/g grids was proposed as a methodology of EM assessment for large integrated circuits (ICs) in [2].

Standard practice employed in the industry for EM assessment is to break up a grid into isolated metal branches, assess the reliability of each branch separately using Black's

model and then use the series model (earliest branch failure time) to determine the failure time for the whole grid. Black's model ignores the material flow between branches. However, in today's mesh structured p/g grids, many branches within the same metal layer may be connected, leading to a so-called interconnect tree (IT) structure, and atomic flux can flow freely between the branches of an IT. An efficient physics-based full-chip EM assessment approach has been proposed in [2], which accounts for the material flow and the coupled stresses within an IT. This method decomposes the power grid into a number of interconnect trees, solves the set of PDEs (Korhonen's equations, [3]) for all branches of every tree characterized by different current densities and geometries (length and width), and links the solutions to each other through suitable BC at the segment junctions, which capture the continuity of stress and atomic fluxes. An accurate simulation of stress evolution was combined with a saturated void length model: it was assumed that a void size achieves saturation immediately after the void is nucleated.

The one-dimensional nature of Korhonen's equation is the main simplification, and potential concern of this simulation approach. In modern dual damascene interconnect structures, the stress distribution and void shape evolution at the metal line-via junctions have an essentially three-dimensional character. Thus, the validity of using a 1D FD approach for EM analysis should be justified.

In this work, the FD approach was implemented for the first time for EM assessment in TSV based 3D IC structures. The methodology developed in [2] was enhanced by a simulation of the voiding kinetics, which provides more accurate estimation of the resistance change during the void evolution. To demonstrate our approach we have chosen test structures characterized by the high level of redundancy. An interplay between growth kinetics of voids and electric current redistribution through the TSVs has allowed us to reproduce the experimentally measured ratio of MTFs occurring in the two cases of upstream and downstream current. The redundancy that's part of the TSV structure has allowed us to verify the

validity of the EM failure criterion based on IR-drop degradation. Based on the results of this work, additional rules were developed for improved construction of 1D ITs that more accurately model the EM phenomena in 3D structures.

II. EXPERIMENT: TEST STRUCTURE AND EM ANALYSIS

The dual damascene copper TSV based EM test-structure consists of RDL and M1 metal layers connected by four TSVs on the right, and a one TSV on the left, as shown in Fig. 1a. At the RDL level, both ends are connected to current supplying pads. The RDL thickness is 1 μm , and width is 14 μm , while the M1 layer thickness is 0.25 μm . The M1 width is 4 μm for a segment of $\sim 500 \mu\text{m}$ length, and 7 μm for the pads under TSVs. The TSV is 3 μm in diameter and 18 μm in height. There is a TiN diffusion barrier at the TSV/M1 interface. The applied currents have led to EM voids in the pads under TSVs in the M1 layer only.

EM tests were performed in two ways: a down-stream case, where the electron flow was from RDL to M1 in the single (left) TSV, and an up-stream case, with reversed current flow, [4]. For down-stream tests, EM failure was caused by voiding under the left TSV, while for up-stream tests EM failure was caused as pad voiding under all four TSVs on the right end, as shown in Fig. 1b.

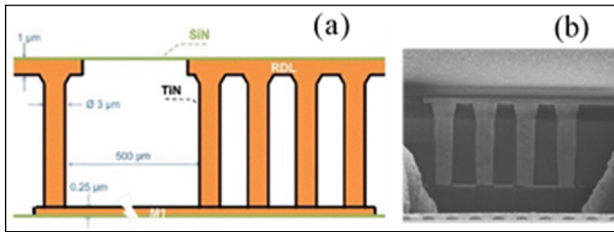


Fig. 1. EM test structure cross section view: (a) a schematic, and (b) SEM image showing multiple voiding under TSVs.

A 10 % resistance change was used as the failure criterion. For applied current values in the range of 10-25 mA, and test temperatures in the range of 250-350 $^{\circ}\text{C}$, the measured MTF ratio $MTF^{up-str} / MTF^{down-str}$ was in the range of 2.6-3.7 instead of the expected 4.0. This can be explained by the effect of TSV redundancy on EM lifetime, as will be shown below.

III. FEA STUDY OF THE TEST STRUCTURE

An accurate FEA of EM in the above test structure has allowed us to simulate the detailed stress evolution and voiding dynamics in both the down-stream and up-stream cases. This was based on a vacancy model for atomic transfer with proper accounting for generation and annihilation of vacancy/plated atom pairs at interfaces and grain boundaries [5]. Distribution of the current density inside the structure was found by solving a Laplace equation for the electric potential.

A critical value of hydrostatic stress created by vacancies and plated atoms was assumed to be responsible for void nucleation at the locations of pre-existing flaws. Growth of the nucleated voids, caused by inflow of vacancies driven by both stress gradient and electric current, was simulated by employing the phase-field method. The latter was coupled with the

elasticity equation for stress evolution and the Laplace equation for electric potential, for describing stress and electric current re-distribution due to voiding in M1 pad. The system of differential equations describing the current distribution, evolution of vacancy and plated atom concentrations, mechanical stress generation, and void surface motion was solved numerically using the Comsol Multiphysics FEA software. The details of FEA simulations were described in [5].

The simulations of EM in the M1 layer demonstrated fast growth of the tensile stress for the down-stream configuration, when voiding in the left pad under the single TSV is observed. The wide pads under TSVs are responsible for the reservoir effect for vacancies accumulated near the cathode. The different sizes of the pads, 7 μm length for the left pad and 28 μm for the right pad, are responsible for different void nucleation times for up-stream and down-stream cases. Despite the small sizes of the pads, in comparison with the length of the M1 line connecting the pads ($\sim 500 \mu\text{m}$), the effect of pad length is significant in the electric current range that was used. This is because the critical stress in the pad is generated when tensile stress is developed only in immediate vicinity of the cathode (Fig. 2), mainly in the pad region. The simulated ratio of void nucleation times $t_{nuc}^{up-str} / t_{nuc}^{down-str}$ from the interval of 2.5-3.3 was obtained by varying the values of critical stress, atomic diffusivity, and electric current.

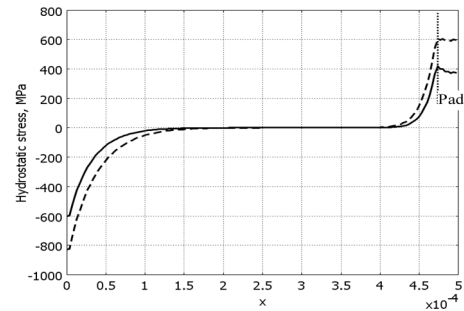


Fig. 2. Pre-voiding hydrostatic stress developed in up-stream configuration, for critical stress values 400MPa (solid line) and 600 MPa (dashed line).

Voiding kinetics were essentially different for the two studied cases. For the down-stream case, a void was nucleated and propagated under the single TSV attached to the pad. Undercutting this TSV has immediately forced the electric current to flow through the TiN liner, which increased the circuit resistivity.

For the up-stream case, different sequences of TSV failures were found, depending on values of the model parameters. The most probable voiding site is located under the first TSV, where current crowding (Fig. 3a) and the fastest stress growth rate were observed. However, in the case of high critical stress a uniform stress distribution in the pad can be established (Fig. 2); in this case the voiding site is determined mainly by the distribution of imperfections in the metal.

In the simulations, we used critical stress values in the range of 400-500 MPa. In this case, the first void appears under the first TSV, which corresponds to experimental observations. Failure of the first TSV (Fig. 3b), which means a cut of the electrical connection between TSV and M1 by a void, increases

the current density in other TSVs (Fig. 3c), causing their sequential failure, as shown in Fig. 3d.

Thus, EM failure of the pad with four TSVs has taken longer to happen than failure of the pad with single TSV, due to two main factors: (i) larger size of the right side pad delayed the tensile stress development at the cathode side, and (ii) the sequential failure of four TSVs was required to achieve circuit failure. As a result, the 10 % resistivity increase in the up-stream case took ~ 3.5 times longer than in the down-stream case, where failure is caused by a void under the single via.

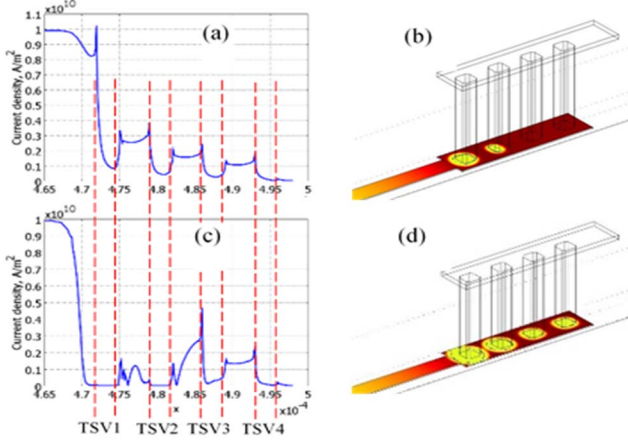


Fig. 3. FEA results for up-stream configuration showing (a) initial current distribution, (b) first TSV failure, (c) current distribution after failure of two TSVs, and (d) the circuit failure. A color map in (b) and (d) corresponds to the value of hydrostatic stress: yellow is zero, the darker red means higher tensile.

Unfortunately, the FEA based approach is computationally expensive and so is not applicable to large circuits. In the next section, we demonstrate the capability of the FD approach to predict EM lifetimes in the above 3D structure, based on the 1D EM model. The results of the FEA approach and the experimental results have been used to verify the quality of the FD approach.

IV. EM ASSESSMENT WITH THE FINITE DIFFERENCE APPROACH

A. General approach

In the 1D approach, EM induced hydrostatic stress σ can be obtained from the volumetric strain θ_v , generated by extra atoms as $\sigma = B\theta_v$, where B is the effective bulk modulus of the confined metal. Then, as shown in [5], assuming fast equilibration of vacancies with stress, the vacancy model of EM used in FEA study can be reduced to Korhonen's equation for the kinetics of hydrostatic stress. In interconnect trees, the stress evolution at any point the in k -th branch, with electric current j_k , is governed by the PDE:

$$\frac{\partial \sigma_k}{\partial t} = \frac{B\Omega}{k_B T} \frac{\partial}{\partial x_k} \left[D_a \left(\frac{\partial \sigma_k}{\partial x_k} - \frac{eZ\rho j_k}{\Omega} \right) \right] \quad (1)$$

Here, t is time, $D_a = D_0 \exp[-Q/(k_B T)]$ is atomic diffusivity, where Q is the diffusion activation energy, k_B is the Boltzmann's constant, T is temperature in Kelvin, eZ is the

effective charge of migrating atoms, ρ is the metal resistivity, Ω is the atomic volume, $x_k \in (0, l_k)$ is the coordinate along the branch k , where l_k is the branch length. By introducing dimensionless quantities, all branches can be uniformly discretized into N segments, and equation (1) can be written in the finite-difference form:

$$\frac{d\eta_{k,j}}{d\tau} = \theta_k \left[\frac{\eta_{k,j+1} - 2\eta_{k,j} + \eta_{k,j-1}}{(\Delta\xi)^2} \right] \quad (2)$$

Here, the central difference formula for space derivative is used together with dimensionless quantities:

$$\tau = \frac{B\Omega}{k_B T} \frac{D_a t}{l_c^2}, \quad \eta_k = \frac{\Omega \sigma_k}{k_B T}, \quad \xi_k = \frac{x_k}{l_k}, \quad \theta_k = \left(\frac{l_c}{l_k} \right)^2, \quad \Delta\xi = \frac{1}{N}$$

and l_c is an arbitrary characteristic length.

The employed segment junction BCs are the following: (a) atomic flux is zero at diffusion barrier (tree end) when there is no void, (b) across branch junctions the incoming atomic flux is equal to the outgoing atomic flux, and stress is continuous when there is no void there, and (c) the hydrostatic stress vanishes at the void surface when void nucleates.

Void growth is modelled based on atomic flux at the void surface. An increase of the void length located at an arbitrary node of k -th branch, during a time interval Δt is

$$\Delta L_k^{void} = \frac{D_a \Omega}{k_B T} \left(\frac{\partial \sigma_k}{\partial x_k} \Big|_{x=x_s} - \frac{eZ\rho j_k}{\Omega} \right) \Delta t \quad (3)$$

The contribution of the first term in (3), describing the stress gradient at the void surface ($x = x_s$), is dominant immediately after void nucleation. After the stress relaxation has happened the second term becomes responsible for void surface motion. The growing void forces the electric current to flow through the high-resistance liner, thus increasing the resistance of the voided branch and changing node voltages. The circuit is deemed to have failed when the voltage drop exceeds some critical value. Therefore, the implemented iterative lifetime simulation flow is summarized as follows:

- (1) Read inputs: resistor R_k netlist, DC current sources, technology parameters, and failure criterion.
- (2) Construct interconnect trees, and discretize branches.
- (3) Assign BCs for all branch junctions and tree ends.
- (4) $t = 0$: calculate j_k and node voltages ($V_{\text{node},k}$).
- (5) Obtain hydrostatic stress.
- (6) Identify voiding site where $\sigma \geq \sigma_{\text{cr}}$; get the void size.
- (7) Is the failure criterion reached?
 - if yes, print lifetime and exit,
 - if no, $t_{\text{new}} = t + \Delta t$; update void size, R_k , j_k and V_{node} .
- (8) Continue iteration: back to (5).

A very efficient method for solving the discretized equations (2) developed in [2] allows fast analysis of large p/g interconnect networks. In order to apply the 1D FD approach for simulating the voltage degradation in the 3D structure shown in Fig. 1, we need to implement an IT construction algorithm that can properly describe voiding kinetics for the upstream configuration observed in FEA study. The large width of the pad, in comparison to the TSV contact areas should be accounted for, in order to describe the sequential failure of vias: wider pad provides a path for atoms to migrate when a void undercuts the bottom of the first TSV (Fig.4).

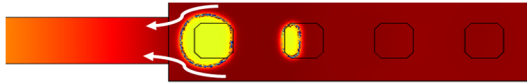


Fig. 4. Atomic migration paths in the pad (arrows) after failure of the first TSV.

B. Construction of trees and pad model

Since the diffusion barrier separates the TSV layer from M1, but there is no barrier between RDL and TSV layers, three interconnect trees (trees 0, 1, 2) were constructed, as shown in Fig. 5. Nodes are defined at each end and junction of branches. To overcome the 1D nature of void model, two additional nodes (N14, N15) are introduced in order to implement a void-void interaction. When the size of a void at the bottom of the first TSV (node N9) reaches the entire TSV cross section, the TSV is electrically blocked. Electric current continues to flow through M1, as the void did not fully destroy the conductance. It also did not affect the atomic transport away from the bottom of the second TSV (N8), which is now a major electron flow inlet into M1. But, the existing void at N9 slows down the pre-voiding tensile stress buildup at N8 and the growth of the void nucleated at N8 due to a quasi-reservoir effect. To depict this interaction, we introduced an additional artificial branch N15-N8, connected to N8. Similarly, voiding at nodes N7 and N6 was obtained, and the failure of the structure in the up-stream case has been simulated.

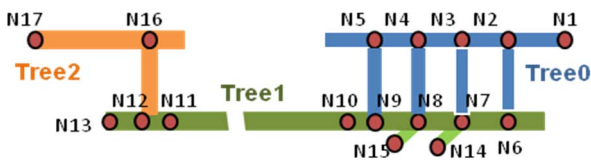


Fig. 5. EM test structure: construction of trees for FD simulation.

C. FD simulation results

To compare the simulation results with measurements, we performed two simulation runs for up-stream and down-stream electric current directions. The EM stress conditions included $i = 10 \text{ mA}$ and $T = 300 \text{ }^\circ\text{C}$. The other parameters used are $\rho_{Cu} = 4.0 \cdot 10^{-8} \text{ ohm} \cdot \text{m}$, $\rho_{TiN} = 1.31 \cdot 10^{-7} \text{ ohm} \cdot \text{m}$, $Q = 1.6 \cdot 10^{-19} \text{ J}$, $\Omega = 1.18 \cdot 10^{-29} \text{ m}^3$, $B = 1 \cdot 10^{10} \text{ Pa}$, $k_B = 1.38 \cdot 10^{-23} \text{ J/K}$, $Z = 10$, $e = 1.6 \cdot 10^{-19} \text{ q}$, $D_o = 7.56 \cdot 10^{-5} \text{ m}^2/\text{s}$, and $\sigma_{cr} = 500 \text{ MPa}$. In both the up-stream and down-stream cases, EM resulted in voiding only in tree 1, as the current density is larger in M1 line due to the small cross section. Stress evolution in the down-stream case (Fig. 6a) shows that voiding occurs at $t \sim 63$ at node N12 under the single TSV. Blocking of

this TSV causes the circuit failure. Resistance vs. time in Fig. 6b shows the lifetime as $t = 463$.

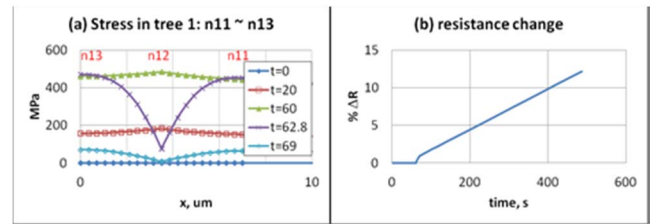


Fig. 6. Simulation results for downstream case: (a) stress evolution in tree 1 (N11~N13), and (b) resistance vs. time.

Stress evolution for the upstream case is shown in Fig. 7, where voiding occurs sequentially at N9, N8, N6 and N7. The ratio of void nucleation times was $t_{nuc}^{up-str} / t_{nuc}^{down-str} \approx 3.3$ almost exactly matching the results of FEA simulations. The lifetime for upstream case is found to be $t = 1711$. The ratio of lifetimes (up/down) is therefore $1711/463 = 3.7$, and is in excellent agreement with the experimental results [4].

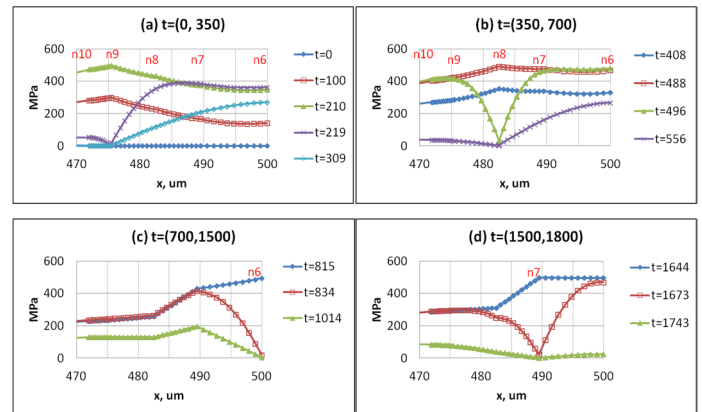


Fig. 7. FD stress profile for the voiding events in upstream case: (a) at N9 ($t=219$), (b) at N8 ($t=496$), (c) at N6 ($t=834$), and (d) at N7 ($t=1673$).

In summary, the implemented 1D-based FD approach for EM assessment represents well the 3D nature of voiding kinetics at M1/TSV junctions.

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