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# 3D MC Simulations of Strain, Channel Orientation, and Quantum Confinement Effects in Nanoscale Si SOI FinFETs

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***Abstract*—An in-house 3D Finite Element (FE) Monte Carlo (MC) toolbox is used to study the effects of uniaxial tensile strain in nanoscale Si $n$-channel SOI FinFETs with two channel orientations ($\langle 100\rangle$ and $\langle 110\rangle$). We simulate a FinFET with a rectangular-like cross-section (4.5 nm$\times$11 nm) and a gate length of 8.1 nm with EOT=0.55 nm and study the effects of two types of tensile strain: uniaxial $\langle 100\rangle$ and uniaxial $\langle 110\rangle$ with strain strengths of 0.5%, 0.7% and 1.0%. To show how quantum confinement can degrade the effectiveness of strain engineering, we compare the results with a bigger device with a rectangular-like cross section (12 nm$\times$30 nm) and a gate length of 25 nm with EOT=1.12 nm. It is found that applying the uniaxial $\langle 100\rangle$ strain increases more the on-current than the uniaxial $\langle 110\rangle$ strain. Moreover, with increasing the strain strength, the quantum confinement induced pre-existing valley splitting starts to weaken the strain effect especially in the $\langle 110\rangle$ channel orientation.**

## I. Introduction

To suppress short channel effects, new device architectures and new materials are increasingly introduced into solutions for mass production in upcoming technology nodes. Multi-gate FETs like FinFETs and nanowire FETs are proven now to be the solutions for sub-10 nm technology because of their superior electrostatic integrity [1]–[3]. Strain engineering, as a well-known performance booster, remains a necessary enhancement option even in the nanoscaled devices. Strain technology can enhance the drain current without decreasing the transistor gate length. Furthermore, the technique is compatible with the new device structures such as multi-gate, SOI and high-$\kappa$/metal gate devices, delivering increase in drive currents [4] without sacrificing too much production cost. This beneficial impact of strain occurs because strain reduces crystal symmetry lifting band degeneracy and allows band warping. Thus more electrons can be driven into the valleys with a light effective mass in the transport direction [5], [6]. However, the effectiveness of strain can be reduced due to the pre-existing quantum confinement induced valley splitting [7].

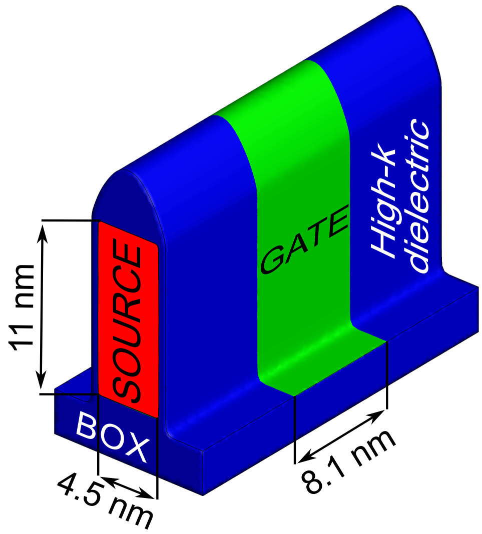


Fig. 1. Schematic of the investigated 8.1 nm gate length $n$-channel Si SOI FinFET (EOT=0.55 nm).

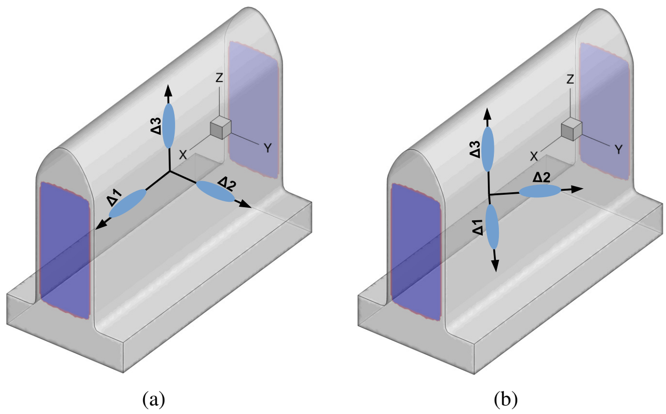


Fig. 2. Conduction band constant energy ellipsoids along $\Delta$ valleys in silicon for (a) $\langle 100\rangle$ and (b) $\langle 110\rangle$ channel orientations. Each of the three ellipsoids is double degenerate.

In this work, we study the effects of strain in nanoscale Si $n$-channel SOI FinFETs with quantum confinement along-side with different channel orientations. The FinFET under study has a rectangular-like cross-section (4.5 nm$\times$11 nm) and a gate length of 8.1 nm with EOT=0.55 nm (Fig. 1). We simulate two different channel orientations: the $\langle 100\rangle$ (Fig. 2(a)) and the $\langle 110\rangle$ (Fig. 2(b)) and study the effects of two types of

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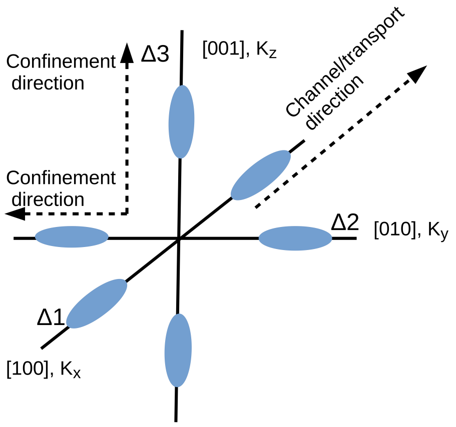


Fig. 3. Six silicon valleys, showing the confinement plane. The transport direction is the $x$-axis.

tensile strain: uniaxial $\langle 100\rangle$ and uniaxial $\langle 110\rangle$ with strain strengths of $0.5\%$, $0.7\%$ and $1.0\%$. To show how the quantum-mechanical confinement can affect the effectiveness of strain engineering, we compare the results with a bigger device with a rectangular-like cross section (12 nm$\times$30 nm) and gate length of 25 nm with EOT=1.12 nm [8].

## II. 3-D Monte Carlo Simulation Toolbox

We apply our in-house 3D Finite Element (FE) Monte Carlo (MC) toolbox which accounts for quantum confinement by using a calibration-free anisotropic Schrödinger equation based quantum corrections (SEQC) [8]–[11]. The simulation toolbox uses anisotropic non-parabolic bandstructure for transport [12] with all Si-related electron scattering mechanisms including interface roughness and ionised impurity scatterings. More details on the 3D MC transport model can be found in Refs. [8], [9], [11], [13]. The finite element (FE) method accounts for the complex 3-D geometry of FinFET device which gives accurate description of the quantum confinement and is capable to take into account all transistor domain including access resistance of the source/drain without need of any post-processing of I-V data [8].

In this work, we study only uniaxial strain since, for the 3-D nanoscale multi-gate FETs, the uniaxial strain (where the strain is applied along the transport direction) is adopted over biaxial strain (where the strain is evenly distributed over the whole surface) because the former can deliver a larger performance improvement [6], [14]. The biaxial strain is becoming more and more difficult to apply in ultra scaled devices. In addition, the threshold voltage change due to uniaxial strain is much smaller which is critical for high-$\kappa$/metal gate devices [15].

To model the effects of strain, the silicon valley edges $\Delta E_{\mathrm{C}}$ are shifted according to the strain type and strain strength [16]. For the uniaxial $\langle 110\rangle$ strain, the effective masses are adjusted for $\Delta 3$ valleys to account for warping due to uniaxial $\langle 110\rangle$ stress resulting in lighter $m_t$ of $\Delta 3$ valleys parallel to the stress [16]. Fig. 3 illustrates the six silicon valleys positioned with respect to the confinement plane and the transport direction ($x$-axis). Table I collects the valley-edge shifts for the $0.5\%, 0.7\%$ and $1.0\%$ tensile strain considered in this work [16].

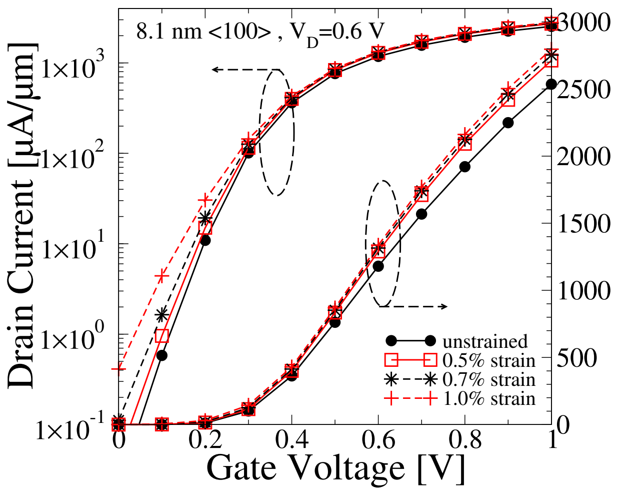


Fig. 4. $\mathrm{I_D}$-$\mathrm{V_G}$ characteristics at $\mathrm{V_D}$=0.6 V in the $\langle 100\rangle$ channel orientation under uniaxial $\langle 100\rangle$ strain with different strengths (8.1 nm gate device).

## III. Strain effects in nanoscaled Si SOI FinFETs

Fig. 4 shows $\mathrm{I_D}$-$\mathrm{V_G}$ characteristics for the $8.1$ nm gate device in the $\langle 100\rangle$ channel orientation under uniaxial $\langle 100\rangle$ strain with a strength of $0.5\%, 0.7\%$ and $1.0\%$ at $\mathrm{V_D}$=0.6 V. The on-current (at $\mathrm{V_G}$=1.0 V) increases by $7\%$, $8.5\%$ and $10.3\%$ under the uniaxial $\langle 100\rangle$ strain with a strength of $0.5\%$, $0.7\%$ and $1.0\%$, respectively. However, we notice some deterioration to the sub-threshold slope under increasing strain conditions. This is because the strain will reduce an overall density of states in the transport directions (as the lighter electron effective mass participation in the transport increases with increasing strain) causing increase in kinetic energy of electrons in the sub-threshold region resulting in the increase of leakage current. Fig. 5 plots the 3 $\Delta$ valleys contributions to the current in the $\langle 100\rangle$ device under uniaxial $\langle 100\rangle$ strain with different strengths to show how different valleys contribute to the current. In the uniaxial $\langle 100\rangle$ strain, $\Delta 1$ conduction band edge

TABLE I. Valley-edge shifts for $\Delta$ valleys in Si with different types and strengths of tensile strain [16].

| Strain type | Uniaxial ⟨100⟩ strain | | | Uniaxial ⟨110⟩ strain | | |
|---|---|---|---|---|---|---|
| strain strength | 0.5% | 0.7% | 1.0% | 0.5% | 0.7% | 1.0% |
| Δ1 | +0.03eV | +0.042eV | +0.06eV | -0.01eV | -0.014eV | -0.02eV |
| Δ2 | -0.045eV | -0.063eV | -0.09eV | -0.01eV | -0.014eV | -0.02eV |
| Δ3 | -0.045eV | -0.063eV | -0.09eV | -0.065eV | -0.091eV | -0.13eV |

TABLE II. Effective-mass tensor and effective transport mass of $\Delta$ valleys for $\langle 100\rangle$ and $\langle 110\rangle$ channel orientations where $1/m^*_{yz}$=0 and degeneracy = 2. Wafer orientation is [100] [9].

| Orientation | Valley | $1/m^*_{yy}$ | $1/m^*_{zz}$ | $m^*_{\mathrm{Tr}}$ |
|---|---|---|---|---|
| ⟨100⟩ | Δ1 | $1/m_t$ | $1/m_t$ | $m_l$ |
| ⟨100⟩ | Δ2 | $1/m_l$ | $1/m_t$ | $m_t$ |
| ⟨100⟩ | Δ3 | $1/m_t$ | $1/m_l$ | $m_t$ |
| ⟨110⟩ | Δ1 | $(m_t+m_l)/(2m_tm_l)$ | $1/m_t$ | $(m_t+m_l)/2$ |
| ⟨110⟩ | Δ2 | $(m_t+m_l)/(2m_tm_l)$ | $1/m_t$ | $(m_t+m_l)/2$ |
| ⟨110⟩ | Δ3 | $1/m_t$ | $1/m_l$ | $m_t$ |

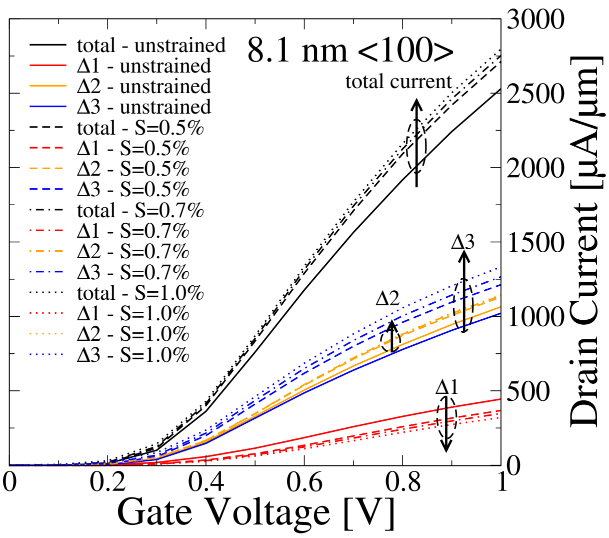


Fig. 5. Valley contributions to the current at $V_D$=0.6 V in the ⟨100⟩ channel orientation under uniaxial ⟨100⟩ strain with different strengths (8.1 nm gate device).

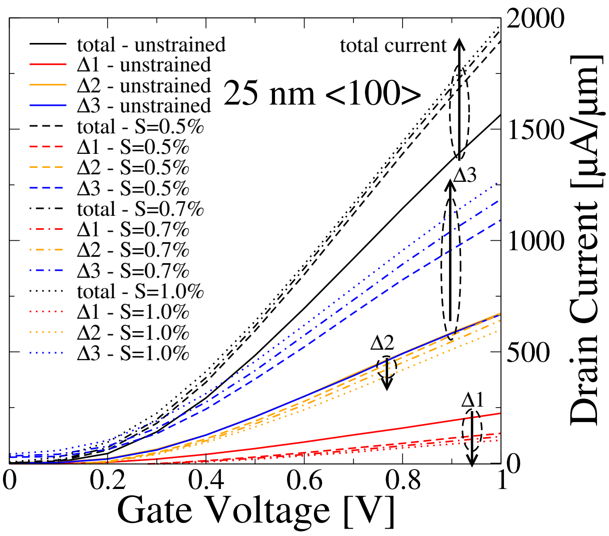


Fig. 6. Valley contributions to the current at $V_D$=1.0 V in the ⟨100⟩ channel orientation under uniaxial ⟨100⟩ strain with different strengths (25 nm gate device).

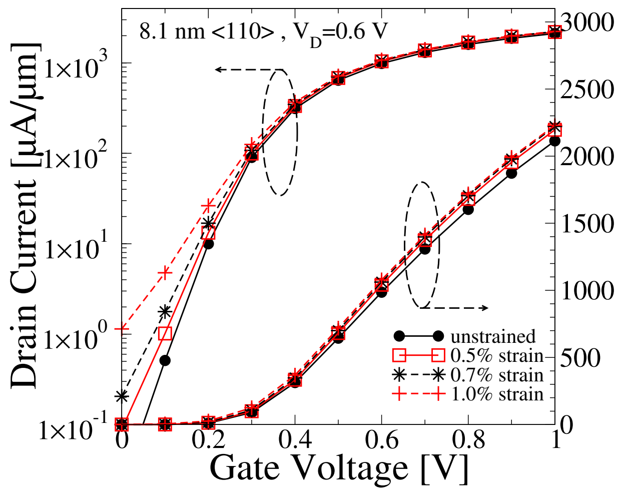


Fig. 7. $I_D$-$V_G$ characteristics at $V_D$=0.6 V in the ⟨110⟩ channel orientation under uniaxial ⟨110⟩ strain with different strengths (8.1 nm gate device).

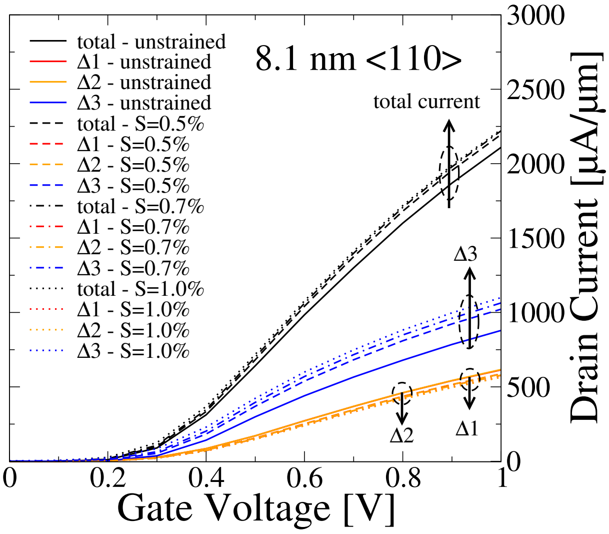


Fig. 8. Valley contributions to the current at $V_D$=0.6 V in the ⟨110⟩ channel orientation under uniaxial ⟨110⟩ strain with different strengths (8.1 nm gate device).

is shifted up reducing its contribution to the drain current because it has the largest effective transport mass ($m_l$) (see Table II). Δ2 and Δ3 bands are shifted down increasing their contributions to the drain current since they have a smaller effective transport mass ($m_t$). However, Δ3 valley contributes more to the current with increasing strain since the valley lays in the less confined direction ($z$-axis). On the other hand, Δ2 valley contributes less to the current because the confinement is much larger in the $y$-direction reducing the effectiveness of strain. To see the effect of confinement over strain, we simulate a FinFET with a gate length of 25 nm (Fig. 6) with a much less confined channel (a width of 12 nm and a height of 30 nm with rounded corners [8]). The 0.5% uniaxial ⟨100⟩ strain increases the drive current (at $V_G$=1.0 V) in the 25 nm gate length SOI FinFET by 21% compared to only 7% for the 8.1 nm gate length device. In addition, Figs. 5 and 6 compare the effect of confinement on the contribution of each valley.

Fig. 7 shows $I_D$-$V_G$ characteristics for the 8.1 nm gate SOI FinFET with a ⟨110⟩ channel orientation at $V_D$=0.6 V under uniaxial ⟨110⟩ strain with strengths of 0.5%, 0.7% and 1.0%. In the ⟨110⟩ orientation, a transformation of coordinates is performed since the ellipsoid principal axes are not aligned with the device coordinate system [9], [17]. Without applying any strain, the ⟨100⟩ channel device delivers more current (20%) than the ⟨110⟩ channel device due to enhanced mobility (lighter effective transport mass). When applying uniaxial ⟨110⟩ strain, the on-current (at $V_G$=1.0 V) is increasing by 3.9%, 5%, and 5.4% at 0.5%, 0.7% and 1.0% strengths, respectively. Fig. 8 shows the 3 Δ valleys contributions to the current under uniaxial ⟨110⟩ strain with different strengths. Under the uniaxial ⟨110⟩ strain, the three conduction bands of Δ valleys are shifted down to increase their contribution to the drain current, especially the Δ3 valley since it has the smallest effective transport mass ($m_t$) (Table 2). Δ3 thus

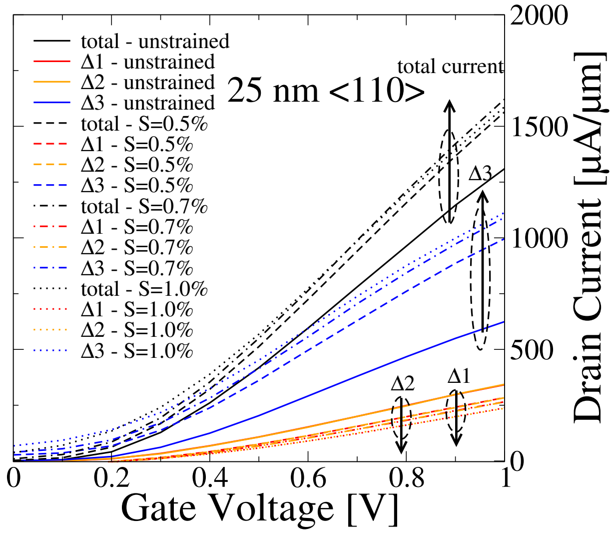


Fig. 9. Valley contributions to the current at $V_D$=1.0 V in the $\langle 110 \rangle$ channel orientation under uniaxial $\langle 110 \rangle$ strain with different strengths (25 nm gate device).

contributes more to the current while $\Delta 1$ and $\Delta 2$ contribute less. Fig. 9 shows comparison for the less quantum confined 25 nm gate length device to clearly demonstrate the effect of minimising the quantum confinement. The $0.5\%$ uniaxial $\langle 110 \rangle$ strain increases the drive current (at $V_G$=1.0 V) by $19\%$ compared to only $3.9\%$ in the $8.1$ nm gate device.

## IV. Conclusion

In conclusion, applying the uniaxial $\langle 100 \rangle$ strain in nanoscale multi-gate transistors with sub-10nm gate lengths increases the on-current much more than the uniaxial $\langle 110 \rangle$ strain. Moreover, with increasing the strain strength the quantum confinement induced pre-existing valley splitting starts to weaken the strain effect especially in the $\langle 110 \rangle$ channel. In the $\langle 100 \rangle$ channel device, the uniaxial $\langle 100 \rangle$ strain increases the on-current with a noticeable difference (by $7\%$, $8.5\%$ and $10.3\%$ for strain strength of $0.5\%$, $0.7\%$ and $1.0\%$, respectively).The on-current in the $\langle 110 \rangle$ channel orientation device is not affected by the strain engineering as much as in the $\langle 100 \rangle$ channel (only $3.9\%$, $5\%$, and $5.4\%$ for $0.5\%$, $0.7\%$ and $1.0\%$ strain, respectively). This is because the principal valleys in the $\langle 110 \rangle$ channel do not lay along the transport direction so that the contribution of the lighter electron effective mass into transport is limited.

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