

Verilog-A Compact Model for a Novel Cu/SiO₂/W Quantum Memristor

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Abstract—In this paper, we develop a Verilog-A model for a memristive device that has shown non-volatile state transitions via half-integer quantized conductance states at room temperature and an on-off ratio of $\sim 10^3$. The model captures the geometrical evolution of a nano-filament and maps it to conductance levels in the equivalent electrical circuit, thereby accurately capturing the DC I-V and transient response of the device. The suitability of the model for circuit simulations is illustrated via a 4×4 crossbar array programming simulation in HSPICE which captures the multilevel programmability of the device.

I. INTRODUCTION

We recently demonstrated a novel Cu/SiO₂/W memristor device exhibiting half-integer quantum conductance states at room temperature operating below 300 mV [1]. In this work, we present a Verilog-A model that accurately captures the switching behavior of this device. Such memristive devices could have several logic and memory applications due to its non-volatility, simple structure and operation characteristics. Its history dependent conductance transitions may be used for synaptic devices in neuromorphic computing systems where high fanout, integration density, and back-end-of-line processing is vital [2], [3]. Its probabilistic switching behavior may be used in realizing stochastic computing systems, as they can efficiently implement multi-cycle multiplication operations using a single cycle AND operation [4], [5]. It may also be used as memory elements, especially in IoT devices, though several reliability challenges need to be addressed to make this a viable alternative to conventional technologies [6], [7].

We recently proposed a simple physics-based model to explain the basic switching characteristics of this device [8]. The device consists of an active top electrode and an inert bottom electrode and shows bipolar resistive switching via the formation of nano-filamentary paths between the electrodes. Building upon that model, here we develop a Verilog-A model for circuit simulations, capturing the observed experimental programming characteristics including its switching response and conductance quantization.

II. DEVICE PHYSICS AND OPERATION

The model we developed is based on the data from a cross-point device consisting of a 10 nm sputter deposited amorphous SiO₂ sandwiched between Cu and W electrodes of 100 μm feature size (Fig. 1). Device dielectric is patterned along with the top electrode and underwent a final 400°C, 5 min annealing process. The annealing was performed to improve the Cu/SiO₂ interface and it also resulted in an

increase in off-state conductance. We used 100 μA current compliance and 1 V voltage compliance during voltage and current sweep measurements respectively to constrain the device to soft breakdown regime. We experimentally observed bipolar pinched hysteresis I-V characteristics below ± 300 mV (Fig. 2), and staircase conductance transitions in current sweep measurements (Fig. 3) at room temperature. The corresponding DC conductance measurement ($I(t)/V(t)$) clearly illustrate the half-integer conductance quantization $G = (n/2)(2e^2/h)$ where $n = 1, 2, \dots$ in our devices.

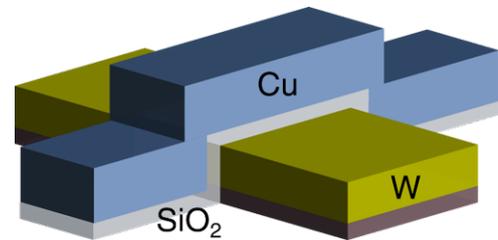


Fig. 1. Fabricated Cu/SiO₂/W crosspoint device with a 10 nm thick sputter deposited SiO₂ dielectric that we reported in [1]. This figure is adapted from the same paper.

The basic device operation can be explained by the physics of electron flow in a nanoscale conducting channel. Typically, electrons undergo frequent scattering and will exhibit diffusive transport when the channel dimensions are large compared to the mean free path and Fermi-wavelength. However, when the channel length becomes comparable to mean free path, the electrons rarely undergo collisions and obey ballistic transport. In addition, if the channel width becomes comparable to Fermi-wavelength, the number of transport modes available becomes limited and theoretically, the device conductance becomes quantized in units of integer multiples of $2e^2/h$. However, half integer quantization has also been observed when a finite voltage is applied across the nano-filament during conductance measurements, which can be attributed to a difference in the number of sub-bands available at the contact Fermi-levels [9], [10]. Therefore, the observation of quantized conductance in our device is a signature of the presence of nano-filamentary channels in the low resistance state.

In our model, we have assumed a single dominant nano-filament to represent the low resistance state of the device for the sake of simplicity. Even if multiple filaments are present, their aggregate effect could be modeled by a single filament with appropriately scaled diameter, and the growth/decay dynamics of each filament may be determined based on the local electric field.

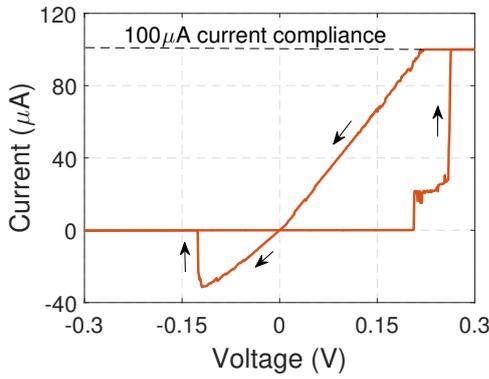


Fig. 2. Quantized memory switching with pinched hysteresis below ± 300 mV experimentally observed in the device, adapted from [1].

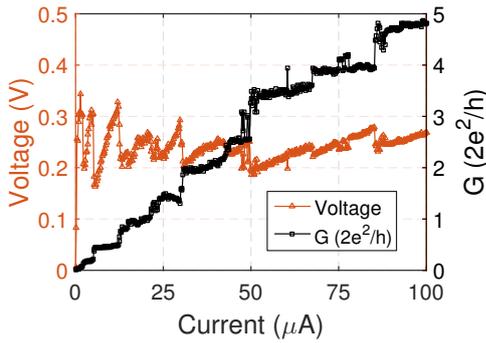


Fig. 3. In current sweep, quantum switching behavior of the device is clearly visible, adapted from [1]. Note that the maximum voltage drop across the device stays relatively constant.

III. COMPACT MODEL

The Verilog-A model of the device includes a series combination of two resistors and a voltage controlled current source (Fig. 4). The resistors model the assumed filament structure and the dependent current source represent the bulk conduction. The physical notion behind the resistive switching is an electric field driven redox process, where the top active-electrode species get oxidized, migrates through the device dielectric, and get reduced at the inert bottom electrode to form a growing filament structure. When this filament bridges the top and bottom electrodes the device conductance switches from high resistance to low resistance state.

We denote the device cross-point area by A_d and dielectric thickness by L . We assume a truncated conical structure (Fig. 5) of height h , tip radius r_t , and base radius r_b for the conductive filament and is represented in the compact model by two resistors in series: the filament resistance, $R_f (= \rho_f h / A_f)$, and the filament gap resistance, $R_g (= \rho_g (L - h) / (\pi r_t^2))$, where ρ_f and ρ_g are the resistivity of the two regions and $A_f (= \pi r_t r_b)$ is the effective filament area. The resistance values, determined by the parameters such as L, h, A_f , evolve as a function of the electric field acting on the filament surface and the rate of evolution is determined by the Mott-Gurney ionic hopping velocity [11]. The filament dynamics are modeled by three growth rates - vertical height evolution (dh/dt), radius evolution at the filament tip (dr_t/dt), and radius evolution at the base (dr_b/dt).

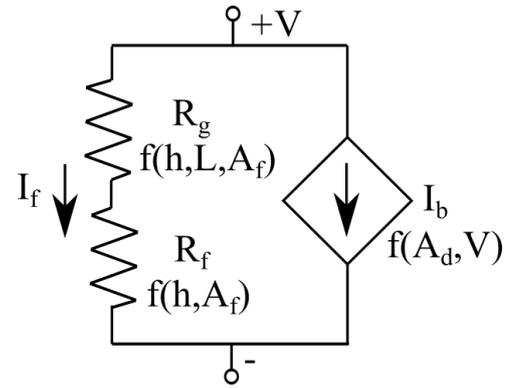


Fig. 4. The circuit equivalent of the Verilog-A model of the memristor. The series resistors represent the filament path and the voltage controlled current source model the background bulk conduction.

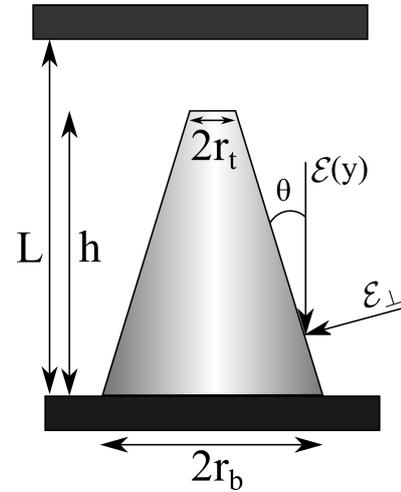


Fig. 5. The assumed truncated conical structure representing the nanofilament model. The effective electric field acting normal to the cone surface which drives the lateral evolution of the filament is shown.

Assuming that the ionic migration through the dielectric is the slowest and the limiting factor in the filament growth process, the vertical evolution is assumed to be proportional to the ionic hopping current [12], with v_h (m/s) as a fitting parameter:

$$\frac{dh}{dt} = v_h \exp\left(-\frac{E_a}{k_B T}\right) \sinh\left(\frac{Zea\mathcal{E}_g}{2k_B T}\right) \quad (1)$$

where E_a is the diffusion barrier for the ionic migration, Z is the charge number of the ion, e is the charge of an electron, a is the effective ionic hopping distance, T is the temperature, and k_B is the Boltzmann constant. The electric field \mathcal{E}_g in the filament gap is proportional to the voltage across the filament gap resistance, R_g . Since R_g is much greater than R_f because of high dielectric resistivity, the electric field will be concentrated in the filament gap till the filament touches the top electrode. This period is characterized by a rapid vertical evolution of the filament with negligible lateral growth. Further, the filament radial evolution rate is also assumed to be determined by the Mott-Gurney ionic hopping current. This ionic current is proportional to the field acting normal to the filament surface (see \mathcal{E}_\perp in Fig. 5). The voltage along the filament can be determined by integrating the distributed

conductance. The electric field \mathcal{E} at height y is

$$\mathcal{E}(y) = -\frac{dV}{dy} = \frac{d}{dy} I \int_0^y \frac{\rho_f}{A_f(h)} dh = \frac{I\rho_f}{A_f(y)} \quad (2)$$

where $A_f(y)$ is the filament area at y and $\mathcal{E}_\perp = \mathcal{E}(y) \sin \theta$. From equation 2, we can see that the electric field is inversely proportional to the filament radius and hence the tip will grow faster compared to the filament base, and the conical structure will evolve to a cylinder. This will cause the surface electric field to vanish asymptotically and further filament growth, which is relatively small, is modeled using the average electric field across the device as

if $r_t < r_b$

$$\frac{dr_{(t,b)}}{dt} = \alpha_{(t,b)} v_r \cos \theta \exp\left(-\frac{E_{ar}}{kT}\right) \sinh\left(\beta_{(t,b)} \frac{Zea\mathcal{E}_\perp}{2k_B T}\right) \quad (3)$$

else

$$\frac{dr_{(t,b)}}{dt} = v_r \exp\left(-\frac{E_{ar}}{kT}\right) \sinh\left(B \frac{eV_{eff}}{kT}\right) \quad (4)$$

where the $\alpha_{(t,b)}$, $\beta_{(t,b)}$, B , and v_r are fitting parameters and subscripts t and b denote tip and base of the filament. The $\cos \theta$ term is used to determine the growth rate in the horizontal direction. By solving the differential equations 1 through 4, we obtain the filament structure as a function of time, which is then mapped to corresponding electrical parameters.

It has been observed that during conductance quantization the average voltage across the device remains relatively constant [1]. If we neglect the voltage drop across the bulk contacts, this voltage corresponds to the drop across the filament and it will represent the contact Fermi-level split. It is suggested that this Fermi level split can be used as an estimation for the sub-band spacing [9]. Therefore the statistically constant voltage drop across the filament suggests that the theoretical increase in the sub-band spacing is compensated by the growing filament radius. We used this idea to estimate the filament radius using the theoretical relation between sub-band spacing and radius for a nano-filament. A least square fit over this estimation is used to relate $r_{(t,b)}$ to R_f in the low resistance state ($R_g = 0$) as shown in Fig. 6. Thus, $R_f = (n/2)(2e^2/h)$ when $h = L$ and is modeled as an ohmic resistor otherwise. The filament gap, lightly doped with the metal ions migrating to the cathode, is also modeled as an ohmic resistor.

The HRS resistance of the device was invariant during forming and normal operation; the device conductance in the HRS is hence assumed to be dominated by the device background conduction rather than that of the broken filament area. This bulk conduction data from the device is fitted with an electron hopping current model and is represented in the Verilog-A model as a voltage controlled current source using the following equation:

$$I_{HRS} = (A_d - A_f) J_0 \sinh\left(\frac{a_{eh} eV}{k_B T L}\right) \quad (5)$$

where a_{eh} is the average electron hopping distance.

This two terminal model is tested in HSPICE using a standard dual sweep I-V measurement of amplitude 500 mV

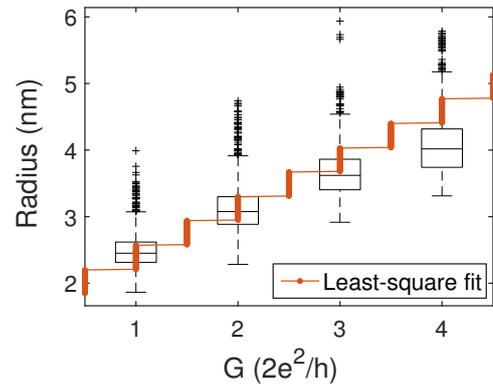


Fig. 6. Filament radius estimation from the device data [1] and the corresponding least square fit (with a floor function) which maps the filament geometry to a conductance state in our model, adapted from [8].

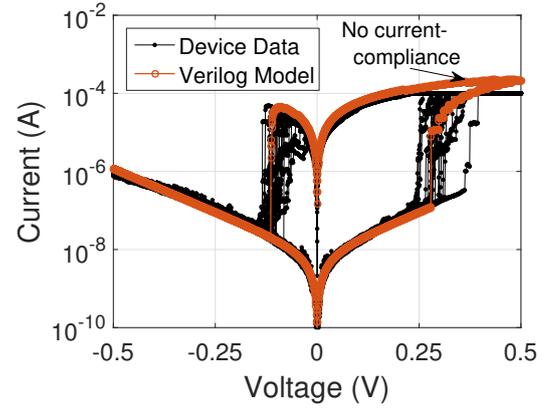


Fig. 7. The voltage sweep response of the device and the corresponding Verilog-A simulation in Hspice is shown for comparison. We can see that the model response shows excellent statistical agreement with the data.

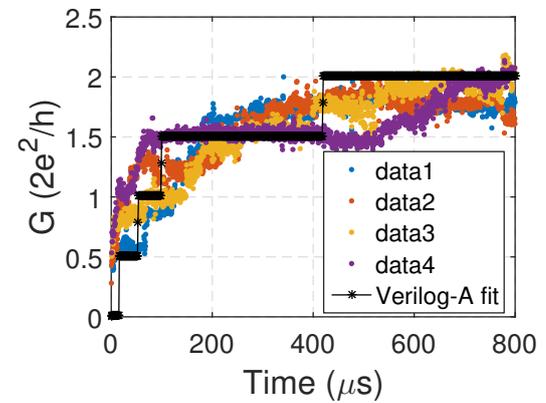


Fig. 8. The Verilog-A model also captures the trends in transient switching characteristics of the device. Response of the device and model to 200 mV pulse is shown.

(Fig. 7) and pulse of amplitude 200 mV (Fig. 8); excellent agreement is obtained with measured device data. The device model simulation used no current compliance compared to the device measurement and hence we can see an overshoot in current in Fig. 7. The resistance transition is comparatively slow once the device is in quantized conductance state and we have kept the voltage range low to avoid irreversible device

breakdown. In the model, we assume an initial filament seed of height 0.5 nm, base radius 2.7 nm, and tip radius 1.5 nm. We match model response with the pulse response data from a different process wafer assuming a slightly lower dielectric thickness (7 nm). The parameter list used in the Verilog-A model is given in Table I.

IV. CIRCUIT SIMULATIONS

To illustrate the use of our Verilog-A model in circuit simulations for machine learning applications [2], we simulated programming of a 4×4 cross-bar array of quantum memristors by the overlap of voltage waveforms applied to the periphery (Fig. 9). We used 80 μs long programming pulses on the word lines that appear at randomly staggered delay compared to the bit line signal. The pulse amplitudes were 0.2 V and -0.1 V for the word and bit lines. For example, Fig. 10 shows a particular case in which a voltage waveform V_{b3} is applied to the bit line 3 with all the other bit lines grounded. The V_{wi} shows the corresponding voltages on the word lines. Depending on the overlap duration and the resultant voltage waveform at the device, higher conductance values are reached (g_{wb} lines in Fig. 10), accurately capturing the expected programming trend. This is similar to Hebbian learning where the connecting weight change is proportional to end point signal correlation.

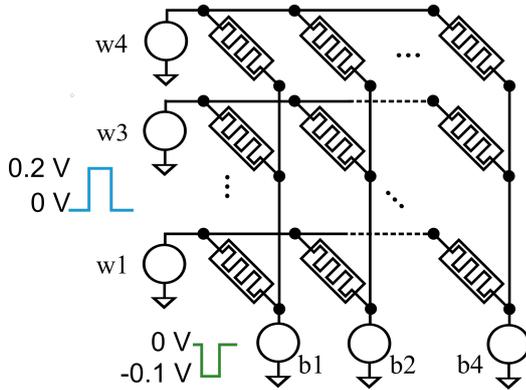


Fig. 9. Parallel programming scheme to illustrate circuit simulation for the cross-bar array of devices. The 4×4 cross bar structure and programming waveforms are shown.

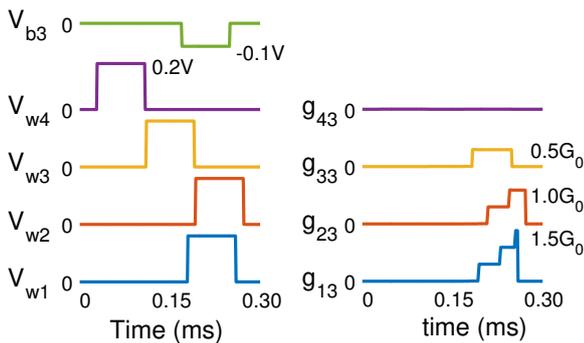


Fig. 10. HSPICE simulations: The applied voltage waveforms (V_{wi} and V_{b3} lines) and the simulated conductance trace (g_{wb} lines).

V. CONCLUSION

We have developed a Verilog-A model that accurately captures the essential aspects of experimentally observed memory

Symbol	Value	Symbol	Value
v_h	1 m/s	ρ_f	$30 \mu\Omega\text{m}$
v_r	85 m/s	ρ_g	$3 \text{M}\Omega\text{m}$
a	20 nm	a_{eh}	2.66 nm
E_a	0.55 eV	E_{ar}	0.41 eV
J_0	1.36A/m^2	A_d	$10^4 \mu\text{m}^2$
α_t	1	β_t	0.6
α_b	0.56	β_b	1

TABLE I. PARAMETERS USED IN THE VERILOG-A MODEL, ADAPTED AND REFINED FROM [8].

switching in the quantum memristor device. The equivalent circuit element parameters were determined by the growth dynamics and structure of a nano-filament. Ionic migration velocity decides the filament evolution rate and data-fitted curves were used to convert it into conductance levels. The model can be used in circuit simulations for testing the architectural feasibility of memory and neuromorphic synaptic crossbar array structures.

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