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Advanced Physical Modeling of SiO*x* Resistive Random Access Memories

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***Abstract*— We apply a three-dimensional (3D) physical simulator, coupling self-consistently stochastic kinetic Monte Carlo descriptions of ion and electron transport, to investigate switching in silicon-rich silica (SiO_x) redox-based resistive random-access memory (RRAM) devices. We explain the intrinsic nature of resistance switching of the SiO_x layer, and demonstrate the impact of self-heating effects and the initial vacancy distributions on switching. We also highlight the necessity of using 3D physical modelling to predict correctly the switching behavior. The simulation framework is useful for exploring the little-known physics of SiO_x RRAMs and RRAM devices in general. This proves useful in achieving efficient device and circuit designs, in terms of performance, variability and reliability.**

Keywords*— *Si-rich silica (SiO_x) resistive random-access memory (RRAM); Multi-scale modelling; Charge transport; Self-heating;

I. Introduction

Resistive random-access memory (RRAM) devices, often considered as a next generation of nonvolatile memory devices, have recently attracted significant attention [1]-[6]. This class of devices offers low cost-per-bit, low power dissipation, and high endurance, and are well-suited for integration in crossbar arrays in 3D chips, as indicated by the International Technology Roadmap for Semiconductors (ITRS) report of 2010 on emerging research devices [1]. Applications of RRAM technology include high-density memories, novel processor architectures, neuromorphic computing and neural networks. Silica RRAM technology provides a further advantage, as it could be more easily integrated with Si CMOS chips [2]-[4].

Most work on RRAMs focuses on transition metal oxide (e.g. TiO_x or HfO_x) devices. While metal oxide RRAMs are currently considered most promising, they face a serious challenge related to Si on-chip integration. Furthermore, previous modeling work has relied heavily on classical and phenomenological methods based e.g. on the resistor breaker network and 2D models [5]. These models do not calculate self-consistently the electric fields and do not consider accurately the heat generation and diffusion phenomena.

II. Simulation Method

Our kinetic Monte Carlo (KMC) based transport simulator employs a microscopic description of electron transport, and a first-principle understanding of vacancy generation, recombination and dynamics. We demonstrate intrinsic switching in Silicon-rich Silica (SiO_x) RRAMs, explore the effect of initial vacancy distributions and self-heating on device characteristics, and highlight the necessity of 3D modelling in this class of devices. The simulator employs a powerful combination of tools, to correctly study the conductive filament (CF) formation and destruction in 3D, by coupling self-consistently oxygen ion and electron transport simulations to the local electric field and temperature distributions determined from physical and atomistic models.

The simulation framework is shown in Fig. 1. In the 3D space, we coupled KMC simulations of ion and electron transport to the atomistic simulator GARAND [7] and a time-dependent heat diffusion equation (HDE) solver. In solving the HDE, we consider Joule heating from ionic movements and electron transitions from trapping processes in the oxide. To simulate electron transport in the oxide, we include trap-to-trap tunneling, electrode-trap tunneling, Schottky emission, Fowler-Nordheim tunneling, emission from traps to the conduction band (CB), tunneling from traps to the CB, and direct tunneling, as illustrated in Fig. 2. We update the occupancies using a KMC simulator instead of the previously used solver [6]. Oxygen ion diffusion, and ion-vacancy generation and recombination events are also modelled via the KMC formalism. For silica, the activation energy governing defect generation can be related to the strength of a Si-O bond which is ~4eV. However, using this value leads to the conclusion that vacancy generation may only occur at very high fields. We performed density functional theory (DFT) simulations to study the defect generation process and showed that electrons can be trapped in the pristine amorphous matrix at wide O-Si-O angles [8]. When electrons localize onto these intrinsic sites, local deformations weaken nearby Si-O bonds and lower the barrier for generation to ~1eV, as shown in Fig. 3.

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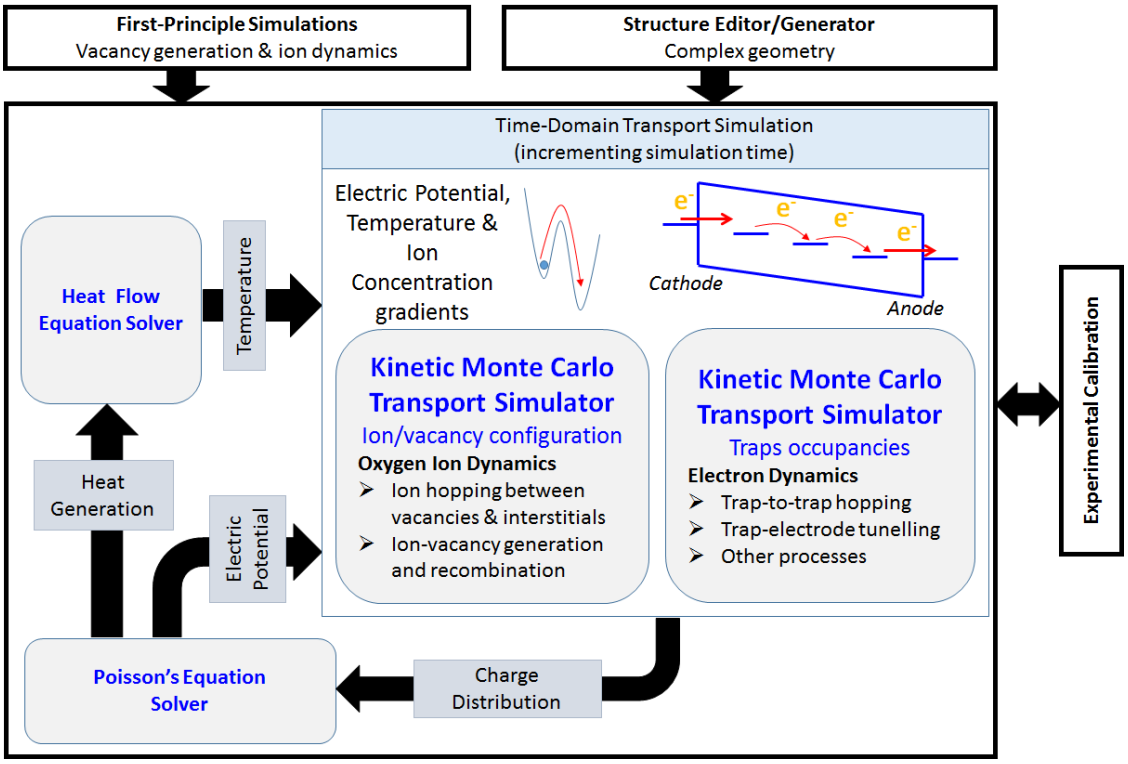

Fig. 1. The simulator, coupling self-consistently ion and electron transport to the electric field and temperature distributions.

Two important aspects of the simulator need to be highlighted: (i) using a fundamental understanding of vacancy generation to extract important parameters such as activation energies and diffusion barriers (not used in our previous work [9],[10]), and (ii) integrating an advanced structure generator into the simulation framework, which allows the generation of a simulation structure of any arbitrary geometry and material profile. The structure editor is particularly useful when studying realistic SiO_x RRAM structures incorporating silicon-rich areas (defect rich areas or areas with Si nano-inclusions [2]) in the oxide, as is the case here. Also, we employ a more advanced HDE solver, as compared to time-independent HDE solvers employed for instance in [11], [12].

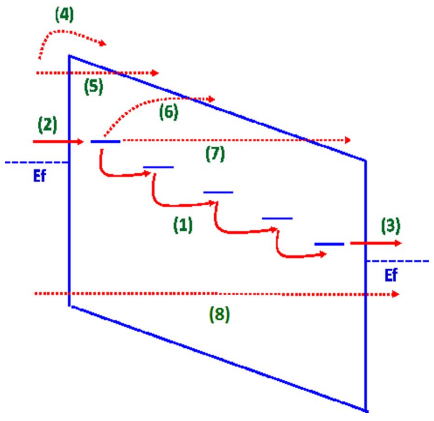

Fig. 2. Electron transport mechanisms in the oxide: (1) trap-to-trap tunneling, (2) and (3) electrode-trap tunneling, (4) Schottky emission, (5) Fowler-Nordheim tunneling, (6) emission from traps to the conduction band (CB), (7) tunneling from trap to the CB, and (8) direct tunneling.

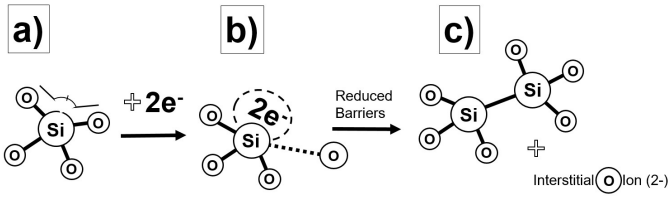

Fig. 3. Trapped electrons lower the barrier for defect generation at nearby sites to ~1eV.

III. Results, Discussion and Conclusions

The full experimental structure typically consists of a thin (around 10nm-40nm) layer of SiO*x* between two TiN electrodes. Fig. 4 shows the electron transport simulation domain. While the electrodes in the experimental setting have a typical area of 100µm×100µm [2], it is only necessary to study a smaller area (e.g. 20nm×20nm), corresponding for example to a grain boundary region, as illustrated in Fig. 4. Switching in silicon-rich silica RRAMs has been demonstrated experimentally by some of the authors [2]-[4], [13], reporting devices that can be cycled between high resistance OFF and low resistance ON states with a resistance contrast of at least 10,000, for a relatively long period.

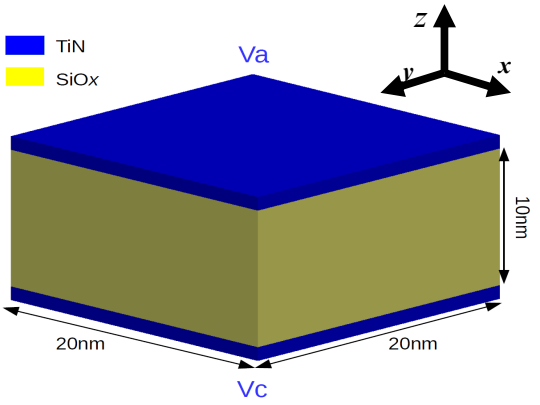

Fig. 4. The simulation domain, including a cross section of the TiN/SiO*x*/TiN structure.

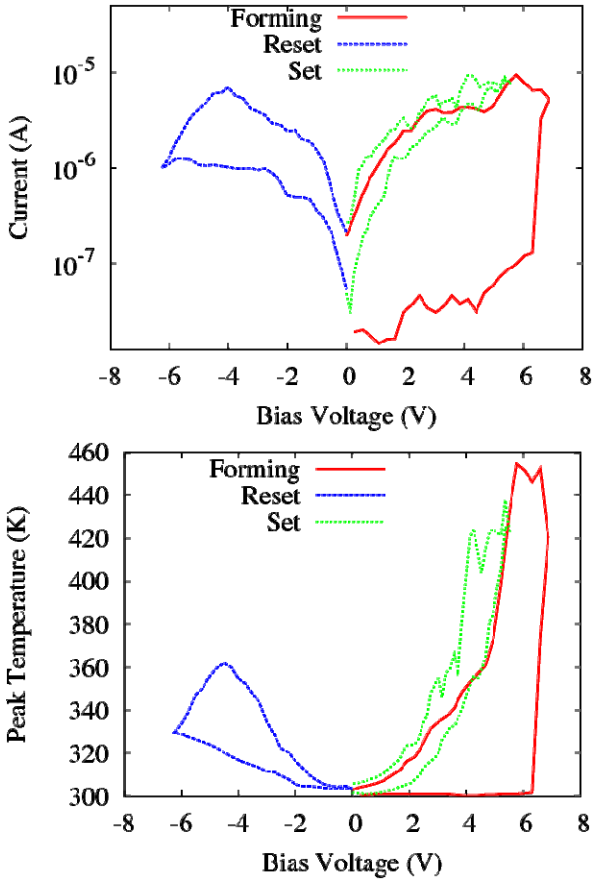

Fig. 5. (top) *I–V* characteristics, showing the forming, set and reset processes, for an arbitrary initial vacancy distribution. We impose a current compliance limit of ~ 10^{-5} A. (bottom) The corresponding variation of the peak temperature.

Fig. 5 shows the *I–V* characteristics and the variation of the peak temperature for an arbitrary initial vacancy distribution. In this example, we impose a current compliance limit of ~ 10^{-5} A. Fig. 5 shows how our simulator reconstructs realistically the measured *I–V* characteristics [2], including the forming, set and reset processes, for a given initial vacancy distribution. Fig. 5 also shows the peak temperatures accompanying the *I–V* characteristics. Clearly, self-heating plays an important role, especially during forming and in the on-state. Fig. 6 shows spatial temperature distribution maps in the oxide, demonstrating heat diffusion during switching, as the CF is constructed during the forming process, destructed during the reset process, and reconstructed during the set process. From Figs. 5 and 6, it can be seen that temperatures can reach peak values as high as 460K during forming and the on-state, despite the relatively low electric currents through the oxide (and hence the reduced power consumption). This behavior is attributed to two main reasons: 1) the very high current densities through the created percolation paths and 2) the poor thermal management in oxides (which have a very low thermal conductivity), both leading to the observed high operating temperatures.

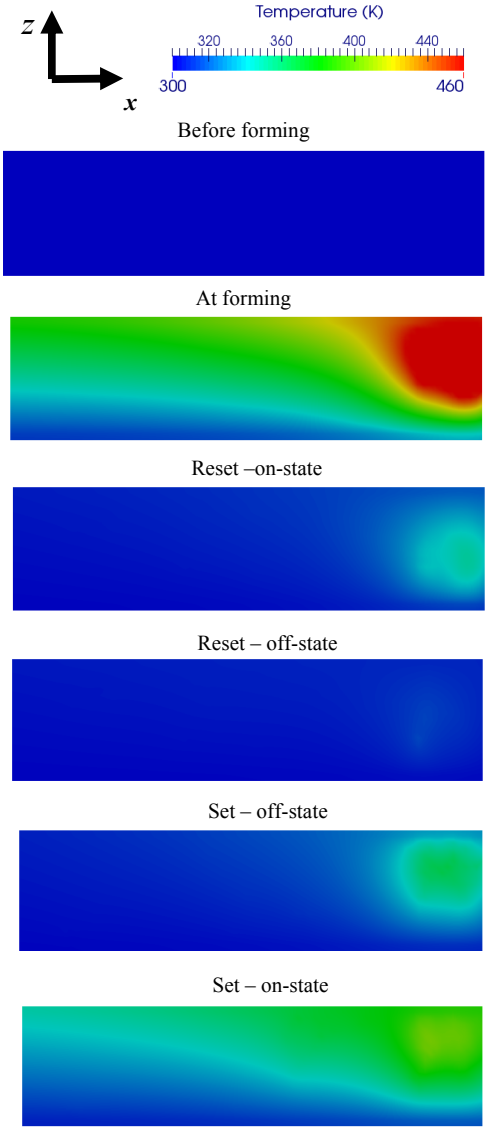

Fig. 6 Temperature map snapshots in the oxide layer, taken to show heat diffusion during the switching processes. The results are for a 40nmx40nmx10nm structure.

Figs. 7 and 8 illustrate the process of conductive filament creation by showing the vacancy distributions, as bias is increased, in two different structures: (i) a SiO_2 'pristine' structure with a low initial vacancy concentration and (ii) a SiO_x structure with a Si-rich (high initial concentration) column, respectively. For the SiO_2 structure, almost no vacancies are generated at low biases (e.g. 5V). As bias is increased (e.g. 10V), more vacancies are generated and filament seeds start to appear. These seeds grow as bias is increased (e.g. 11V). At ~12V, an accelerated generation of oxygen vacancies occurs and forms a complete conductive filament, bridging the two electrodes. The same process occurs for the Si-rich structure, but in this case the filament creation occurs at lower biases. As opposed to pristine (SiO_2) structures, switching is possible in defect-rich structures at low forming biases, without reaching hard-breakdown which is undesirable as it may cause irreversible switching. Figs. 7 and 8 illustrate the 3D nature of conductive filaments, which highlight the necessity of using 3D simulators to predict correctly switching and device characteristics.

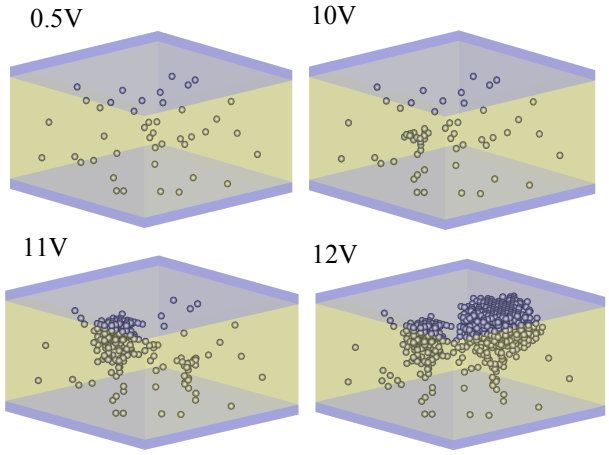

Fig. 7: Vacancy distributions for the (SiO_2) structure with relatively low initial vacancy concentrations, as the bias voltage is increased up to the CF forming. For this structure, the CF may only be formed at high fields, increasing the possibility of hard breakdown and hence irreversible ON/OFF state transitions.

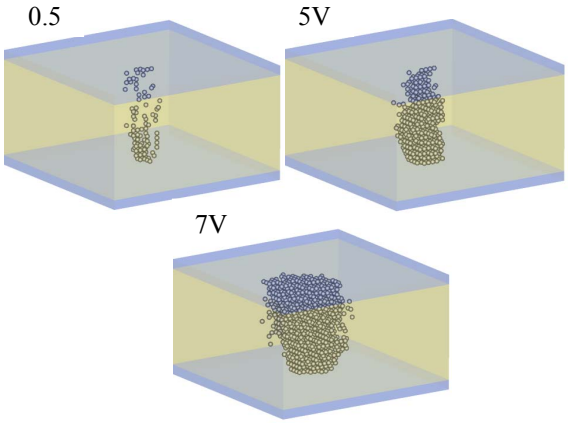

Fig. 8: Vacancy distributions as the bias voltage is increased. The device includes a column with a relatively high initial vacancy concentration.

IV. Conclusions

We employ a self-consistent 3D electrothermal kinetic Monte Carlo simulator, combining first-principal calculations and microscopic simulation methods, to explore resistance switching in silicon-rich silica RRAM devices. The results support the hypothesis that switching is an intrinsic property of the SiO_x layer, as a result of the forming and destruction of conductive filaments in the highly sub-stoichiometric oxide. We demonstrate the impact of self-heating effects, the role of the initial vacancy distributions, and also the necessity of 3D physical modelling to predict correctly the switching phenomenon in RRAM structures. The simulator provides insight into device physics, and is useful for facilitating efficient designs in terms of performance, variability and reliability in RRAM devices and circuits.

Acknowledgment

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