

Atomistic Simulation Flow for Source-Drain Epitaxy and Contact Formation Processes of Advanced Logic Devices

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Abstract— An atomistic simulation flow for contact formation process was developed and integrated into logic transistor front-end process simulation. Existing atomistic kinetic lattice Monte Carlo model of epitaxy process was extended to silicidation. Metal and silicon diffusion and silicide formation reactions were taken into account at atomic level which allowed accurate simulation of silicide shape including faceting effects. This approach enables device performance prediction depending on design rules and parameters thus providing a way for TCAD-based technology optimization. As an implementation example a contact resistance prediction depending on contact opening and recess depth for a 10-nm class logic device is demonstrated.

Keywords—kinetic Monte Carlo; epitaxy; multi-scale simulation; atomistic; silicidation; contact resistance.

I. INTRODUCTION

Reduction of contact resistance is an important performance knob for modern logic transistors, but for sub-10 nm devices the conventional continuum simulation of silicidation [1] loses its accuracy due to silicide faceting and anisotropy driven by atomic-scale interactions. In order to secure simulation predictability for FinFETs and other emerging transistor architectures a simulation flow has to be developed that would include atomistic effects during source/drain (S/D) formation, contact implantation and silicide formation processes. Even though simulation of S/D formation can be performed using a kinetic Monte Carlo (KMC) method that was used for decades to simulate epitaxy [2-4], and solid phase epitaxial regrowth (SPER) [5], so far no attempts to incorporate silicidation in a similar framework were reported. Therefore the present work focuses on the development of an atomistic multi-scale simulation flow for silicidation process to explain trends in Fin-type logic device contact resistance depending on process conditions (such as contact implantation dose and energy and silicidation temperature and time) and transistor structure parameters.

To provide useful results for process technology optimization, the flow has to be incorporated in a full transistor simulation setup, including both front-end process and device electrical parameters extraction. It adds complexity to the task

because a robust and efficient atomistic-to-continuum data transfer methodology has to be developed.

II. ATOMISTIC SILICIDATION SIMULATION MODEL

Silicidation process strongly depends on the shape of transistor source and drain (S/D) which is formed by epitaxial process and thus predictive simulation of silicidation must include simulation of epitaxy. This is why previously developed kinetic lattice Monte Carlo (KLMC) model of epitaxy [6] was used as the backbone of atomistic silicidation simulation flow.

A. KLMC Simulation of Epitaxy

The model was originally developed for S/D shape prediction and it can consider growth of Si/SiGe structures. The model considers adsorption, desorption, and diffusion of atoms on a virtual lattice (ideal diamond-type lattice). Probabilities of all process follow Arrhenius law and energy barriers for reactions are dependent on local atomic configurations [7]. Model parameters (binding energies and reaction rate pre-factors) were calibrated to predict SiGe growth rates depending on crystal orientation and final S/D structure shape based on TEM.

Typically, silicidation process is accompanied with recrystallization of silicon amorphized by preceding high-dose contact ion implantation step, so a model of SPER process and associated redistribution of dopants has to be an integral part of atomistic silicidation simulation flow. It was implemented in a manner similar to [5] with dopant atoms “pushed” by the passing amorphous/crystalline interface moving towards the surface.

B. KLMC Silicidation Model

Depending on silicide type, silicidation process is driven by diffusion of silicon or metal atoms through silicide to metal and silicon interfaces, respectively [8]. Once diffusing species reach interface they interact with it forming silicide. For the sake of generality developed KLMC silicidation model considers simultaneous diffusion through silicide of silicon atoms to metal interface and metal atoms to silicon interface. It

covers both Ti- and Ni- silicides. In addition to these reactions, during silicidation process dopants may be redistributed via two different mechanisms: so-called snow-plow effect during SPER in silicon and dopant condensation by the growing silicide. Therefore atomistic reactions considered by KLMC model (shown in Fig. 1) are divided in three groups: metal-related (reactions 1-3), silicon-related (reactions 4-6) and dopant-related (reactions I and II).

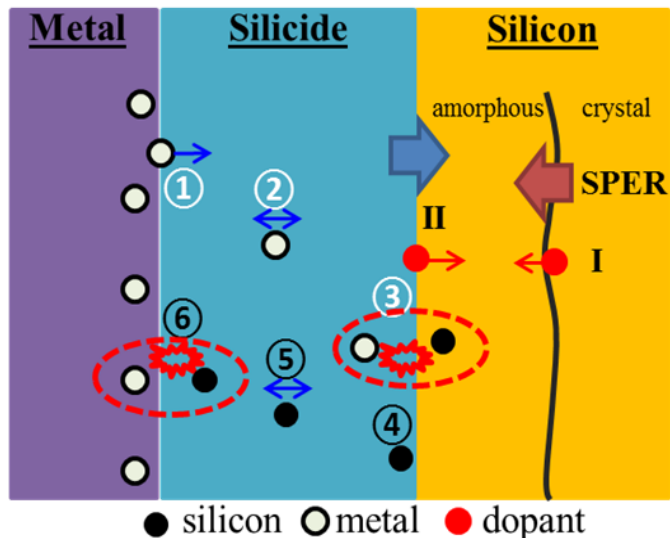


Fig. 1. Schematic of key physical processes of silicide formation and dopant redistribution considered within the developed KLMC silicidation model framework.

- 1) Generation of mobile metal species at metal-silicide interface.
- 2) Diffusion of metal species in silicide.
- 3) Reaction of metal species with silicon and formation of silicide.
- 4) Injection of mobile silicon atoms into silicide from silicon-silicide interface.
- 5) Diffusion of silicon through silicide.
- 6) Formation of silicide at metal side after reaction of silicon with metal.

The model considers two kinds of dopant redistribution processes during silicidation reaction:

- I) Snow-plow effect during SPER: at the moment when recrystallization interface passes dopant position, it can be pushed into the amorphous region with certain probability.
- II) Dopant condensation to silicon from forming silicide: if during silicide formation a dopant atom happens to be at the interface, it can be pushed into the silicon.

Example of atomistic dopant distribution evolution during silicidation is shown in Fig. 2 and concentration profile in Fig. 3. Model parameters were tuned to exaggerate effects for demonstration purposes. For silicidation prediction dopant profiles were calibrated with SIMS experimental data.

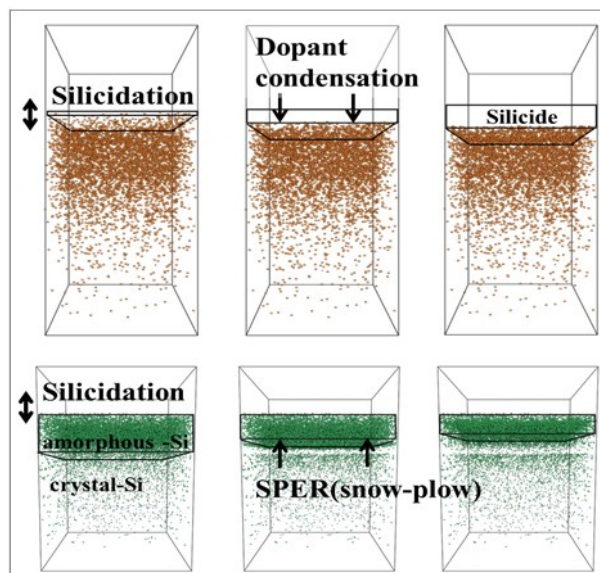


Fig. 2. Dopant redistribution during silicidation: (a) dopant condensation, (b) snow-plow effect.

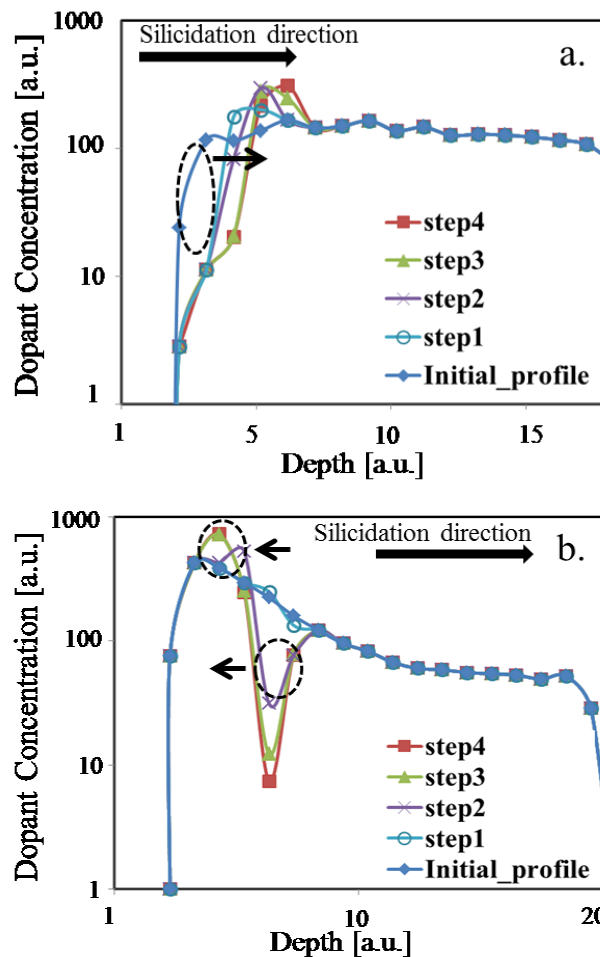


Fig. 3. Evolution of dopant concentration during silicidation process (in consecutive time steps (1-4), only with dopant condensation (a), and only with snow-plow effect (b)).

III. SIMULATION SETUP & CALIBRATION FLOW

A study of available H/W data showed that final silicide shape strongly depends on the shape of the structure right after contact recess and metal deposition. Therefore to improve accuracy of silicidation simulation a topography simulation step has to be incorporated in multi-scale silicidation simulation flow that is summarized in Fig. 4.

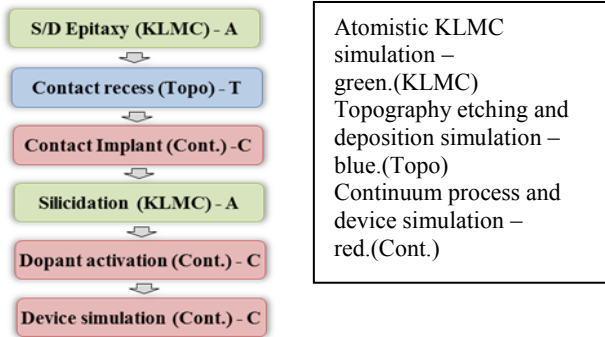


Fig. 4. Multi-scale epitaxy, etching and silicidation simulation flow.

A. Multi-Scale Epitaxy and Silicidation Simulation Flow

To achieve desired accuracy of contact resistance prediction a simulation flow was set up in the following order: firstly KLMC epitaxy simulation was performed to obtain S/D structure, then etching and metal deposition simulation was performed with topography tool (calibrated based on TEM data.), and finally silicidation simulation was performed with KLMC again. This integrated approach allowed simultaneous optimization of contact recess depth, silicide shape and structure parameters.

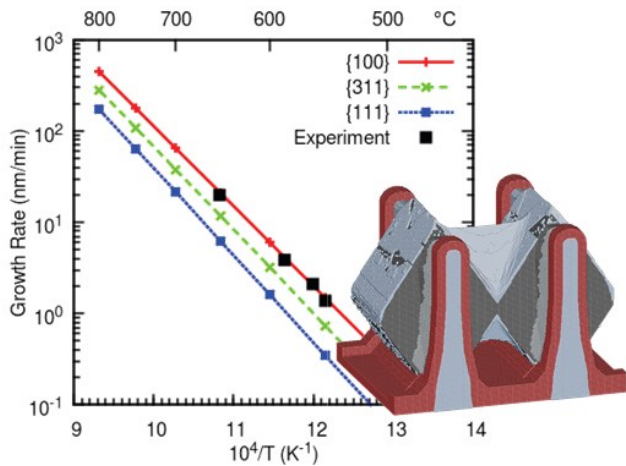


Fig. 5. Simulated growth rates for various Si substrate surface orientations and various temperatures in comparison with experimental data [6]. Inset shows general structure of adjacent S/D structures of two Fin-type transistors (gate structure and spacers are removed for clarity).

B. Calibration Flow

To calibrate KLMC epitaxy model comparison with both 1D experimental data (growth rate depending on temperature

and surface orientation.) and 3D data (TEM images of grown S/D structures of real devices). Basic adsorption/desorption energies and prefactors were calibrated first with growth rate data (Fig. 5). To increase simulated S/D shape accuracy an empirical non-linear binding energy model was used for nearest neighbors and up to third-nearest neighbors interactions were considered. Binding energies were tuned based on final S/D shapes obtained from TEM data.

After that a commercial tool is used to simulate contact recess shape and process simulation tool was used to simulate contact implantation step (using Monte Carlo method.) and extract initial dopant distribution and amorphized region shape.

Finally, metal deposition was simulated by topography tool again and the resulting silicon and metal shapes that were used as an input for atomistic silicidation model. Calibration of topography tool was done with TEM images of as-deposited metal layers before silicidation anneal.

To calibrate silicidation process simulation at first reacting species (Si or metal) were chosen depending on silicide type and then the diffusivity and reaction rates for these species were calibrated based on extensive TEM and SIMS data. Special attention was paid to the facet formation observed in some of silicidation TEM images since it allowed fine-tuning of energy parameters that define silicidation reaction rates depending on local atomistic neighborhood. Fig. 6 shows simulation results for contact structure taken from [9], depending on initial contact recess depth.

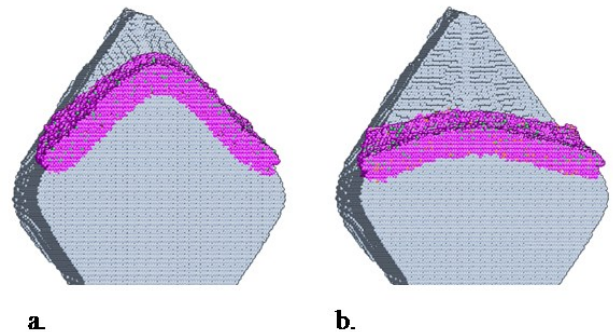


Fig. 6. Silicidation simulation result depending on contact recess depth: (a) shallow recess, (b) deep recess.

IV. CONTACT RESISTANCE SIMULATION

Atomistic simulation allowed us to estimate impact of different contact recess depths on final silicide shape. Once all structures were prepared by KLMC or topography simulation, they were all imported into continuum process simulation tool to simulate dopant diffusion and activation during process steps. After that device simulation was performed to extract contact resistance. It was found that different contact recess depths give completely different contact resistance dependence on gate-to-gate pitch (Fig. 7) due to changes in silicide shape and dopant redistribution during silicidation that affects Schottky barrier height at the contact.

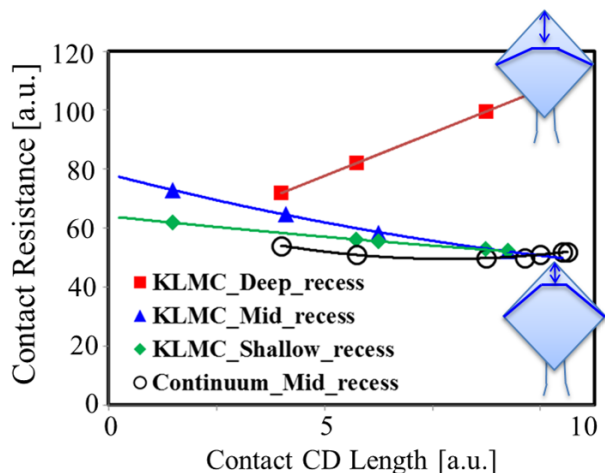


Fig. 7. Contact resistance as a function of recess depth and gate-to-gate pitch. Deep recess leads to the change of trend depending on contact opening, because of the difference in doping distribution below the silicide.

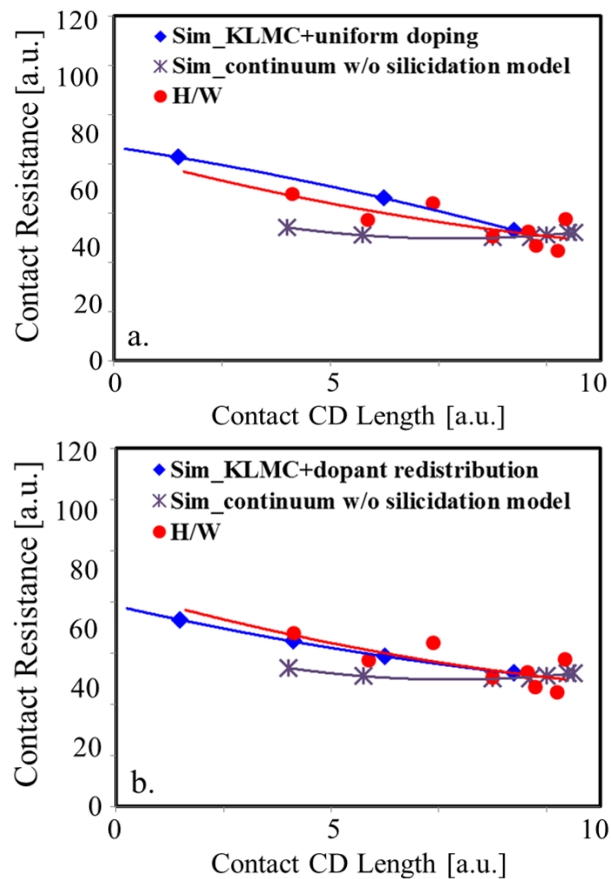


Fig. 8. Contact resistance experimental data and simulation results with constant dopant distribution (a) and considering dopant redistribution during silicidation (b).

Fig. 8a shows that simulation of silicide shape alone is not sufficient to accurately predict contact resistance and that snow-plow and dopant condensation effects have to be an integral part of the silicidation simulation. Once the effects were included, desired accuracy of contact resistance simulation was achieved (Fig. 8b). Remaining discrepancy with H/W data can be explained by existence of thermal dopant diffusion during silicidation that is not considered by the model at the moment.

V. CONCLUSIONS

For the first time a fully integrated multi-scale simulation flow for S/D epitaxy and silicidation processes has been developed. A combination of atomistic KLMC epitaxy and silicidation models with etching and deposition simulation and continuum dopant diffusion/activation simulation allows prediction of contact silicide shape and contact resistance for logic modern sub-10 nm logic transistors.

Additional accuracy improvement is possible by integration of advanced atomistic dopant diffusion model in KLMC framework.

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