Transient 3-D TCAD Simulation of Multiple Snapback Event in Mixed-Mode Test for Mutual Relation between Protection Devices

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***Abstract*—Mutual ESD behavior dependency between multiple devices under Transmission Line Pulse stress was investigated using transient 3-D TCAD simulation. Interestingly, the transient response of drain voltage has multiple snapback profiles in the mixed-mode test. When one of the devices in the mixed-mode test is turned on, the current waveform of the other adjacent devices shows snapback profile. This mutual relation between protection devices affects the ESD robustness. If there is a big imbalance of individual ESD characteristics between the devices under the mixed-mode test, the lattice temperature hot-spot and failure may occurs in the device even though the robustness of the other connected device is lower than that of the device in the single-device test.**

Keywords—multiple-snapback event; mixed-mode simulation, ESD robustness; TLP test

I. INTRODUCTION

Electrical parameters of single device are extracted through the use of nano-scale tungsten wires (nano probing) in the semiconductor industry. The characterization of individual devices such as ESD protection devices is instrumental to engineers and circuit designers during initial product development and failure analysis to aid with yield enhancement, quality and reliability issues [1]. However, extracting device characteristics of each individual protection device in the circuit such as ODT circuit, including several physical devices and lumped elements, through the nano probing is difficult because of the possibility of damage on probe itself.

Over the last few decades, the robust development methodology and optimization of ESD protection devices have been extensively studied and reported [2–7]. However, these studies of the ESD behavior were concentrated on single protection device characteristics; the mutual ESD behavior between several devices has not yet been clarified. In this work, we report on the mutual ESD behavior dependency between multiple devices (NMOS) under Transmission Line Pulse (TLP, 100 ns square pulse) stress and its effect on the ESD robustness. In order to take into account the interrelation between the protection devices, the mixed-mode 3D TCAD simulation approach is employed [2]. Circuit diagrams and device layouts for the single and mixed-mode test are presented in Figs. 1 and 2.

II. SIMULATION MODEL

Fig. 1 shows circuit diagrams for single-device test and mixed-mode test. In the mixed-mode test, DUT A and B are connected to a single PAD, as shown in Fig. 1(b). DUT A represents Tr. 1 (Fig. 2(a)) and DUT B represents Tr. 2 (Fig. 2(b) or Tr. 3 (Fig. 2(c)) for two different combinations (Tr. 1-Tr. 2 and Tr. 1-Tr. 3). Device layout top views of each NMOS device are shown as Fig. 2. Geometrical parameters such as W, C represent the finger width and the contact width, respectively.

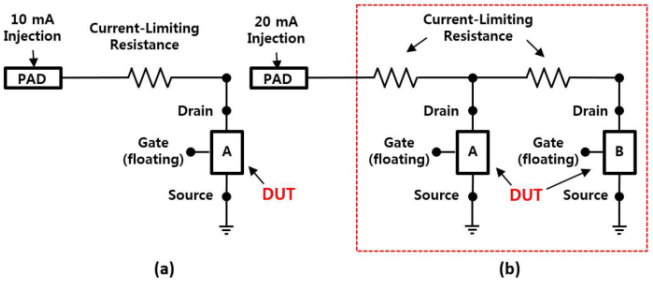

Fig. 1. Circuit diagrams of (a) single-device test and (b) mixed-mode test. DUT A denotes Tr. 1 and DUT B denotes Tr. 2 or Tr. 3.

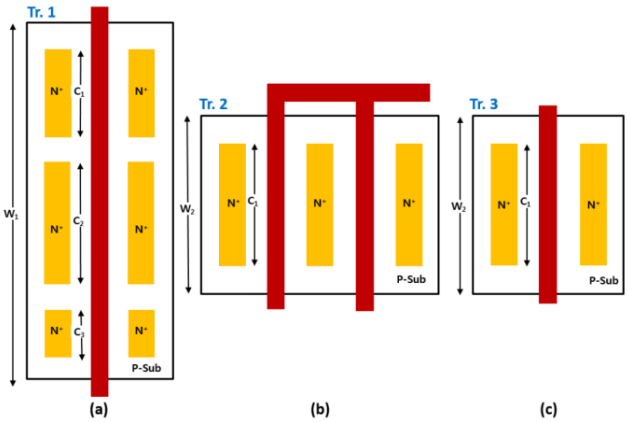

Fig. 2. Device layout top views of NMOS devices. Geometrical parameters such as W, C represent the finger width and the contact width, respectively. (a) Tr. 1. (b) Tr. 2. (c) Tr.3.

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TLP stress is injected through the PAD and current level is 10 mA for the single-device test and 20 mA for the mixed-mode test.

III. RESULTS AND DISCCUSIONS

Fig. 3 shows the simulated transient responses of both drain voltage and lattice temperature for TLP under the single-device test. Arrow in the figure indicates the point of failure of Tr. 3. In other words, Tr. 3 can't endure the injected current level and hot-spot ($T_{max} > T_{melting}$) is formed. This in turn results in an increase of possibility of device failures (second breakdown failure). In view of lattice temperature, Tr. 1 has the best ESD robustness (Tr. 1 > Tr. 2 > Tr. 3) among the three devices because most ESD damages are thermally initiated, as show in Fig. 3.

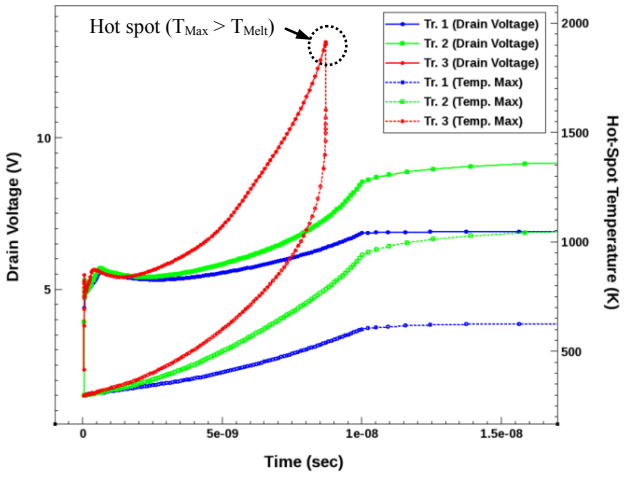


Fig. 3. Simulated transient responses of both drain voltage and lattice temperature for TLP under the single-device test.

In the mixed-mode test, however, ESD behavior are different aspect. Fig. 4 shows simulated transient responses of both drain voltage and drain current for TLP when both Tr.1 and Tr. 2 are connected to a single PAD. In the mixed-mode test, waveform of drain voltages of Tr. 1 and Tr. 2 are almost the same. Because of that, the injected current level through the PAD will be divided unequally into the two different devices.

In the single-device test, the drain voltage level of Tr. 2 ($V_{D, Tr. 2}$ = 9.3 V) is higher than that of Tr. 1 ($V_{D, Tr. 1}$ = 6.92 V) under the same drain current during pulse on time. In contrast, in the mixed-mode test, the drain current level of Tr. 1 is higher than that of Tr. 2 under the same drain voltage ($V_{D, Tr. 1+2}$ = 7.65 V), as shown in Fig. 4. At t = 0.7 ns, Tr. 1 is turned on first and the drain current of Tr. 2 shows snapback profile. Then, at t = 3.2 ns, Tr. 2 is turned on and the drain current of Tr. 1 shows snapback profile. In other words, when the device is turned on, current waveform of the other adjacent (or connected) devices show snapback profile. That is because, when Tr. 1 is turned on, the voltage required to sustain the same current level is reduced. Thus, the drain voltage shows snapback profile as shown in Fig. 4. However, the injected current increases until the peak of TLP is reached; thus, Tr. 1's current level increases continually. At this time, the node of drain of Tr. 2 is connected to the same node of Tr. 1; thus, the current of Tr. 2 follows the drain voltage. This in turn results in the snapback profile of the drain current of Tr. 2, as shown in Fig. 4.

Fig. 5 shows simulated transient responses of both drain voltage and drain current for TLP when Tr. 1 and Tr. 3 are connected under the mixed-mode test. As shown in previous case (Fig. 4), the multiple snapback profile is also observed. Tr. 1 is turned on first and the drain current of Tr. 3 shows snapback profile. Then, Tr. 3 is turned on and the drain current of Tr. 1 shows snapback profile. However, there is a big difference of drain voltage between the devices ($V_{D, Tr. 1}$ = 6.92 V, $V_{D, Tr. 3}$ > 13.2 V) under the single-device test. Thus, in the mixed-mode test, the drain voltage level of Tr. 1 is pulled up and that of Tr. 3 is pulled down to about 9.43 V (= $V_{D, Tr. 1+3}$), as shown in Fig. 5.

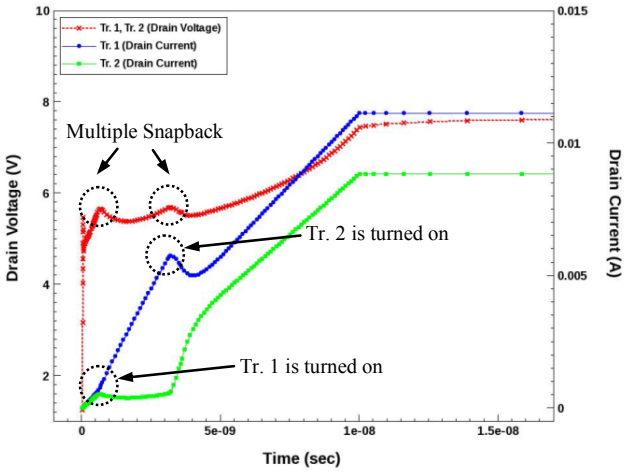


Fig. 4. Simulated transient responses of both drain voltage and drain current for TLP when Tr.1 and Tr. 2 are connected under the mixed-mode test.

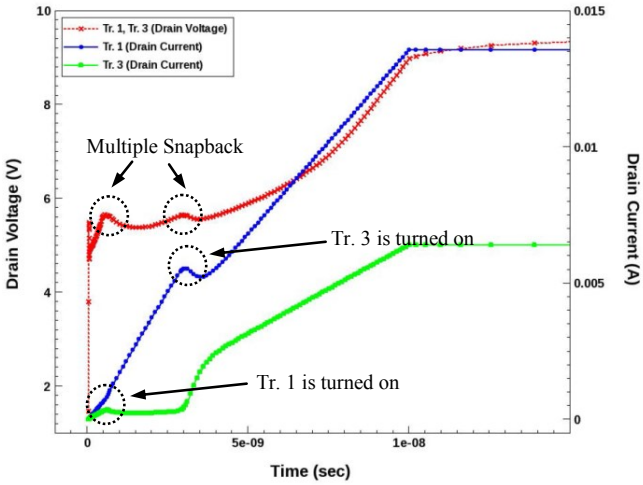


Fig. 5. Simulated transient responses of both drain voltage and drain currentfor TLP when Tr.1 and Tr. 3 are connected under the mixed-mode test.

This in turn results in the sharp increase in lattice temperature and the formation of hot-spot at Tr. 1 in the mixed-mode test with Tr. 1 and Tr. 3. In other words, if there is a big imbalance of ESD robustness between the devices under the mixed-mode test, the lattice temperature hot-spot may occurs at the device with better ESD performance among the devices.

Figs. 6 and 7 show simulated transient responses of max lattice temperature for TLP under the mixed-mode test. As shown in Fig. 6, after Tr. 1 is turned on first at t = 0.7 ns, the max lattice temperature of Tr. 1 increases further than that of Tr. 2. However, the turning on of Tr. 2 after t = 3.2 ns is accompanied by a sharp increase in lattice temperature. Finally, the lattice temperature of Tr. 2 will overtake Tr. 1's lattice temperature. This is because the ESD robustness of Tr. 1 is better than Tr. 2, as shown in Fig. 3 in the single-device test.

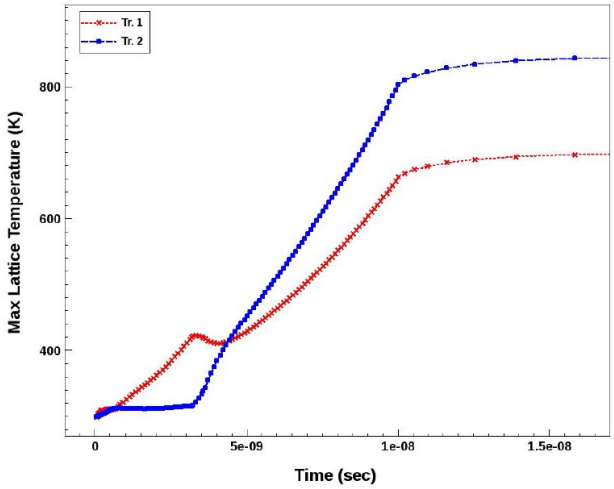


Fig. 6. Simulated transient responses of max lattice temperature for TLP when Tr.1 and Tr. 2 are connected under the mixed-mode test.

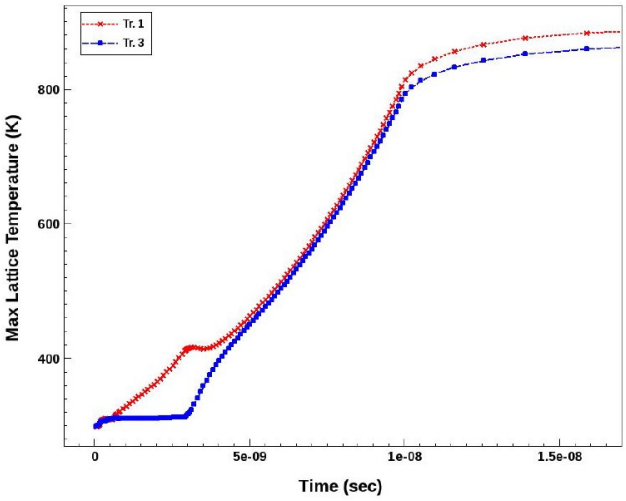
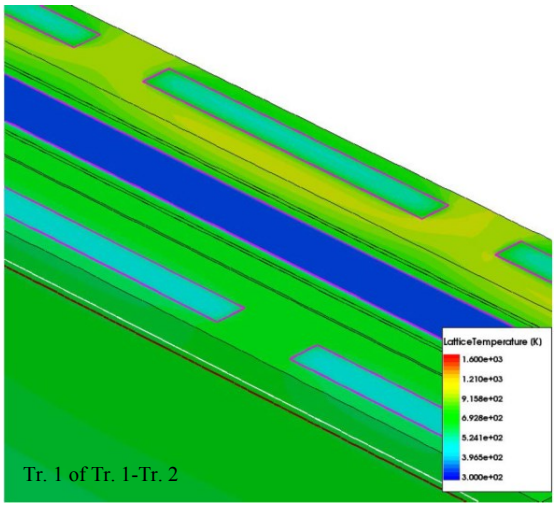


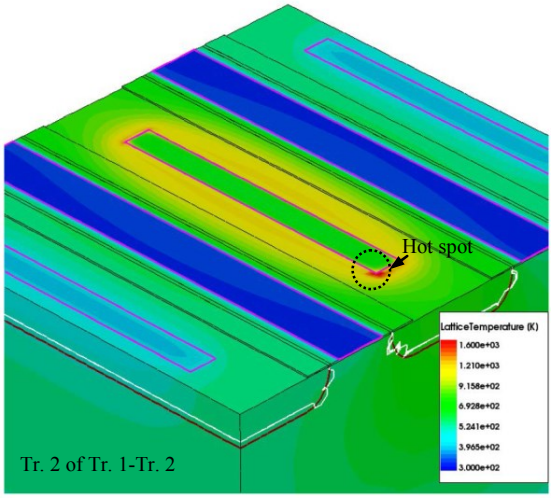
Fig. 7. Simulated transient responses of max lattice temperature for TLP when Tr.1 and Tr. 3 are connected under the mixed-mode test.

In the mixed-mode test with Tr. 1 and Tr. 3, a sharp increase in a lattice temperature of Tr. 3 is also observed after Tr. 3 is turned on. However, the lattice temperature of Tr. 3 can't overtake that of Tr. 1 even though Tr. 3 has the lowest ESD robustness in the single-device test, as shown in Fig. 7. This kind of mutual ESD behavior between the devices under TLP stress will eventually affect the ESD robustness as presented in Fig. 8.

Fig. 8 shows simulated lattice temperature hot-spot profiles in the mixed-mode test. TLP stress is injected through the PAD with current level of 25 mA for the hot-spot formation. Arrows in the figures indicate hot-spot as the position of possible failures. In the mixed-mode test with Tr. 1 and Tr. 2, the lattice temperature of Tr. 2 increases faster than that of Tr. 1. Thus, hot-spot is formed and failure occurs in the Tr. 2 as shown in Fig. 8 (b).

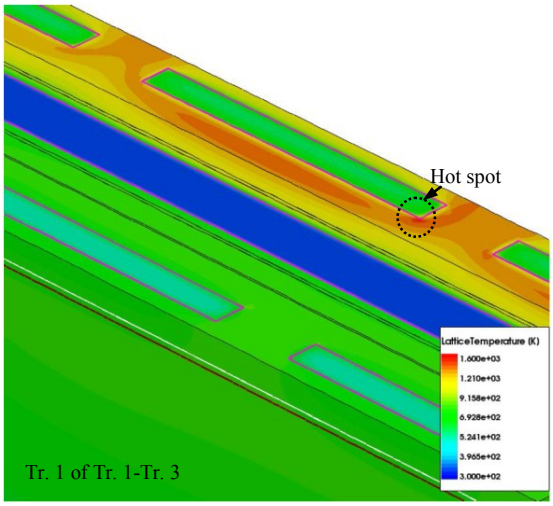


(a)

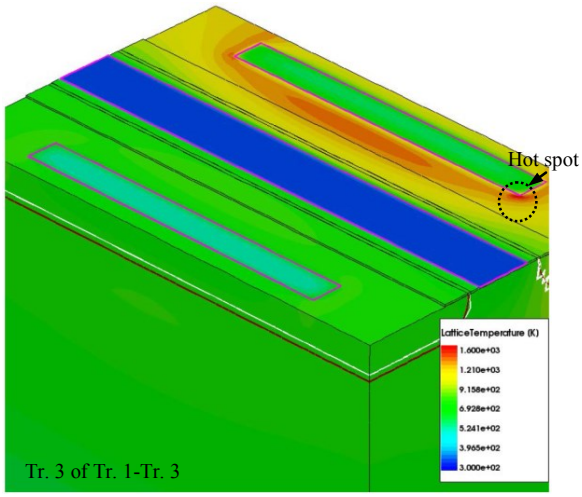


(b)

Fig. 8. Simulated lattice temperature hot-spot profiles in the mixed-mode test with Tr. 1-Tr. 2. Arrows in figures indicate hot-spots as the position of possible failures. (a) Tr. 1. (b) Tr. 2.



(a)



(b)

Fig. 9. Simulated lattice temperature hot-spot profiles in the mixed-mode test with Tr. 1-Tr. 3. Arrows in figures indicate hot-spots as the position of possible failures. (a) Tr. 1. (b) Tr. 3..

In contrast, the test with Tr. 1 and Tr. 3, the lattice temperature of Tr. 1 increases faster than that of Tr. 3 and the hot-spot is formed first in Tr. 1. Then, the hot-spot is also formed in Tr. 3, as shown in Fig. 9. As already discussed, this is because the adjacent device Tr. 3 has lower ESD robustness and Tr. 1's drain current level is pumped up for the unequal divide of the injected current. Thus, in the mixed-mode test with Tr. 1 and Tr. 3, hot-spot will be formed first in Tr. 1 even though Tr. 3 has the lowest ESD robustness among the other devices in the single-device test.

IV. CONCLUSION

In conclusion, mutual ESD behavior dependency between multiple devices under TLP stress has been presented. In the mixed-mode test, transient response of drain voltage has multiple (= total number of devices) snapback profiles.

When one of the devices in the mixed-mode test is turned on, the current waveform of the other adjacent devices shows snapback profile. This kind of mutual relation between the protection devices under TLP stress will eventually affect the ESD robustness. In other words, if there is a big imbalance of individual ESD characteristics between the devices under the mixed-mode test, the lattice temperature hot-spot and failure may occur in the device (ex. Tr. 1) even though the robustness of the other connected device (ex. Tr. 3) is lower than that of the device in the single-device test.

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