

Channel-Potential Based Compact Model of Double-Gate Tunneling FETs Considering Channel-Length Scaling

Peng Wu, *Jinyu Zhang, Li Zhang and Zhiping Yu
Institute of Microelectronics
Tsinghua University
Beijing 100084, China
*Email: zhangjinyu@tsinghua.edu.cn

Abstract—A channel-potential based compact I-V model for Double-Gate Tunneling FETs (DG-TFETs) incorporating channel length scaling is presented. The model covers both sub-threshold and strong-inversion operation regimes and achieves good agreement with TCAD results while the channel length is scaled down to 10nm. The effect and mechanism of channel length scaling on the performance of DG-TFETs are investigated. As expected, the scaling down of channel length deteriorates off-state and sub-threshold performance of DG-TFETs and leads to worse output saturation characteristics. However, our compact model provides a quick and quantitative means to assess the impact of TFET scaling on the device performance.

I. INTRODUCTION

Tunneling FETs (TFETs) are widely considered as a promising candidate for low power applications as they can achieve a steeper sub-threshold swing (SS) than the 60mV/dec limit of conventional MOSFETs by exploring the band-to-band tunneling (BTBT). In order to facilitate TFET circuit design and simulation, an accurate, physics-based compact model for TFETs is essential. A number of models of TFETs have been reported in literatures [1–3]. However, most of these models assume a zero electric-field region in the channel [1, 2], hence can only be applied to devices with sufficiently long channels. Furthermore, some models ignore the effects of inversion charge in the channel and fail to reproduce the well-known superlinear onset of output characteristics in TFETs and have poor accuracy for strong inversion.

In this paper, we present a channel-potential based I-V model which rectifies these deficiencies in TFET modeling and can predict the device performance correctly with the scaling down scenario. In order to verify our model, simulation is conducted using Sentaurus Device TCAD tool set. Dynamic nonlocal band-to-band tunneling model is used for accurate calculation of the tunneling current.

II. CHANNEL POTENTIAL MODELING

The device under study is an n-type DG-TFET shown in Fig. 1. Since band-to-band tunneling current is strongly dependent on the potential distribution in the channel, an accurate modeling of channel potential is needed. Therefore we start from channel potential modeling.

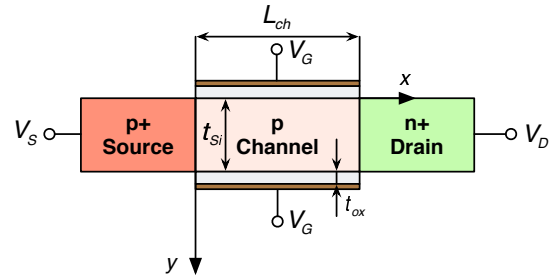


Fig. 1. Structure of n-type Double-Gate Tunneling FET studied in this paper. Doping of source, channel and drain: 10^{20} cm^{-3} , $5 \times 10^{14} \text{ cm}^{-3}$ and $5 \times 10^{18} \text{ cm}^{-3}$, respectively. Body thickness: 10nm. Gate dielectric: 3nm SiO_2 . Channel lengths: 10nm~50nm. Gate workfunction: 4.25eV

For a short-channel device, the 2D Poisson's equation in the channel region should be solved

$$\frac{\partial^2 \phi_{ch}(x, y)}{\partial x^2} + \frac{\partial^2 \phi_{ch}(x, y)}{\partial y^2} = \frac{qN_{ch}}{\epsilon_{Si}} \quad (1)$$

where ϕ_{ch} is the potential in the channel, and N_{ch} is the acceptor concentration in the channel. Inversion charge in the channel is ignored.

To simplify the problem, the potential distribution in the channel depth direction is approximated by a parabolic potential distribution [3]

$$\phi_{ch}(x, y) = \phi_{S, ch}(x) + a_1(x)y + a_2(x)y^2 \quad (2)$$

Considering boundary conditions at the top and bottom surfaces of the channel

$$\phi_{ch}(x, 0) = \phi_{S, ch}(x) \quad (3)$$

$$\phi_{ch}(x, t_{Si}) = \phi_{S, ch}(x) \quad (4)$$

$$\left(\frac{\partial \phi_{ch}(x, y)}{\partial y} \right)_{y=0} = - \frac{\epsilon_{ox}}{\epsilon_{Si} t_{ox}} (V_G - V_{FB}) \quad (5)$$

$$\left(\frac{\partial \phi_{ch}(x, y)}{\partial y} \right)_{y=t_{Si}} = \frac{\epsilon_{ox}}{\epsilon_{Si} t_{ox}} (V_G - V_{FB}) \quad (6)$$

The coefficients in (2) can be solved

$$a_1(x) = -\frac{\varepsilon_{\text{ox}}}{\varepsilon_{\text{Si}}} \frac{V_G - V_{\text{FB}} - \phi_{S,\text{ch}}(x)}{t_{\text{ox}}} \quad (7)$$

$$a_2(x) = \frac{\varepsilon_{\text{ox}}}{\varepsilon_{\text{Si}}} \frac{V_G - V_{\text{FB}} - \phi_{S,\text{ch}}(x)}{t_{\text{ox}} t_{\text{Si}}} \quad (8)$$

The 2D Poisson's equation (1) is reduced to a 1D differential equation of surface potential

$$\frac{d^2 \phi_{S,\text{ch}}(x)}{dx^2} = \frac{\phi_{S,\text{ch}}(x) - \psi_{ch}}{\lambda_0^2} \quad (9)$$

where

$$\psi_{ch} = V_G - V_{\text{FB}} - \frac{qN_{\text{ch}} t_{\text{Si}} t_{\text{ox}}}{2\varepsilon_{\text{ox}}} \quad (10)$$

The potential profiles in source and drain depletion regions can be approximated as one-sided $p^+ - p/n$ and $p/n - n^+$ junctions

$$\phi_{S,S}(x) = V_{S0} + \frac{qN_S}{2\varepsilon_{\text{Si}}} (x + L_S)^2, \quad -L_S < x < 0 \quad (11)$$

$$\phi_{S,D}(x) = V_D + V_{D0} - \frac{qN_D}{2\varepsilon_{\text{Si}}} (x - L_{\text{ch}} - L_D)^2, \quad L_{\text{ch}} < x < L_{\text{ch}} + L_D \quad (12)$$

where

$$L_S = \sqrt{\frac{2\varepsilon_{\text{Si}} V_{S,\text{dep}}}{qN_S}} \quad (13)$$

$$L_D = \sqrt{\frac{2\varepsilon_{\text{Si}} V_{D,\text{dep}}}{qN_D}} \quad (14)$$

and $V_{S,\text{dep}}$ and $V_{D,\text{dep}}$ are potential drops in source and drain depletion regions, which are to be solved using boundary conditions.

By enforcing continuity of potential and E-field at the boundaries of channel and source/drain depletion regions, surface potential in the channel can be solved

$$\begin{aligned} \phi_{S,\text{ch}}(x) = & \psi_{ch} + \frac{V_{S0} + V_{S,\text{dep}} - \psi_{ch}}{\sinh\left(\frac{L_{\text{ch}}}{\lambda_0}\right)} \sinh\left(\frac{L_{\text{ch}} - x}{\lambda_0}\right) \\ & + \frac{V_D + V_{D0} + V_{D,\text{dep}} - \psi_{ch}}{\sinh\left(\frac{L_{\text{ch}}}{\lambda_0}\right)} \sinh\left(\frac{x}{\lambda_0}\right), \quad (15) \\ & 0 < x < L_{\text{ch}} \end{aligned}$$

where

$$\lambda_0 = \sqrt{\frac{\varepsilon_{\text{Si}} t_{\text{ox}} t_{\text{Si}}}{2\varepsilon_{\text{ox}}}} \quad (16)$$

$$V_{S,\text{dep}} = \psi_{ch} - V_{S0} + \frac{qN_S \lambda_0^2}{\varepsilon_{\text{Si}}} \tanh^2\left(\frac{L_{\text{ch}}}{\lambda_0}\right) \quad (17)$$

$$- \sqrt{\frac{2qN_S \lambda_0^2 (\psi_{ch} - V_{S0})}{\varepsilon_{\text{Si}}} \tanh^2\left(\frac{L_{\text{ch}}}{\lambda_0}\right) + \left(\frac{qN_S \lambda_0^2}{\varepsilon_{\text{Si}}} \tanh^2\left(\frac{L_{\text{ch}}}{\lambda_0}\right)\right)^2}$$

$$V_{D,\text{dep}} = V_D + V_{D0} - \psi_{ch} - \frac{qN_D \lambda_0^2}{\varepsilon_{\text{Si}}} \tanh^2\left(\frac{L_{\text{ch}}}{\lambda_0}\right) \quad (18)$$

$$+ \sqrt{\frac{2qN_D \lambda_0^2 (V_D + V_{D0} - \psi_{ch})}{\varepsilon_{\text{Si}}} \tanh^2\left(\frac{L_{\text{ch}}}{\lambda_0}\right) + \left(\frac{qN_D \lambda_0^2}{\varepsilon_{\text{Si}}} \tanh^2\left(\frac{L_{\text{ch}}}{\lambda_0}\right)\right)^2}$$

In order to incorporate the impact of inversion charge in the channel, several corrections are made in strong inversion operation regime.

Firstly, the ‘‘mid-channel’’ potential ψ_{ch} saturates as inversion charge becomes prominent. ψ_{ch} serves as constant term in (15) and in a long channel device, it refers to the surface potential in the middle of the channel, which is far from the influence of source and drain junctions. Since the drain-to-source voltage mainly drops on the tunneling barrier, Fermi level in the channel is in equilibrium with the drain in strong inversion, therefore ψ_{ch} is mainly controlled by V_D rather than V_G in this regime. This phenomenon is an intrinsic property of TFETs and is referred as ‘‘dual-modulation’’ effect in previous literature [2]. To capture this ‘‘dual-modulation’’ effect, mid-channel potential ψ_{ch} is corrected as

$$\psi_{\text{dep}} = V_G - V_{\text{FB}} - \frac{qN_{\text{ch}} t_{\text{Si}} t_{\text{ox}}}{2\varepsilon_{\text{ox}}} \quad (19)$$

$$\psi_{\text{inv}} = V_D + \Phi + \alpha(\psi_{\text{dep}} - V_D - \Phi) + \beta(\psi_{\text{dep}} - V_D - \Phi)^2 \quad (20)$$

$$\begin{aligned} \psi_{ch} = & F(\psi_{\text{dep}}, \psi_{\text{inv}}) \\ = & \psi_{\text{dep}} + \psi_{\text{inv}} - \sqrt{(\psi_{\text{dep}} - \psi_{\text{inv}})^2 + \delta^2} \quad (21) \end{aligned}$$

where

$$\Phi = \frac{kT}{q} \frac{N_{\text{ch}} N_{\text{tran}}}{n_i^2} \quad (22)$$

is the band-bending at transition, N_{tran} is inversion charge density at transition, with an empirical value $1 \times 10^{19} \text{ cm}^{-3}$, F is a smoothing function, α, β, δ are fitting parameters.

Fig. 2 shows modeled ψ_{ch} along with TCAD results. From the figure, we can see that the model captures the ‘‘dual-modulation’’ effect very well.

Secondly, the characteristic length for the surface potential distribution along the channel direction in the tunneling region decreases with increased inversion charge (as derived from the variational analysis [4]).

$$1/\lambda^2 = 1/\lambda_0^2 + 8N_{\text{inv}}/\varepsilon_{\text{Si}} t_{\text{Si}} (\psi_{ch} - \psi_{ch,0}) \quad (23)$$

where

$$N_{\text{inv}} = 2C_{\text{ox}}(V_G - V_{\text{FB}} - \psi_{ch}) \quad (24)$$

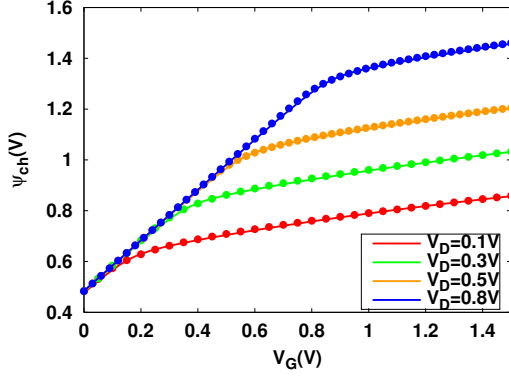


Fig. 2. $\psi_{ch} - V_G$ under different drain biases. Symbols: TCAD results. Lines: Model.

is the inversion charge in the channel and $\psi_{ch,0}$ is mid-channel potential at flat-band.

Fig. 3 shows modeled surface potential and TCAD results. Since the effects of source/drain depletion regions and the effects of inversion charge in the channel are considered, the model works well for both short channel and long channel DG-TFETs under both low and high gate biases.

III. CURRENT MODELING

The next step is to calculate the tunneling current based on the surface potential model. Using Kane's Model [5], the generation rate for band-to-band tunneling can be calculated

$$G_{\text{BTBT}} = A_{\text{Kane}} \frac{E^2}{\sqrt{E_g}} \exp\left(-\frac{B_{\text{Kane}} E_g^{3/2}}{E}\right) \quad (25)$$

where $E = \frac{E_g}{qL_{\text{tun}}}$, L_{tun} is tunneling path length derived from surface potential model

$$L_{\text{tun}}(V) = L_S - \sqrt{\frac{2\epsilon_{\text{Si}}}{qN_S}(V - V_{S0})} + L_{ch} - \lambda \operatorname{arccosh}\left[1 + \left(\cosh\frac{L_{ch}}{\lambda} - 1\right) \frac{\psi_{ch} - V - E_g}{\psi_{ch} - V_{S0} - V_{S,dep}}\right] \quad (26)$$

The tunneling current can be calculated by integrating the generation rate over the volume of the tunneling window

$$I = q \int G_{\text{BTBT}}(f_S - f_D) dx dy \quad (27)$$

where

$$f_{S/D} = \frac{1}{1 + \exp\left(\frac{qV(x) - E_{F,S/D}}{kT}\right)} \quad (28)$$

are Fermi distribution functions in source and drain.

By assuming that the tunneling current is uniform in y -direction, (27) is simplified to

$$I = qt_{\text{Si}} \int G_{\text{BTBT}}(x)(f_S - f_D) dx \quad (29)$$

Thus a compact current model is developed based on the surface potential model. Figs. 4 and 5 show modeled current of

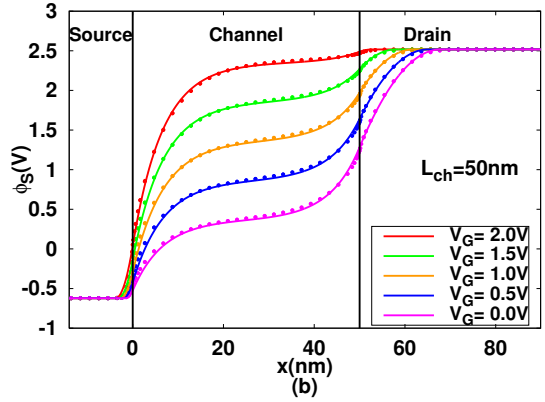
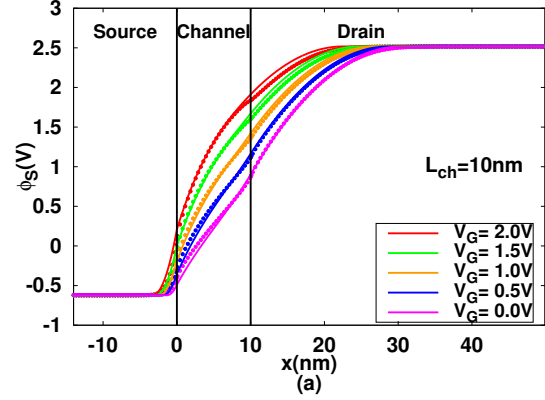


Fig. 3. Surface potential profile of DG-TFETs with channel lengths of (a) 10nm (b) 50nm. $V_D=2.0\text{V}$. V_G ranges from -2V to 2V. Symbols: TCAD results. Lines: Model.

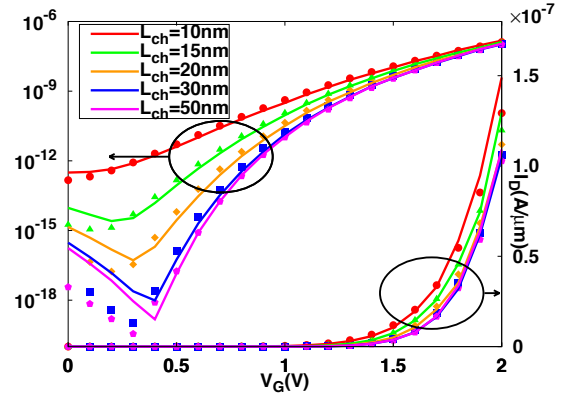


Fig. 4. $I_D - V_G$ characteristic of DG-TFETs with different channel lengths. $V_D=2.0\text{V}$. Symbols: TCAD results. Lines: Model.

DG-TFETs along with TCAD results. From these figures, we can see that our model well captures the channel length dependency of $I - V$ characteristics. In different operation regimes, including sub-threshold and strong inversion regimes, both transfer characteristic and superlinear onset and saturation in output characteristic are well modeled.

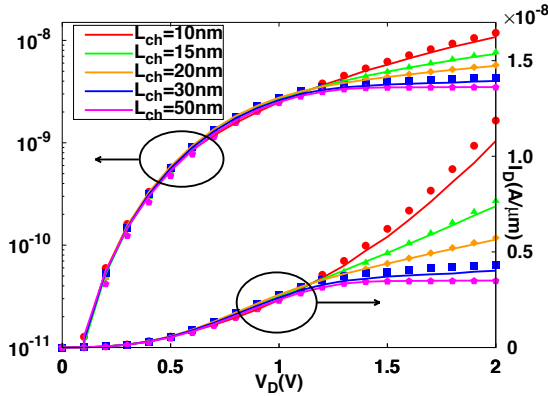


Fig. 5. I_D - V_D characteristic of DG-TFETs with different channel lengths. $V_G=1.5V$. Symbols: TCAD results. Lines: Model.

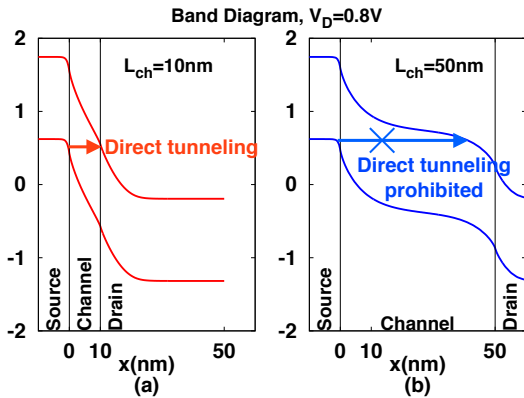


Fig. 6. Band diagram of DG-TFETs with different channel lengths at OFF-state. I_{OFF} is significantly higher with short channel length due to direct tunneling.

IV. DISCUSSION

As shown in Figs. 4 and 5, the down-scaling of channel length leads to a significantly higher OFF-state current (I_{OFF}) and sub-threshold swing (SS) and deteriorates the output saturation characteristics. This is similar to the short channel effects in conventional MOSFETs, yet the underlying mechanisms are different.

Fig. 6 shows the band diagram for DG-TFETs in the OFF-state. In a short channel DG-TFET (Fig. 6a), direct tunneling is significant, causing leakage current. While in a long channel DG-TFET (Fig. 6b), direct tunneling is prohibited due to long tunneling path.

Fig. 7 shows the band diagram for DG-TFETs in saturation. In a long channel DG-TFET (Fig. 7b), when the drain voltage continues to increase, only the channel potential near the drain increases, and tunneling window remains unaffected, leading to saturation of the drain current. However, in a short channel DG-TFET (Fig. 7a), increasing drain voltage affects channel potential in tunneling window and shortens the tunneling path, resulting in the increase of current even after saturation. The

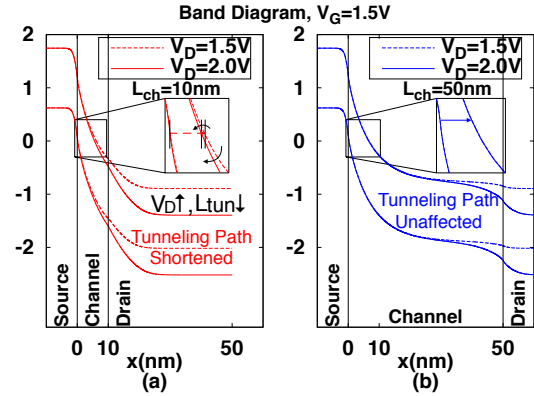


Fig. 7. Band diagram of DG-TFETs with different gate lengths in saturation region.

phenomenon is called drain-induced barrier thinning (DIBT), similar to DIBL effect in conventional MOSFETs which also leads to finite output conductance in saturation region.

V. CONCLUSION

A channel-potential based model for Double-Gate Tunnel FETs including channel length scaling has been developed, and based on the model, the mechanisms for the short channel effects are analyzed. Our model provides a guideline for the scaling down of Tunnel FETs and aids in circuit simulation and design with the scaling down scenario.

ACKNOWLEDGMENT

This work was supported in part by the 973 Program of China under Grant 2011CBA00600 and Grant 2011CB933004, in part by the Important National Science and Technology Special Projects of China under Grant 2011ZX02707.

REFERENCES

- [1] L. Zhang and M. Chan, "SPICE modeling of double-gate tunnel-FETs including channel transports," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 300–307, Feb 2014.
- [2] C. Wu, R. Huang, Q. Huang, C. Wang, J. Wang, and Y. Wang, "An analytical surface potential model accounting for the dual-modulation effects in tunnel FETs," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2690–2696, Aug 2014.
- [3] M. Bardon, H. Neves, R. Puers, and C. Van Hoof, "Pseudo-two-dimensional model for double-gate tunnel FETs considering the junctions depletion regions," *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 827–834, April 2010.
- [4] C. Shen, S.-L. Ong, C.-H. Heng, G. Samudra, and Y.-C. Yeo, "A variational approach to the two-dimensional nonlinear poisson's equation for the modeling of tunneling transistors," *IEEE Electron Device Lett.*, vol. 29, no. 11, pp. 1252–1255, Nov 2008.
- [5] E. Kane, "Zener tunneling in semiconductors," *J. Phys. Chem. Solids*, vol. 12, no. 2, pp. 181–188, 1960.