Layout-Based TCAD Device Model Generation

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***Abstract*—In this work, a fully automated process emulation is presented. Starting from industrial standard gdsII mask files a user friendly and fast way to create TCAD ready models has been realized. A three step approach is used. The creation of virtual layers to allow for logical operation based on masks is shown. Then the geometrical and dopant profile instantiation is carried out. Third the mesh generation based on and optimized on the information of the first two steps is shown. Industry-relevant sample applications for the implemented work-flow ranging from a radiation hardened latch to a state of the art FinFET SRAM cell are demonstrated.**

I. Introduction

In the past three-dimensional device models were needed only for a handful of TCAD applications e.g. the simulation of real three dimensional effects like an ion impact. But with the introduction of non-planar technologies like FinFETs [1] the demand of three-dimensional device models increased. Due to increasing complexity of recent technology generations, full process simulation is computational expensive and thus limited to a small number of devices [2]. In this work, we focus on the input generation for device simulation which is described in the first three steps of Fig. 1. As an alternative to process simulation we present a fast and efficient approach for creating three-dimensional device models of transistors or small cells directly from a mask layout using process emulation.

II. Method

A cell design is typically stored as gdsII mask file [3]. It contains a number of two-dimensional layers describing device regions (see Fig. 2). Typical device regions are the active region, doping wells, the contacts, and the interconnect structure.

Our method combines the layout with technology information of the target process to construct the device model. The technology information is stored in a separate file which describes rules how to convert the gdsII into a three-dimensional structure. It contains process parameters like doping concentration (N_{well}, $N_{contact}$, N_{sub}, etc.), layer thickness (oxide, epi, substrate, etc.), as well as additional bits of information to create an optimized device simulation model.

As shown in Fig. 3 the structure generation passes three processing steps: I) virtual layer creation, II) geometrical segment and doping profile generation, III) mesh generation for device simulation.

First, additional "virtual technology layers" are assigned by logic bool operations on the given layer to define helper masks (c.f. Fig. 4). For example, the contacts are specified using the contact mask but exclude three other masks as shown in the following listing. By referring to other sections e.g. `~Variables` very flexible definitions can be created where the result can be tweaked by changing a small parameter-set only.

```
/* Contact Active<->Metal1 (from GateLine)*/
+Layer_139 : LayerDefaults
{
   name       = "ContactActive";
   definition = "ContactMask \\ ( PolyMask |
       Spacer1Mask | Spacer2Mask )";
   onTopOf    = "Active";
   create     = true;
   thickness  = ~Variables.polyThickness +
       ~Variables.contactThickness;
   TypeSettings : ~SegmentDefaults
   {
      Material = "Conductor";
   }
}
```

Second, the geometrical layers are extruded to three-dimensional segments. In this step, the segment material is assigned. Also the vertical position (here: above `"Active"`), thickness and the material is specified. All data can be specified as shown in the above listing. Furthermore, similar to the geometrical segments, doping boxes with an analytical doping profile given by type, mode (i.e. Gauss, raised-cosine,...), maximum concentration (N), slopes (sigmas) are generated as shown in following listing and in Fig. 5.

```
+Layer_1011 : LayerDefaults
{
   definition = "Active & pplusMask";
   type       = "Doping";
   ...
   TypeSettings : ~TechXDopingDefaults
   {
      dopType   = "donor";
      mode      = "gauss";
      N         = ~Variables.PMOSdopingVth;
      xSigLeft  = ~Variables.dopingVthsigmaY;
      ...
   }
}
```

Finally, a mesh optimized for device simulation is generated based on information extracted from the gdsII file. Typical refinements are: a) refinement to interfaces like the oxide-semiconductor interface where the channel is induced by the gate, b) box refinements in electrical active regions like the fin or c) a refinement on the built-in potential (which is statically derived from the dopant concentration) to cover critical pn-junctions. In the following listing an exemplary specification

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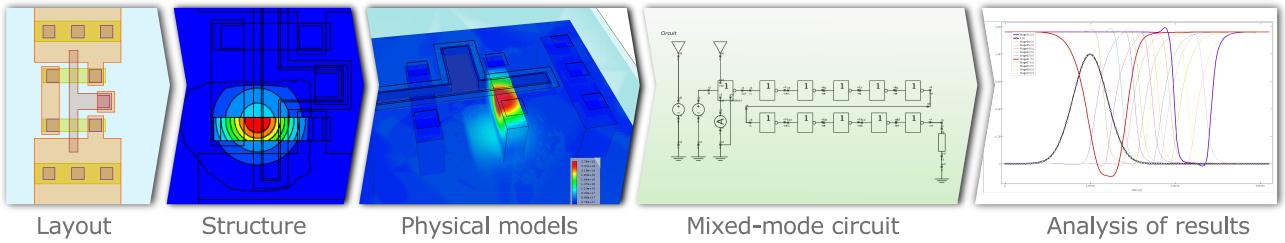

Figure 1. Starting with a gdsII layout the device structure is generated and processed using (selected) physical models and an optional mixed-mode circuit with compact devices. Finally, post processing and data analysis is carried out.

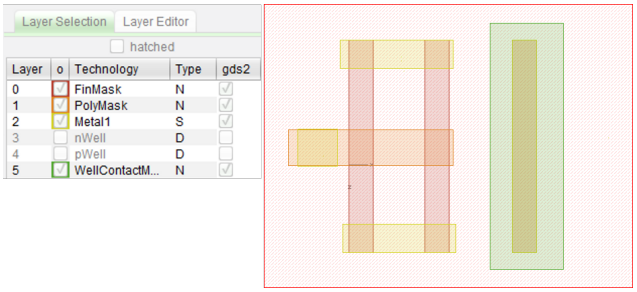

Figure 2. Typical layers of an nMOS transistor cell based on FinFET technology loaded from a gdsII file: FinMask, PolyMask, Metal, WellContact.

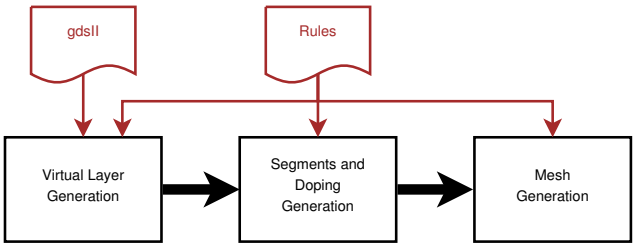

Figure 3. Process emulation flow from the gdsII mask file to a TCAD simulation ready model. First the gdsII file is used to create the (virtual) layers which are extruded in the next step to segments and doping profiles. Finally, a mesh optimized for device simulation is created. As the "Rules" file controls the complete work flow a user interaction is not needed to run the process.

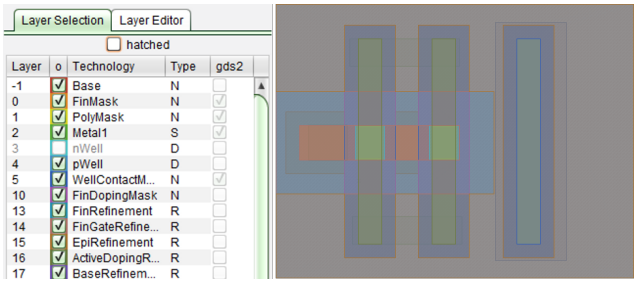

Figure 4. Virtual technology layers are created by logical operations. Combined with the original layer these "helper layers" are used to extrude device segments and boxes for doping profiles.

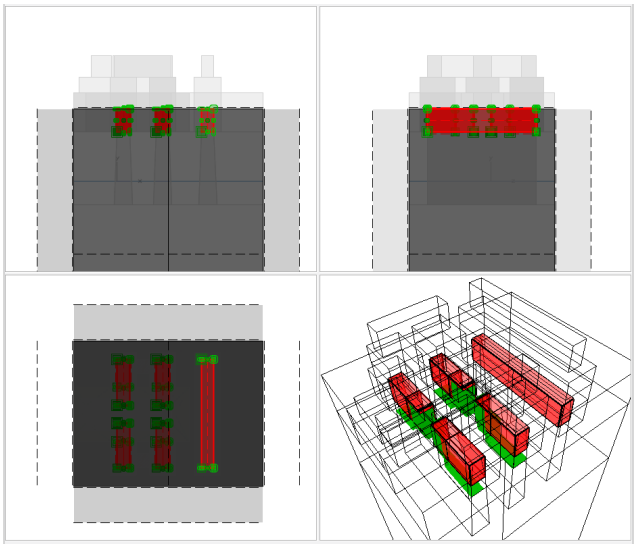

Figure 5. Doping boxes (red) for the source-drain doping and the resulting pn-junctions (green) in a live preview (lower right).

of a box refinement with a minimum tetrahedron size of 8 nm and an extension of the box size by 6 nm is given. Fig. 6 shows a typical usage of the refinement boxes for whole fins.

```
+Layer_1013
{
    ...
    TypeSettings : ~BoxRefineDefaults
    {
        mindist = 8 nm;
        xRight  = 6.0 nm;
        ...
    }
}
```

The process emulation directly creates a device model ready to run with our simulator Minimos-NT. Fig. 7 shows the output of the layout structure generation. The procedure is highly automated and needs a minimum of user interaction.

III. Applications

Device simulation from gdsII files enables a broad range of applications. Besides single transistors, it particularity targets small cells up to 20 transistors. Fig. 11 shows the doping profile of a device model of a radiation hardened latch [4].

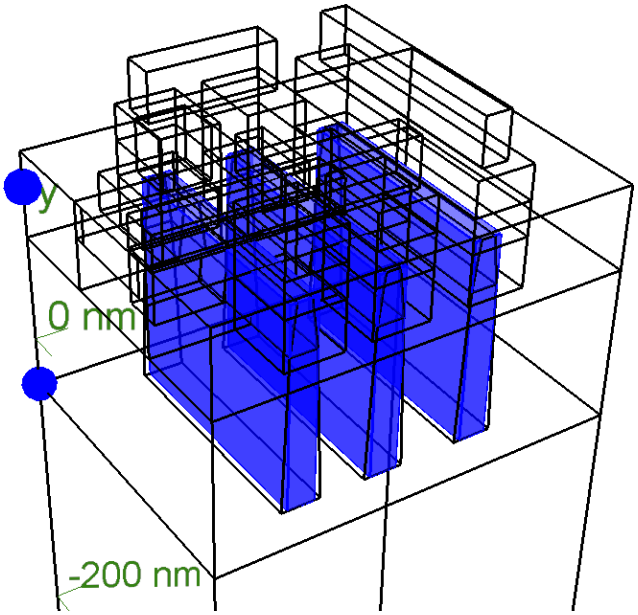

Figure 6. Refinement boxes can be used to generate an efficient tetrahedron grid. Within these boxes the maximum tetrahedron size can be specified. Here the refinements in the fin regions are shown.

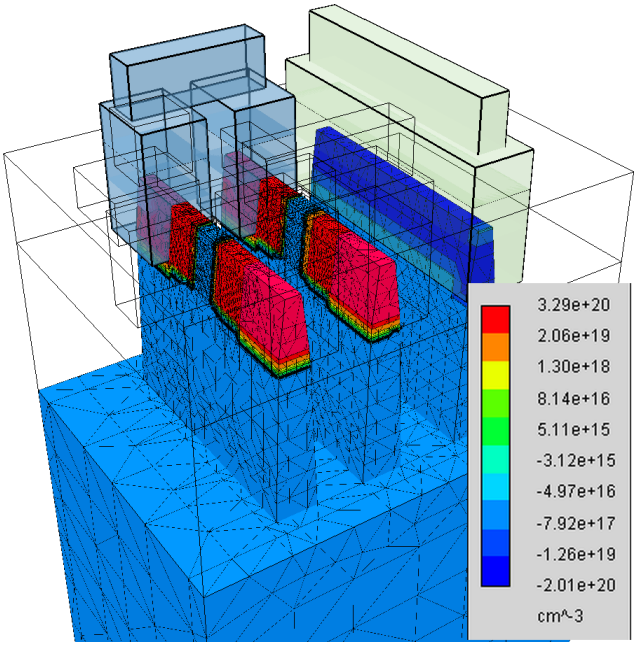

Figure 7. Net doping concentration and grid of an nMOS-FinFET. Additionally the source and the well contact are shown in transparent-blue and -green respectively.

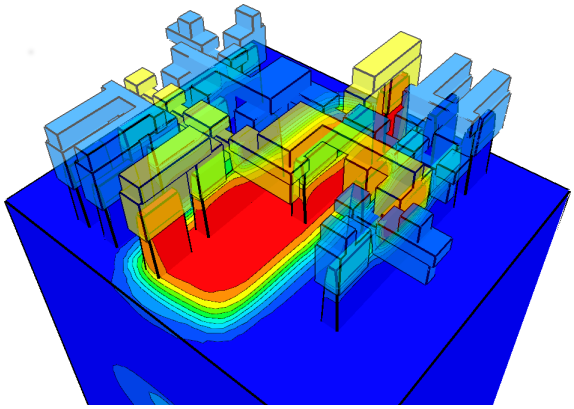

Figure 8. Potential and selected contacts/interconnects of a FinFET SRAM with 100 k vertices and 600 k tetrahedrons. The contact color corresponds with the potential (yellow is high potential, blue is low).

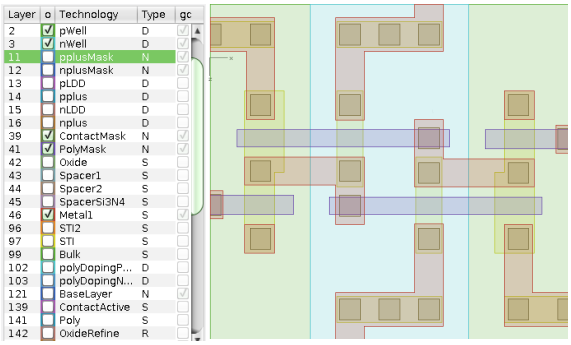

Figure 9. The gdsII layout of the 6T-SRAM cell. The bigger width of the pMOS transistors can be clearly seen (in the green region) The "Polymask" used for gate contacts is shown in blue/purple, the lowest metal connection layer is shown in red.

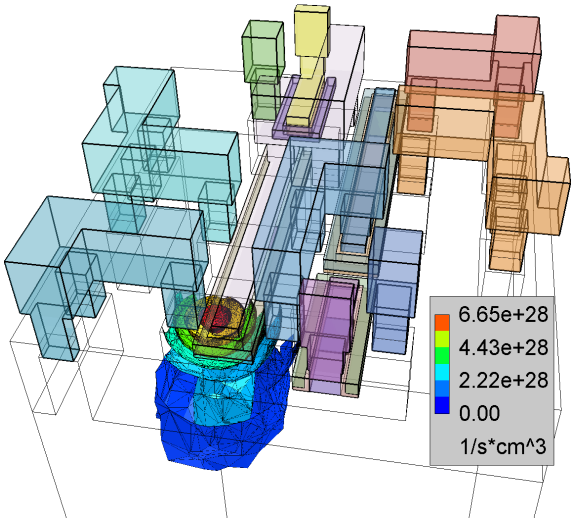

Figure 10. Carrier generation rate due to the impact of an heavy ion in a CMOS SRAM. Selected segments are shown in a transparent style. The position is between the source and gate contact which might have high impact in terms of contact currents and disturbance of the function.

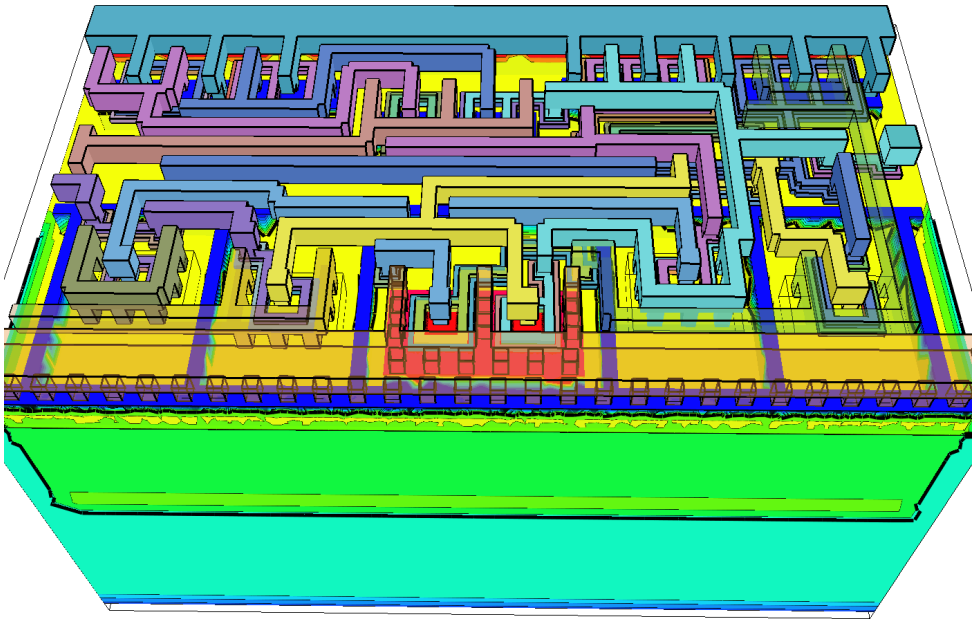

Figure 11. Net doping concentration and interconnect structure of an irradiation hardened latch with approx. 1 M vertices and 5 M tetrahedrons.

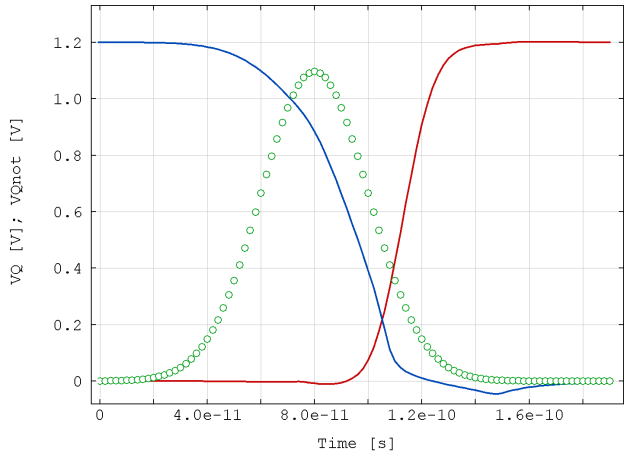

Figure 12. Contact potential plot of the CMOS SRAM with heavy ion impact. Continuous lines show the output contacts of the SRAM: Q (red) and $\overline{Q}$ (blue), the peak generation rate is about 1×10^{29} cm^{-3} (green circles, not to scale)

Our approach is flexible enough to target planar as well as upcoming non-planar device technology [1], see Fig. 8. We demonstrate an efficient simulation flow from structure generation to mixed-mode analysis [5] (Fig. 1). It is important to note that an arbitrary number of interconnect layers can be included, a necessity for cross-capacitance calculations [6].

Here, for an detailed analysis a typical application which requires three dimensional device simulation is chosen. A simulation of a single event upset (SEU) of a full 6-transistor SRAM cell due to high-energy particle interaction is carried out. A heavy ion model is used to calculate the resulting carrier generation in the device. This particle-device interaction causes the SRAM to change state, which is known as a single event upset (SEU).

The SRAM structure is created using the gdsII layout (see Fig. 9) and comprises more than 200.000 mesh nodes. Fig. 10 depicts the generation rate due to the ion beam impact. Fig. 12 shows the resulting potential changes at the output contacts.

IV. Conclusion

A fast method to create full 3D TCAD device models directly from industry standard gdsII files is presented. Our method can be applied by device engineers as well as cell designers to efficiently investigate transistors and device interaction on a TCAD level. We have demonstrated the tool's capabilities by applying the process to industry-relevant devices like an irradiation hardened latch and a FinFET SRAM cell.

References

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